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Design and Implementation of a Novel Multilevel DC-AC Inverter

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Abstract: ***A novel multilevel DC-AC inverter is proposed in this paper. A seven level AC output voltage is generated using the proposed multilevel with the befitting gate signals design. The total harmonic distortion in the sinusoidal output voltage reduced using low pass filter. With the suggested multi-level inverter the switching losses and the voltage stress of power devices can be reduced. The operating principles of the proposed inverter and the voltage balancing method of input capacitors are discussed. Finally, a laboratory model of multilevel inverter with 400 V input voltage and output 220 V_{rms} / 2kW is enforced. 16F877A PIC microcontroller is used to control the multilevel inverter with sinusoidal pulse-width modulation (SPWM).***

Keywords: Multilevel inverter, DC to AC inverter, Microcontroller, MPPT.

1. Introduction

As a result of high technology development, the demand and the quality of electric power is higher than before. The qualification of power device and power conversion technique is advanced as there is an improvement in semiconductor technology. One of the power converters which can transform DC to AC is called inverter. Electrical equipment such as uninterruptible power supply, servo motor, air-conditioning systemare powered by an inverter and smart grid compose of renewable energy. To satisfy different demands and characteristic of loads, the output frequency and voltage have to change with different loads.

In recent years, the amount of power equipment required is increasing and hence there is a serious issue of harmonic pollution in power systems. Several standards and regulations have been formulated to limit quality of harmonics and power factor of electric equipment. Furthermore, the industry demand higher power applications, the specification of power device is higher. IGBT cannot operate at high frequency in spite of features such as high power rating and high voltage stress. And the design of IGBT gate driver is complicated. MOSFET is the appropriate component to operate at high frequency, but power rating is not as good as IGBT. To solve the problem, many different topology of multilevel use low rating component at high power application.

The purpose of multilevel topology is to reduce voltage rating of power switch. Therefore, it usually use at high power application. Low dv/dt, low input current distortion, and lower switching frequency can be obtained by combining output voltages in multilevel form. As a result of advantages of multilevel topology, several topologies have emerged in recent years.

A novel multilevel inverter is designed and implemented in this paper. The major feature of the proposed topology is the reduction of power components. The sinusoidal pulse-width modulation (SPWM) is used to control proposed circuit by 16F877A PIC microcontroller.

2. Block Diagram

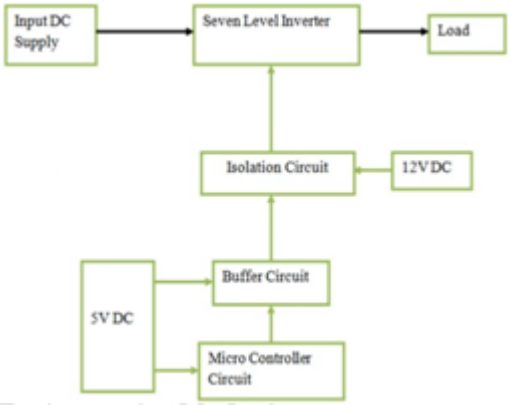

Figure 1: Block diagram of seven level inverter

1) **Isolation Circuit:** Damage to either of electrical circuit when one of them is under fault conditions can be prevented with the help of isolation circuit. High voltage and low voltage circuits can be isolated with this circuit. The isolation circuit is directly connected to seven-level inverter and a 12V DC is required to control the isolation circuit.
2) **Microcontroller Circuit:** The 16F877A PIC Microcontroller is used here. The microcontroller circuit is used to control the turning on and off of the switches of a seven level inverter. To control the microcontroller circuit we require a 5V DC. The microcontroller circuit is connected to a seven level inverter via isolation circuit.
3) **Load:** Multilevel structure is usually used in inductive loads such as motor. Thus, this paper applies the proposed topology in inductive load. We get output 220vrms/2 KW across the load.
4) **Buffer circuit:** It is used to provide transformation ofelectrical impedance from one circuit to another. To control the buffer circuit we require a 5V DC.
5) **Input DC supply:** We are providing a supply of 400V dc input voltage which is connected to a seven level inverter.

3. Circuit Diagram of Proposed Seven Level Inverter Topology

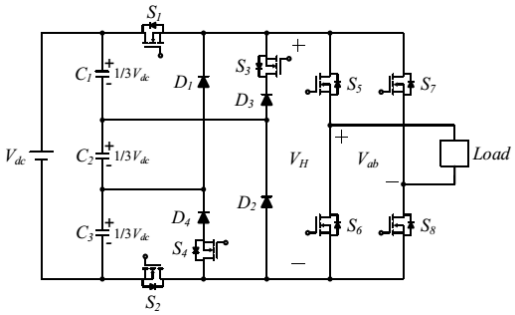

Figure 2: Circuit diagram of proposed seven-level inverter topology.

3.1 Circuit Configuration

Fig 2 shows the proposed novel topology used in the seven-level inverter. An input voltage divider is composed of three series capacitors C_1, C_2, and C_3. The divided voltage is transmitted to H-bridge by four MOSFET, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFET. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design.

3.2 Operating Principles

The required seven voltage output levels ($\pm 1/3V_{dc}$, $\pm 2/3V_{dc}$, $\pm V_{dc}$, 0) are generated as follows:

1) To generate a voltage level $V_o = 1/3V_{dc}$, switchS_1 is turned on at the positive half cycle while the energy is provided by the capacitor C_1 and the voltage across H-bridge is $1/3V_{dc}$. Then the switches S_5 and $S_8$are turned on and thus the voltage applied to the load terminals is $1/3V_{dc}$. Fig. 3 shows the current path at this mode.
2) To generate a voltage level $V_o = 2/3V_{dc}$, S_1 and S_4 are turned on while the energy is provided by the capacitor C_1 and $C_2$and the voltage across H-bridge is $2/3V_{dc}$,.Then the switches S_5 and $S_8$are turned on and thus the voltage applied to the load terminals is $2/3V_{dc}$. Fig. 4 shows the current path at this mode.
3) To generate a voltage level $V_o = V_{dc}$, S_1 and S_2 are turned on while the energy is provided by the capacitor C_1, C_2, andC_3 and the voltage across H-bridge is V_{dc}. Then the switches S_5 and $S_8$are turned on and thus the voltage applied to the load terminals is V_{dc}. Fig. 5 shows the current path at this mode.
4) To generate a voltage level $V_o = -1/3V_{dc}$, S_2 is turned on at the negative half cycle while the energy is provided by the capacitor C_3 and the voltage across H-bridge is $1/3V_{dc}$.Then the switchesS_6 and S_7 are turned on and thus the voltage applied to the load terminals is $-1/3V_{dc}$. Fig. 6shows the current path at this mode.
5) To generate a voltage level $V_o = -2/3V_{dc}$, S_2 and S_3 are turned on while the energy is provided by the capacitor C_2 and $C_3$and the voltage across H-bridge is $2/3V_{dc}$. Then the switches S_6 and S_7 are turned on and thus the voltage applied to the load terminals is $-2/3V_{dc}$. Fig. 7 shows the current path at this mode.
6) To generate a voltage level $V_o = -V_{dc}$, S_1 and S_2 are turned on while the energy is provided by the capacitor C_1, C_2, and C_3, the voltage across H-bridge is V_{dc}. Then the switches S_6 and S_7 are turned on and thus the voltage applied to the load terminals is $-V_{dc}$. Fig. 8 shows the current path at this mode.
7) To generate a voltage level $V_o = 0$, switchesS_5 and S_7 are turned on and thus the voltage applied to the load terminals is zero. Fig 9shows the current path at this mode.

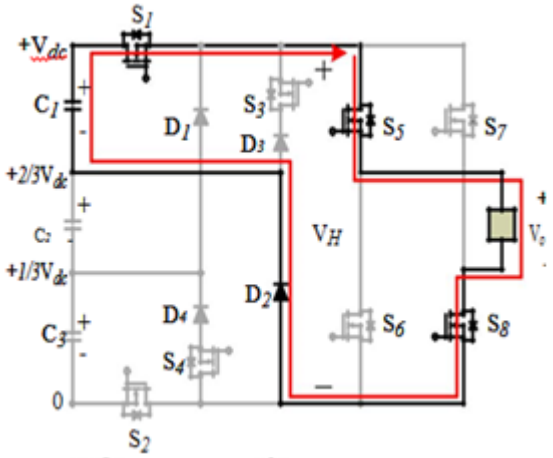

Figure 3: Switching combination of output voltage level $1/3V_{dc}$.

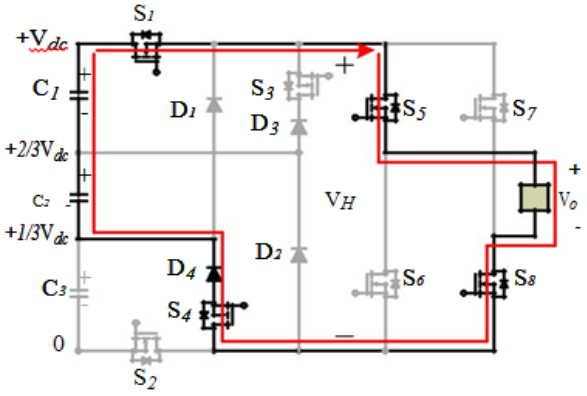

Figure 4: Switching combination of output voltage level $2/3V_{dc}$.

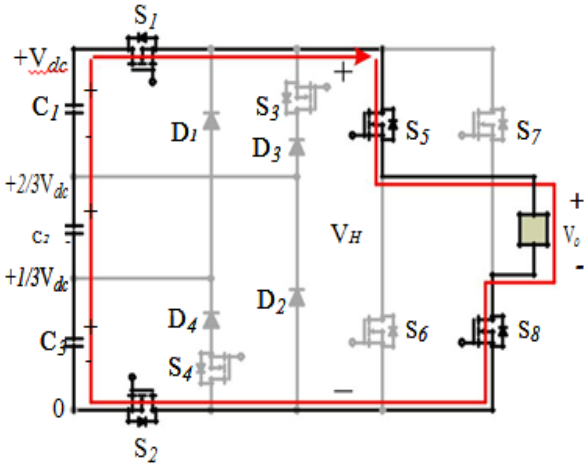

Figure 5: Switching combination of output voltage level V_{dc}

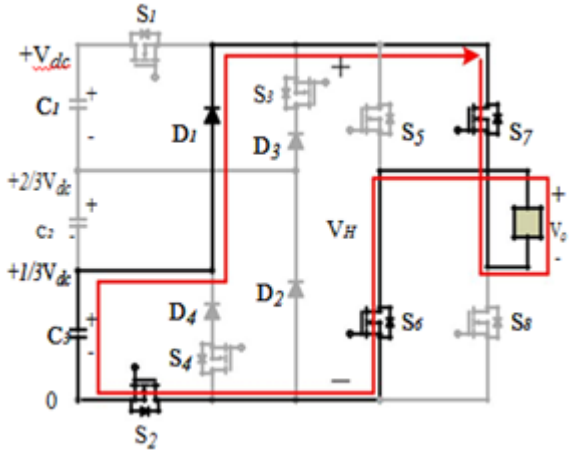

Figure 6: Switching combination of output voltage level -1/3V_{dc}.

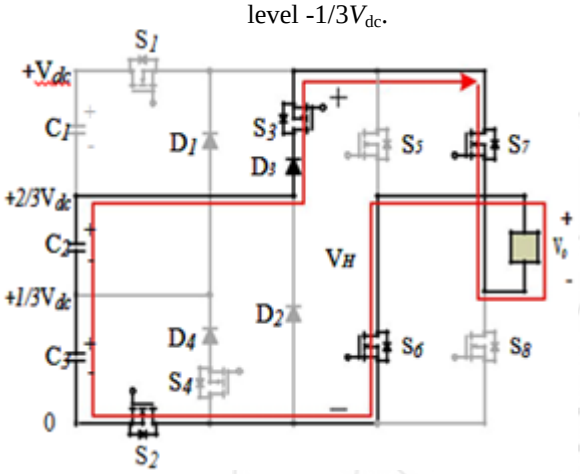

Figure 7: Switching combination of output voltage level -2/3V_{dc}.

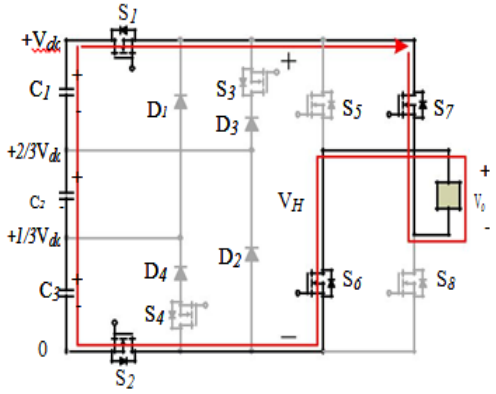

Figure 8: Switching combination of output voltage level -V_{dc}.

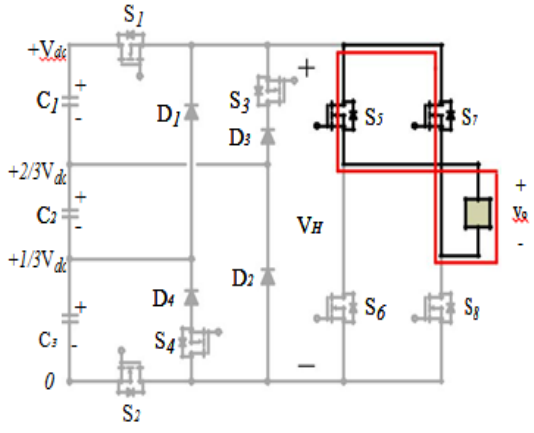

Figure 9: Switching combination of output voltage level 0.

Table 1: Switching combinations required togenerate the seven-level output voltage waveform

Output voltage Vo	Switching combinations							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1/3V_{dc}	on	off	Off	off	On	off	off	On
2/3V_{dc}	on	off	Off	on	On	off	off	On
V_{dc}	on	on	Off	off	On	off	off	On
-1/3V_{dc}	off	on	Off	off	off	on	On	Off
-2/3V_{dc}	off	on	On	off	off	on	On	Off
-V_{dc}	on	on	Off	off	off	on	On	Off
0	off	off	Off	off	On	off	On	Off

Table 2: Voltage stress comparison between four different seven level inverters

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

4. Experiment Results

A 16F877A PIC microcontroller is used to verify the proposed seven-level inverter. Table 3 shows the characteristics of the inverter. Fig 10shows the prototype of the proposed seven-level inverter.

Table 3: The specification of the proposed inverter

Input voltage V_{dc}	400 V
Output voltage V_o	220 V_{rms}
Rated output power P_o	2 kW
Switching frequency f_s	18 kHz

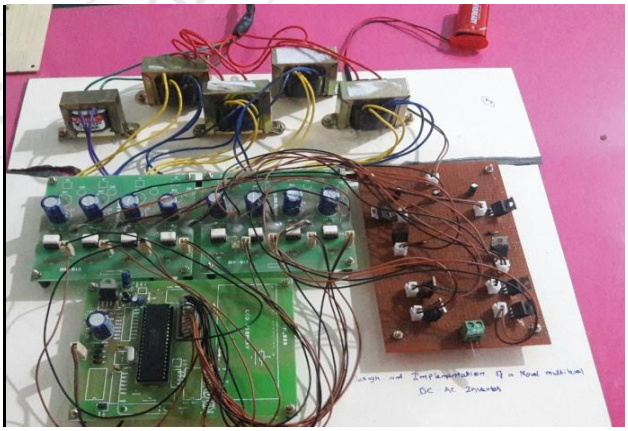

Figure 10: Experimental setup for the prototype

The efficiency at different output power is shown in Fig.11. The output power is from 200 W to 2000W. The highest efficiency is 96.9% at 800 W, and the lowest is 94.6% at 2000 W. The efficiency is always above 94.5%.

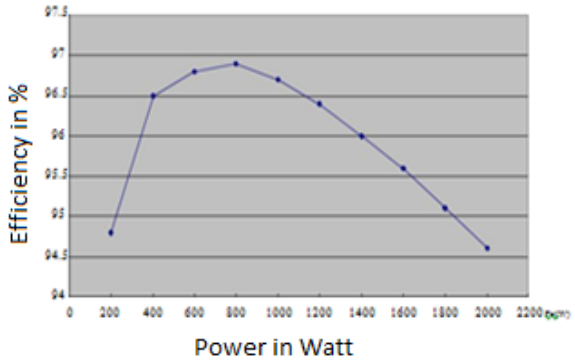

Figure 11: The efficiency of the proposed inverter

5. Simulation Result

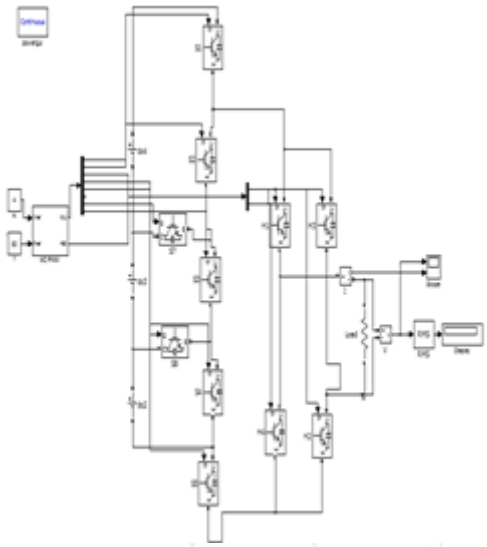

Figure 12: Simulation model for a seven level inverter

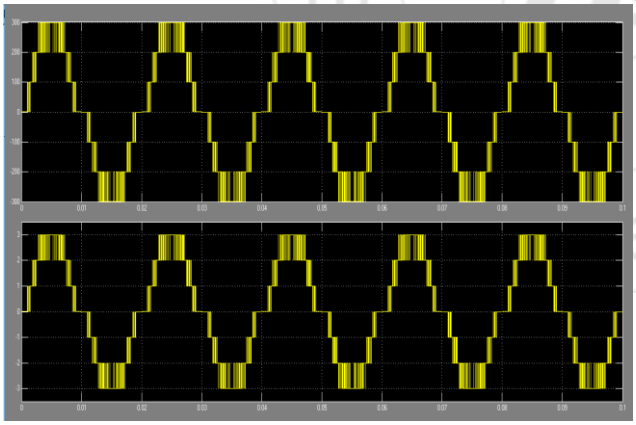

Figure 13: Output voltage and current for a seven level inverter

6. Conclusion

A novel seven-level inverter is designed and implemented with microcontroller in this paper. With this design the number of power devices will be reduced. The proposed system is compared with traditional structures. Finally, a laboratory model of seven-level inverter with 400 V input voltage and output 220 V_{rms} /2 kW is implemented. Experimental results show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.

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