International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391

Performance Evaluation of Binary to Gray Code Converters Using Quantum Dot Cellular Automata

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Abstract: ***Quantum dot-cellular automata (QCA) are potential alternatives to the conventional complementary metal-oxide semiconductor (CMOS) technology. In this technology, structures are formed using quantum cells and their sizes are at nanoregime. In QCA architectures QCA cell is a fundamental building block which is used to build logic devices and basic gates. This paper proposes various layouts of QCA based binary to gray code converter and evaluates the performance of various implementations. To verify the functionality of the proposed device, some physical proofs are provided. The proper functionality of binary to gray code converters is checked and validate by means of computer simulations using QCADesigner tool. We presented the various design methodology for binary to gray code converter. The comparison of various implementation of binary to gray code converter designs is also given.***

Keywords: Quantum dot Cellular Automata (QCA); Majority Logic, XOR gate, binary to gray code converters.

1. Introduction

According to Moore's law the numbers of components on an IC doubles every 18 months [1]. In recent times, complementary metal-oxide semiconductor (CMOS) technology faces some serious challenges in designing at nanoscale and reaches its physical limitations [2]. Quantum dot cellular automata is one of the technologies at nanoscale which is used to overcome the limits of CMOS. As the name of the technology shows, primitives constructed with cellular structure. It is first introduced by C. S. Lent et.al in 1993 [3]. QCA offers a revolutionary approach to computing at nano level. QCA technology has a wide range of advantages over CMOS such as reduced semiconductor device size ultralow power consumption; faster switching speed and highly dense structure. Operating frequencies for QCA are in the range of THz [4]. The fundamental unit of QCA is QCA cell. A set of symmetric QCA cells placed next to each other forming an interconnected architecture, transfer the information between cells due to the columbic interaction [5]-[6]. So, in QCA the information is transferred via columbic interaction rather in the form of electric current. So, power loss is negligible. Several studies have shown that QCA can be used to design general purpose computational and memory circuits [7]. Since every QCA circuit is implemented using majority and inverter gates, hence, efficiently construction of QCA circuits using majority gates has attracted a lot of attentions. Some alternative technologies for CMOS technology has been proposed by the International Technology Roadmap for Semiconductor (ITRS) [8]. QCA is one of them that work very well on nanoscale [9].

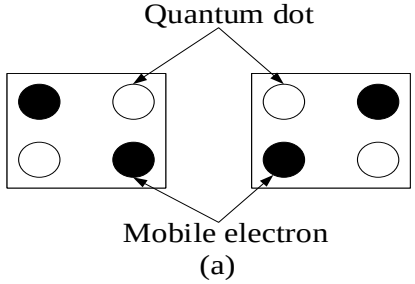
In this paper, we have proposed the four implementations of the QCA based binary to gray code converter and presented the simulation results of these individual designs. These can be used in development and design of specific communication circuits. A detailed comparison with regard to various features of these designs is also presented. The paper constitutes four sections. The first and second section provides the necessary introduction and review of QCA fundamentals. The third section presents the implementations of the various QCA binary to gray code converter topologies. Demonstration of the functionality and validation of the proposed architecture is done using QCADesigner [10]. The advantages of the proposed structures have been summed up as conclusion in the fourth section.

2. QCA Fundamentals

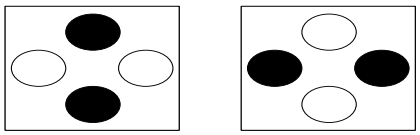
In this section, the basic building blocks of QCA and computation mechanism using QCA cells are described as below.

2.1 QCA cell

The QCA cell is the basic logic unit which has four quantum dots. Quantum dot is a semiconductor nanostructure that confines the movement of valence band holes, conduction band electrons in all three spatial directions. Quantum cell contains two mobile electrons or holes that repel each other due to mutual Columbic interaction and as a result they occupy farthest possible site i.e. diagonal sites of the cell. Electrons can tunnel between quantum dots but due to high potential barrier electrons cannot tunnel outside the cell. QCA cells are divided into two types. A type-1 QCA cell has shown in Figure 1(a). A type-2 QCA cell has four quantum dots at the midpoint of the sides of cells as shown in figure 1(b).



(a)



(b)

Figure 1: (a) type 1 (90°) QCA cell (b) type 2 (45°) QCA cell with opposite polarization.

The QCA cell may be in one of the two polarization state depending on the electron's position: polarization $P = +1$ and $P = -1$ corresponds to logic value '1' and '0' respectively. In these devices interaction among bits is required for binary computation. The interaction between the QCA cells is nonlinear that is it gets aligned with a slight modification in neighboring cell.

2.2 QCA wire

An array of QCA cells, that allows propagation of information known as QCA wire. In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. There are two type of QCA wire that can be used to form a circuit using QCA technology. Those are (a) 90° QCA wire (b) 45° QCA wire.

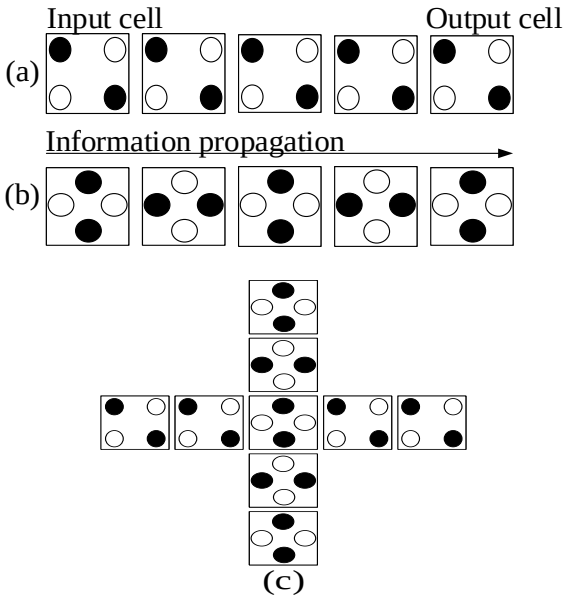


Figure 2: (a) QCA wire (90°); (b) QCA wire (45°); (c) coplanar wire crossing

In figure 2(a) adjacent cell has the same polarization so has minimum columbic repulsion. In second type of wire i.e. in figure 2(b) adjacent cells have opposite polarization [11]. The 45° rotated cells are used in coplanar wire crossing as shown in figure 2(c).

2.3 Majority gate

Other than Boolean logic, a different manner to implement digital operations is Majority logic. Majority logic manipulates and represents digital functions on the basis of majority decision instead of using Boolean logic operators (OR, AND and their complements) [12]. It is more sophisticated process than that of Boolean logic. Thus with the reduced number of logic gate we can implement a given digital function [13]-[14]. There are many types of majority gate viz. 3-input majority gate, 5-input majority gate, 7-input majority gate but the most effective and frequently used majority gate is 3-inputmajority gate.

From the figure 3(a) we can see 3 inputs majority gate requires only five QCA cells. It is a four-terminal logic gate in which three cells represents input terminals, one is output terminal and remaining one represents device cell [15]. Figure 3(b) is the symbolic representation of majority gate.

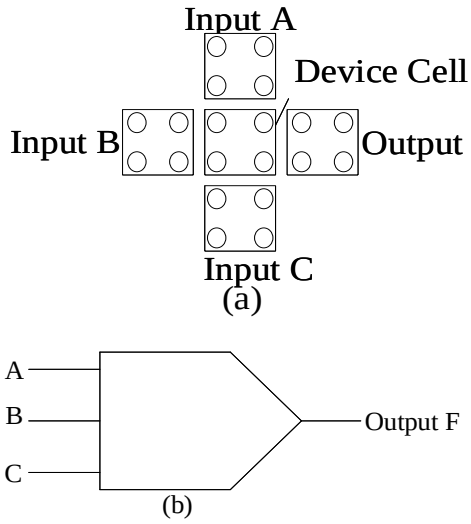


Figure 3: (a) majority gate and (b) its symbol

Let three input of majority gate as A, B, C then the logic function is:

$$M(A,B,C) = AB + BC + AC$$

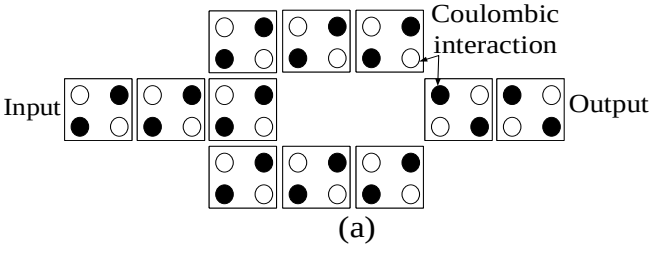
The 3-input majority gate can be converted into 2-input OR gate or 2-input AND gate by fixing one of three inputs to +1 or -1 respective [16].

OR Gate: $F = (A,B,1) = A + B$

AND gate: $F = M(A,B,O) = AB$

2.4 Inverter

Inverter can be implemented in two ways in QCA that are as shown in figure 4. The first inverter is built by neighboring QCA cells on the diagonal, which causes Coulomb forces to place the two electrons in opposing wells of the cell with respect to the source. An inverter can be formed by placing one cell touching the corner of the other cell. The electrostatic interaction is inverted, because the quantum dots corresponding to different polarizations are misaligned between the cells [17].



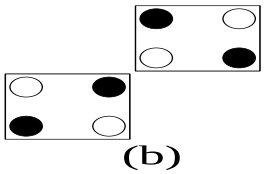
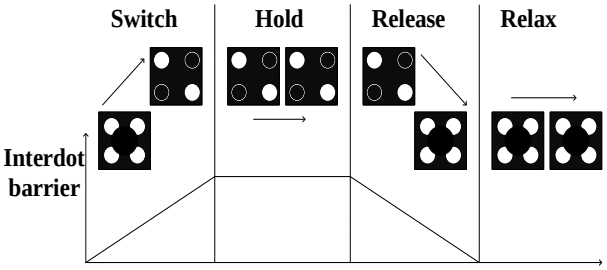


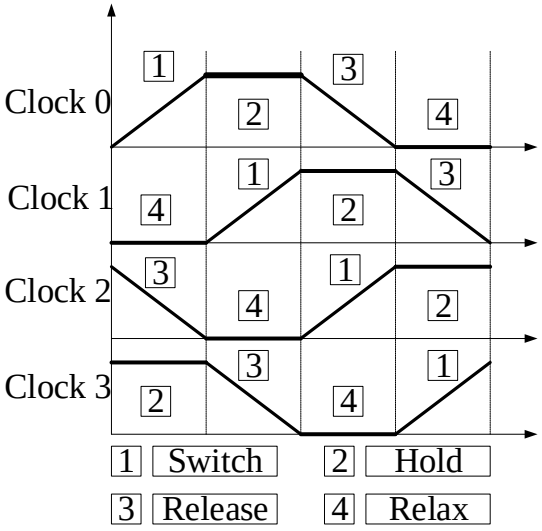
Figure 4: QCA inverters

2.5 Clocking

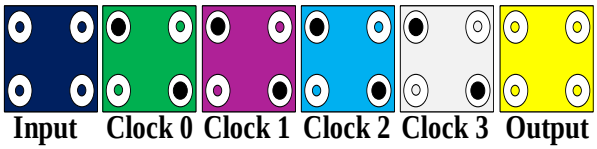
The clock is an electrical pulse that controls the tunneling barriers within a cell and hence keeps control on the polarization of the cell [18]. To control the direction of data flow In QCA technology, the cells of the circuits are divided into four segments, called clock zone. In each zone, barrier between the dots can be modulated using single potential.



(a)



(b)



(c)

Figure 5: (a) four phase of clocking (b) four clocks with each one lagging its prior 90◦ (c) switching of signal

There are four phases of QCA clocking zones namely switch (low to high), hold (high), release (high to low) and relax (low) [19]. The phase of each clock zone is shifted by 90 degrees to the previous one as shown in figure 5(b). Proper switching of QCA array can be ensured by QCA clocking.

From the figure 5(a) we can see that in the switch phase, the interdot potential barrier is raised gradually, so QCA cells settle down to one of the polarization state influenced by neighboring cell during this phase. Interdot potential is high in hold phase. In release and relax phase interdot potential is lowered so QCA cells are unpolarized. To implement QCA circuit switching of the clock is as shown in figure 5(c).

3. QCA implementation of binary to gray code converter

3.1 Ex-OR Gate

In digital logic Exclusive-OR gate is required for wide range of applications such as arithmetic and logic unit, reversible logic circuit, parity checking and detection circuit, code inverter etc. That's why it is highly required to design XOR with low power consumption and high speed. XOR Symbol is shown in figure 6 and the truth table for XOR gate is shown in table 1.

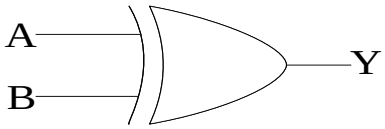


Figure 6: XOR symbol

Table 1: Truth table for the XOR gate

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

3.2 Binary to gray code converter

A code is symbolic representation of digital information. In digital electronics, there are many types of code as binary code, excess three code, binary coded decimal (BCD), gray code and many more. Code converter is a combinational circuit that converts one code into another. One of the most commonly used code gray code. Gray code is a unit distance and non-weighted code.

Let four binary bits B0, B1, B2 and B3 are applied at the binary to gray code converter as the inputs and corresponding outputs are G0, G1, G2 and G3. The truth table of four-bit binary to gray code converter is shown in table 2. From the table, it can be seen that the output G0 is same as the input B0. The output G1 is XORed value of B0 and B1; G2 is XORed value of B1 and B2; G3 is XORed value of B2 and B3. Logic diagram of binary to gray code convertor shown in figure 7 and truth table of it is shown in table 2.

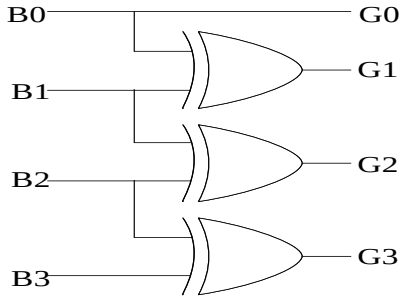


Figure 7: logic diagram of binary to gray code converter

Binary to gray code conversion:

- The MSB (Most Significant bit) of gray code can be obtained by simply copying the MSB of binary code
- Other bits of the output gray code can be obtained by XORing binary code bit at that index and previous index.

Gray code equivalent of the given binary number in the equation form can be represented as follows:

$G0 = B0$
$G1 = B0 \oplus B1$
$G2 = B1 \oplus B2$
$G3 = B2 \oplus B3$

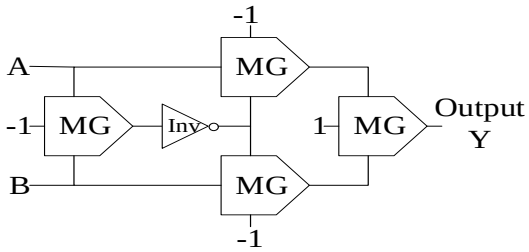
Table 2: Truth table of binary to gray converter

Inputs				Outputs			
B0	B1	B2	B3	G0	G1	G2	G3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

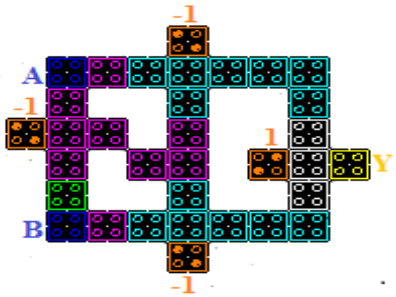
3.3 The first design

The logic used in the first design is given in equation 1 and simplified as:

$$Y = \overline{A.B}.A + \overline{A.B}.B \quad (1)$$
$$Y = (\bar{A} + \bar{B}).A + (\bar{A} + \bar{B}).B$$
$$Y = \bar{A}.A + \bar{B}.A + \bar{A}.B + \bar{B}.B$$
$$Y = \bar{A}B + A\bar{B}$$



(a)



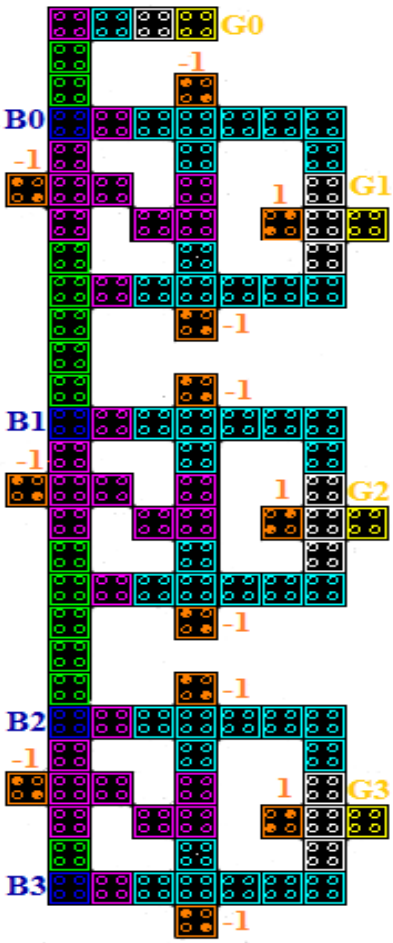
(b)

Figure 8: (a) Schematic and (b) layout of first XOR gate

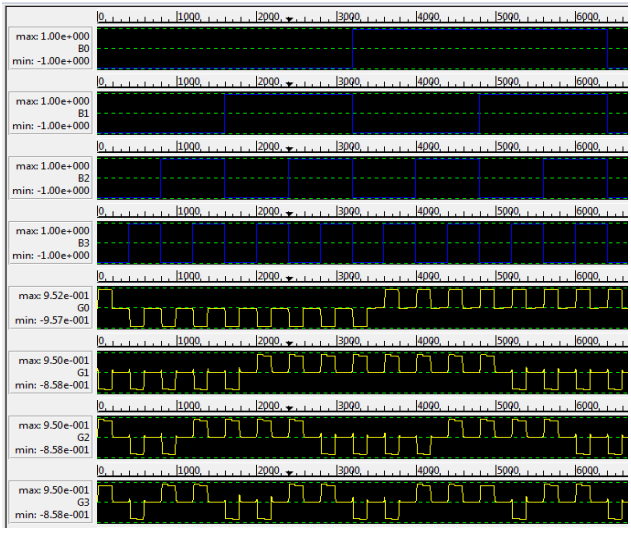
XOR gate shown in figure 8(b) that is used to develop binary to gray code converter shown in figure 9(a) is proposed by another author [20]. This XOR requires four majority gate and inverter with zero crossover. The output of XOR gate in the form of majority logic, represented by figure 8(a) can be written as:

$$Y = M(M(A, \overline{A.B}, -1), M(B.\overline{A.B}, -1), 1)$$

The proposed binary to gray code converter, shown in figure 9(a) has a complexity of 111 cells and $0.11\mu m^2$ area. This design has the latency of 1 clock cycle that can be seen from the waveform shown in figure 9(b).



(a)



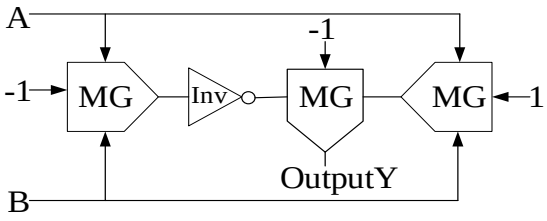
(b)

Figure 9: (a) QCA implementation and (b) simulation result of first proposed binary to gray code converter

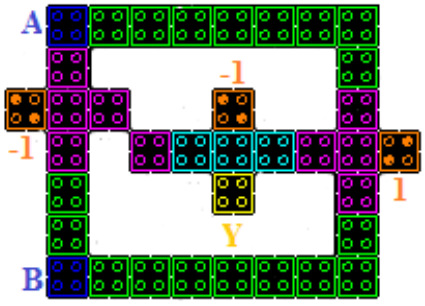
3.4 The second design

The logic used in the second design is given in equation 2 and simplified as:

$$Y = (\overline{A.B}).(A + B) \quad (2)$$
$$Y = (\bar{A} + \bar{B}).(A + B)$$
$$Y = \bar{A}.A + \bar{B}.A + \bar{A}.B + \bar{B}.B$$
$$Y = \bar{A}B + A\bar{B}$$



(a)

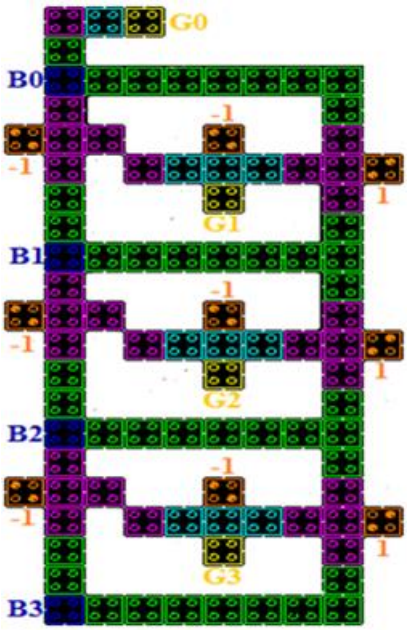


(b)

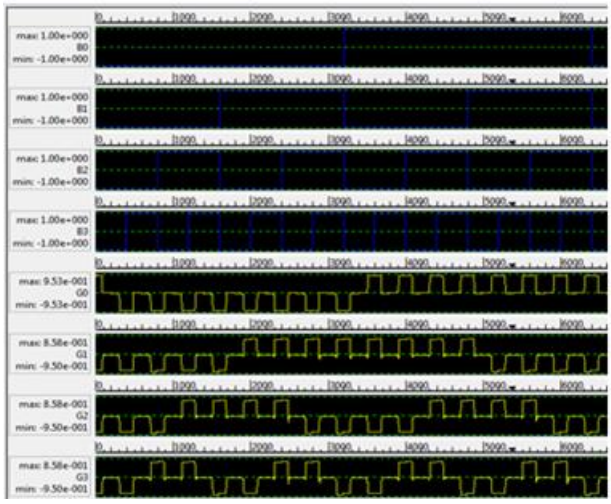
Figure 10: (a) Schematic and (b) layout of second XOR gate

XOR gate shown in figure 10 (b) that is used to develop binary to gray code converter shown in figure 11 (a) is proposed by another author [20]. This XOR requires four majority gates and one inverter with zero crossover. The output of XOR gate in the form of majority logic represented by figure 10(a) can be written as:

$$Y = M(\overline{A.B}, M(A, B, 1), -1)$$



(a)



(b)

Figure 11: (a) QCA implementation and (b) simulation result of second proposed binary to gray code converter

The proposed binary to gray code converter, shown in figure 11(a) has a complexity of 96 cells and 0.09 μm^2 area. This design has the latency of 0.75 clock cycle that can be seen from the waveform shown in figure 11(b).

3.5 The third design

The used gate is based on interaction between QCA cells. Here no majority gate is employed to design the XOR gate.

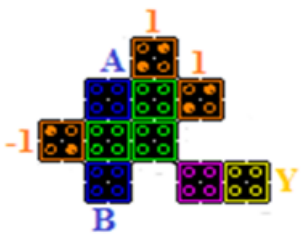
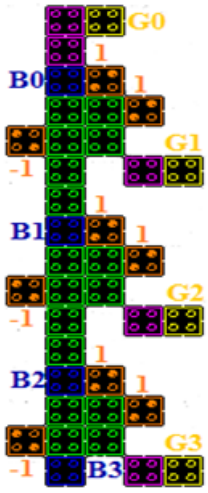
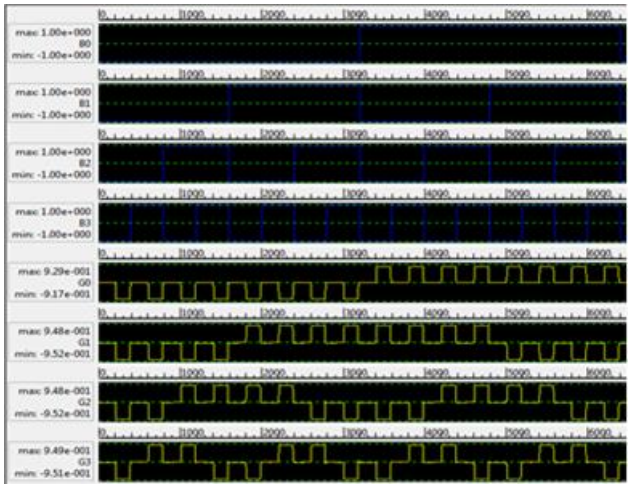


Figure 12: Layout of third XOR gate



(a)



(b)

Figure 13: (a) QCA implementation and (b) simulation result of third proposed binary to gray code converter.

XOR gate shown in figure 12 that is used to develop binary to gray code converter shown in figure 13 (a) is proposed by another author [21]. By using this design, we can reduce the number of cells, area and delay. In this design only 10 cells and 2 clock phases are required.

The proposed binary to gray code converter, shown in fig: 13(a) has a complexity of 38 cells and 0.04 μm^2 area. This design has the latency of 0.5 clock cycle that can be seen from the waveform shown in figure 13(b).

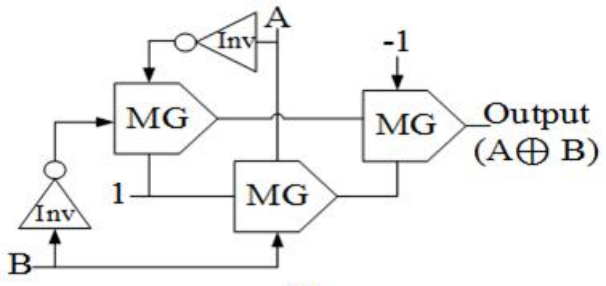
3.6 The fourth design

The logic used by proposed XOR gate in the fourth design is as follows:

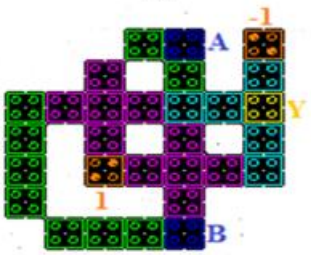
$$Y = (\bar{A} + \bar{B}).(A + B) \quad (3)$$
$$Y = \bar{A}.A + \bar{A}.B + \bar{B}.A + \bar{B}.B$$
$$Y = \bar{A}B + A\bar{B}$$

The proposed XOR requires three majority gates and two inverters with one crossover represented by figure 14(a) and the layout is represented in the figure 14(b). The output of XOR gate in the form of majority logic can be written as:

$$Y = M(M(\bar{A},\bar{B},1),M(A,B,1),,-1)$$

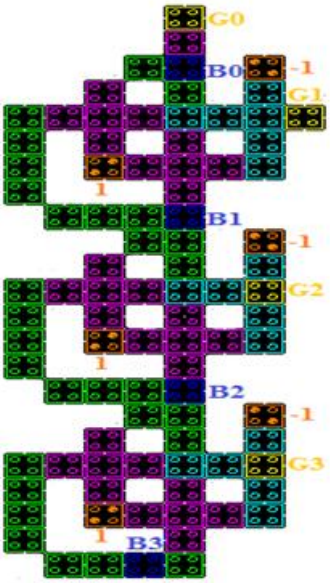


(a)

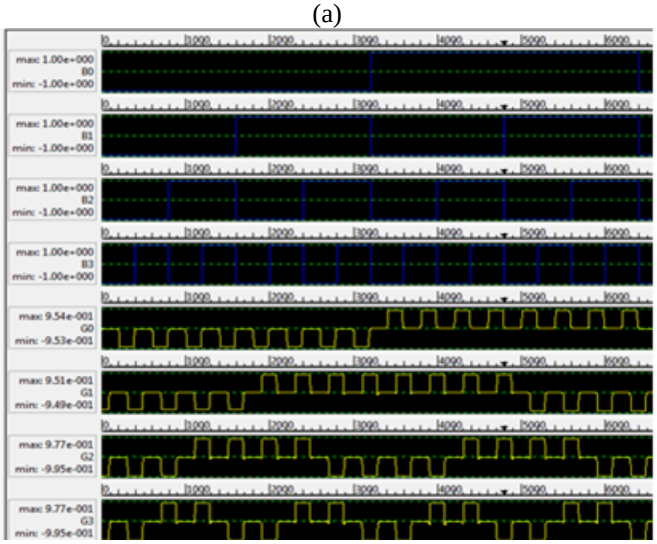


(b)

Figure 14: (a) Schematic and (b) layout of fourth XOR gate



(a)



(b)

Figure 15: (a) QCA implementation and (b) simulation result of fourth proposed binary to gray code converter.

The proposed binary to gray code converter, shown in figure 15(a) has a complexity of 90 cells and 0.07 μm^2area. This design has the latency of 0.75 clock cycle that can be seen from the simulated waveform shown in figure 15(b).

Table 3: Comparison of logic structure

Binary to gray code converter logic structures	Complexity (cell count)	Area (μm^2)	Clock utilized	Latency (clock cycles)
First design (figure 9)	111	0.11	4	1
Second design (figure 11)	96	0.09	3	0.75
Third design (figure 13)	38	0.04	2	0.50
fourth design (figure 15)	90	0.07	3	0.75

Table 3 gives the comparison between all the logic structures of binary to gray code converter on the basis of complexity (cell count), area (μm^2), clock utilized and latency (clock cycle).

4. Conclusion

In this paper, we have proposed four structures of binary to gray code converter using Quantum dot Cellular Automata (QCA) with less number of QCA cells and area compared. These designs are simulated and verified with the table using QCA Designer tool version 2.0.3. These designs can be used to minimize are and complexity. Table3 gives the comparison of proposed designs. It can be seen from the table that the proposed designs have reduced number of QCA cell count and area. In third design number of clock as well as latency is reduced.

References

[1] G.E. Moore, Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff., IEEE Solid-State Circ. Soc. Newslett. 11 (2006) 33–35,http://dx.doi.org/10.1109/NSSC.2006.4785860.
[2] C.S. Lent, P.D. Tougaw, A device architecture for computing with quantum dots, Proc. IEEE 85 (1997) 541–557, http://dx. doi.org/10.1109/5.573740.
[3] C.S. Lent, S., P. Douglas Tougaw, Wolfgang Porod, and Gary H. Bernstein. "Quantum cellular automata." Nanotechnology 4, no. 1 (1993): 49.
[4] Seminario J.M, Derosa P.A, Cordova L.E and Bozard B.H., A molecular device operating at terahertz frequencies, IEEE Transactions on Nanotechnology, 3(1), 2004, 215–218. http://dx.doi.org/ 10.1109/TNANO.2004.824012
[5] Lent, Craig S., P. Douglas Tougaw, Wolfgang Porod, and Gary H. Bernstein. "Quantum cellular automata."In Nanotechnology, vol 4, no. 1 (1993): 49.
[6] Snider, Gregory L., Alexei O. Orlov, I. Amlani, X. Zuo, G. H. Bernstein, C. S. Lent, J. L. Merz, and W. Porod. "Quantum-dot cellular automata." Journal of Vacuum Science & Technology A 17, no. 4 (1999): 1394- 1398.
[7] D. Berzon, T.J. Fountain, A Memory Design in QCA Using the SQUARES Formalism, University College, London, UK, 1998 Tech. Rep.
[8] International Technology Roadmap for Semiconductors (ITRS), [Online]. Available: http://www.itrs.net
[9] C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernstein, Quantum cellular automata, Nanotechnology 4 (1993) 49–57.
[10] K. Walus, T. Dysart, G. Jullien, and R. Budiman, "Qcadesigner: A rapid design and simulation tool for quantum-dot cellular automata," IEEE Trans. Nanotechnology, vol. 3, no. 1, pp. 26–31, Mar. 2004.
[11] Lent, C. S., and Tougaw, P. D., Lines of interacting quantum-dot cells: A binary wire, Journal of Applied Physics, 74(10), 1993, 6227-6233. http://dx.doi.org/10.1063/1.355196
[12] T. Oya, T. Asai, T. Fukui, Y. Amemiya, A majority-logic device using an irreversible single-electron box, IEEE Transactions on Nanotechnology 2 (2003).
[13] S. Amarel, G. Cooke, R.O. Winder, Majority gate network, IEEE Transactions Electronic Computers EC-13 (1964) 4–13.
[14] A.R. Meo, Majority gate networks, IEEE Transactions on Electronic Computers EC-15 (1966) 606–618.
[15]] K. Walus and G. Jullien, "Design tools for an emerging SoC technology: Quantum-dot cellular automata," Proc. IEEE, vol. 94, no. 6, pp. 1225– 1244, Jun. 2006.
[16] M. Abdullah-Al-Shafi, "Synthesis of Peres and R Logic Circuits in Nanoscopic Scale", Communications on Applied Electronics, vol. 4, no. 1, (2016), pp. 20-25.
[17] W. J. Townsend and J. A. Abraham, "Complex Gate Implementations for Quantum Dot Cellular Automata," Proceedings of the 4th IEEE conference of Nanotechnology, Munich, 17-19 August 2004, pp. 625-627.
[18] C. Lent and P. Tougaw, "A device architecture for computing with quantum dots," Proc. IEEE, vol. 85, no. 4, pp. 541–557, Apr. 1997.
[19] K. Hennessy and C. S. Lent, "Clocking of molecular quantum-dot cellular automata," J. Vac. Sci. Technol. B, Microelectron. Process. Phenom., vol. 19, no. 5, pp. 1752–1755, Sep. 2001.
[20] Mohammad Rafiq Beigh, Mohammad Mustafa, Firdous Ahmad, "On the Performances evolution of efficient XOR structures in Quantum Dot Cellular Automata," Journal of scientific research, 4, pp. 147-156, 2013.
[21] Jin-Seong Lee, Young-Won You and Jun-Cheol Jeon "Implementation of QCA XOR Gate Based on Interaction between QCA Cells," in proceedings of the Manila International Conference on Trends in Engineering and Technology (MTET), pp. 23-24, 2017.

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