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Efficient Design of 1- bit Low Power Full Adder using GDI Technique

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Abstract: ***The two important issues in designing of analog circuits are area and power which can be controlled by various parameters. Addition is one of the important mathematical operations which serve as a building block. A low power full adder is the important circuit in the designing of other large circuits. In this paper, three low power full adders are designed using basic gate OR, AND, XOR and XNOR. These gates are designed by using GDI technique. When the number of transistors are decreased then the power consumption and area is reduced.GDI is a new technique for low power digital circuits .This techniques reduce the power consumption, propagation delay and transistor count of digital circuits. The adder cell consists of XOR and XNOR gates. The performance of different adder is compared in respect of various parameters. From results, its cleared that the due to less transistor count the power consumption and area is reduced DSCH and MICROWIND tool is used for the circuit design and simulation of it.***

Keywords: Low power adder, Gate diffusion technique, full adder, VLSI

1. Introduction

In most of the VLSI (very large scale integration) applications like microprocessor, DSP (digital signal processing), image and video processing many types of logic gates are used. AND, OR, XOR, XNOR are important one. They are the building blocks for other operations. These gates are used to perform different operations like addition, subtraction, multiplication and many others.

The most important operation is adder which is used in VLSI applications. It behaves as a fundamental block for many other operations like division, subtraction, multiplication etc. In digital systems, adders effect overall system performance. Therefore to enhance its performance had become an important aim [1]-[3].

According to MOORE'S Law, the number of transistors per square inch on integrated circuits become double every year. As the density of circuit is increasing so power dissipation vital parameter in circuit designing. As the technology is advancing day by day, the need for low power dissipation and high speed had attracted many researchers [4], [5].

The incredible growth in the electronics gadgets like mobile, laptop etc had allowed researchers to do work in low power microelectronics. The reason for working on low power applications is that the technology is increasing but the battery efficiency is not increasing in that order in which technology is increasing. Therefore low power consuming device is in more demand [6].

As the technology advances, it allows fulfillment of hardware of different applications such as microprocessor, DSP etc. Due to increasing demand and trendiness of electronic devices, the researchers have to focus on chip area, higher speed, reliability, low power consumption.

The standards for design of full adder are multifold [7]. The number of transistors decides the complexity of ALU (arithmetic logic unit), multiplier etc. The two other standards which are important in designing of full adder are Power consumption and speed. Full adder is the fundamental block for designing other large adders like ripple carry adders, carry select adder, carry save adder. There are different logic styles which can be used to design full adder. The parameters in which performance of full adder can be seen are power dissipation and delay. To increase the performance of full adder, delay should be less.

The digital circuits, performance can be improved by choosing correct logic styles. It also depends on the number of transistor used. The full adder can be designed by using different design styles which are Conventional CMOS, Pass transistor logic, Transmission full adder.

The conventional CMOS [8]-[10] full adder is made of NMOS pull down and PMOS pull up transistors. The designs made by it are very simple but transistor count is more. It e complementary pass transistor logic [8] - [10] is cross coupled PMOS transistors.

The demerit of this technology, it consumes more power because of number of inverters. Transmission function full adder (TFA) [10]-[12] and Transmission gate full adder [10], [12] design are low power consuming.
The demerit of this style is that it had more number of transistors.

Another design style to design full adder is GDI (Gate Diffusion Input) technique. It is an alternative of CMOS logic. It is a style in which less number of transistors required therefore it consumes less power. It consists of pull up and pull down transistor.

In this paper, design of AND, OR AND, XOR, XNOR gates are made with the help of GDI logic. The full adders are

designed by using GDI XNOR and GDI XOR. The performance of proposed full adders is compared in delay, power consumption and number of transistors. There are 2 methods by which full adders can be designed. The two designing methods are using two XOR/XNOR & MUX or two MUX & XOR/XNOR. Due to different designing methods all the parameters gets changed.

2. GDI Technique

The basic GDI cell is shown in fig.1. It looks like CMOS inverter but the source and drain input of both the transistors are different [13] - [15].

In CMOS inverter, the source and drain inputs are always tied to V_{DD} and GND respectively. While in GDI the diffusion terminal act as external input. GDI cell consist of three inputs – P(input to the source/drain of PMOS) and N (input to the source /drain of NMOS) and G(common gate input of NMOS and PMOS).The bulk of both NMOS and PMOS are connected to with N or P respectively which is shown in fig 1.

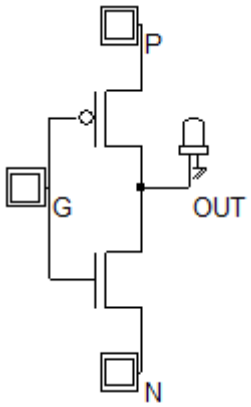

Figure 1: Basic GDI cell

It helps to realize the various Boolean functions such as AND, OR, MUX, INVERTER, F1, F2 as shown in Table.1 Table 1 shows the implementation of different logic function using GDI technique. When these implementations are done with the help of CMOS then transistor count is increased and due to which the power consumption also increases while with the help of GDI, the transistor count is less and power consumption is also low.

Table 1: Different logic function realization using GDI cell

N	*P*	*G*	*Output*	*Function*
0	B	A	A'B	F1
B	1	A	A' + B	F2
1	B	A	A + B	OR
B	0	A	A.B	AND
C	B	A	A'B +AC	MUX
0	1	A	A'	NOT
B'	B	A	A'B+AB'	XOR
B	B'	A	AB+A'B'	XNOR

Table 2 shows the number of transistors required to implement the various functions by CMOS logic and GDI technique.

Table 2: Comparison of transistor count between CMOS & GDI

Function	CMOS (no. of transistors)	GDI (no. of transistors)
F1	6	2
F2	6	2
OR	6	2
AND	6	2
NOT	2	2
MUX	12	2
XOR	4	16

3. Logic Circuit Using GDI Cell

For designing any large circuit using GDI the knowledge of basic circuits is needed. Many gates have been made using GDI cell. These gates are used to form a large circuit. Many digital applications need low power consumption, for this the basic need is that gates used in designing should not consume much power. The GDI based basic gates are as below [16], [17] –

3.1 AND gate

To design the AND gate with GDI cell, PMOS and NMOS are taken. Input A is applied at the gate effects the area and power consumption. The terminal Input B is applied at N terminal and terminal P is grounded which can be seen in fig 2.

Output = A.B

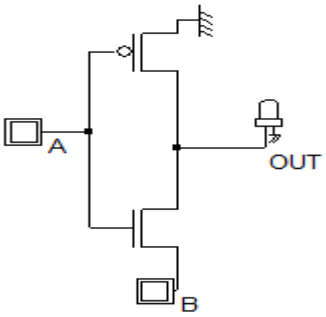

Figure 2: AND gate using GDI cell

3.2 OR gate

To design the OR gate with GDI cell, PMOS and NMOS is taken. Input A is applied at the gate terminal. Input B is applied at P terminal and terminal N is grounded which can be seen in fig 3.

Output = A+B

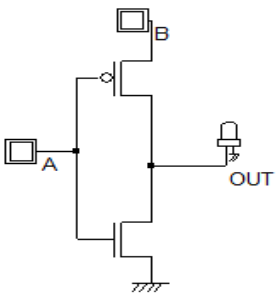

Figure 3: OR gate using GDI cell

3.3 XOR gate

To design XOR gate with GDI cell, two GDI cells are cascaded in parallel and input A is applied to gate of first GDI cell and also to source of second GDI cell. Input B is applied to the second GDI cell. Output of the first GDI cell is applied to the drain of second GDI cell. The drain of first GDI cell is grounded and V_{dd} is connected to the source. The connections are shown in fig 4. The output of XOR gate is given by second cell. The output of gate is shown below.

Output = A XOR B
$= \bar{A}B + A\bar{B}$

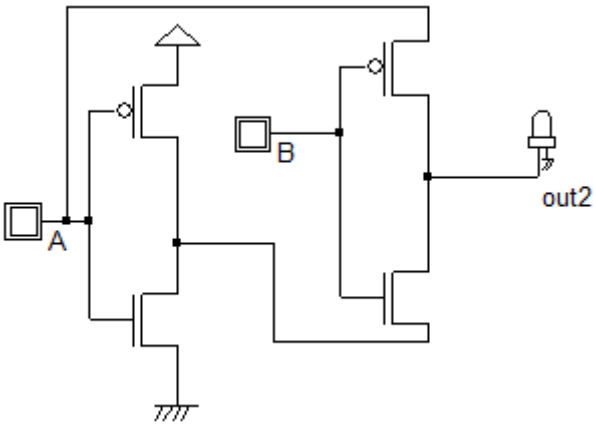

Figure 4: XOR gate using GDI cell.

3.4 NOT gate

To design the OR gate with GDI cell, PMOS and NMOS is taken. It is similar to CMOS inverter.

Output = $\bar{A}$

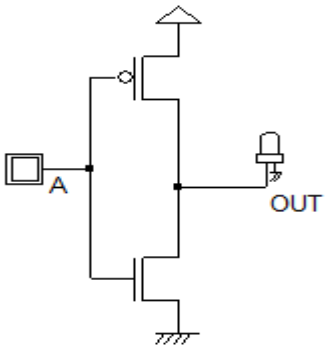

Figure 5 : NOT gate

3.5 XNOR gate

To design XNOR gate using GDI cell, two GDI cell are cascaded parallel to each other. Input A is applied to the gate of first cell and it is connected to the drain of the second cell. The drain of first GDI cell is grounded and source is connected to the $V_{dd.}$ The source of second cell is connected to the output of the first cell. The connections are shown in fig 6. The output of gate is given by second cell. The output of gate is given below.

Output = A XNOR B
$= \bar{A}\,\bar{B} + AB$

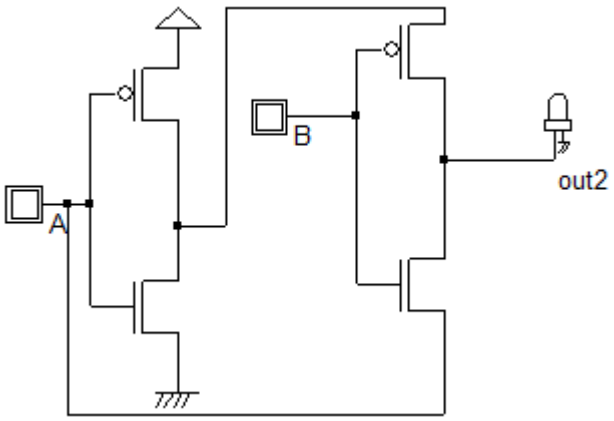

Figure 6: XNOR gate using GDI cell

4. Full Adder Design Using GDI XOR/XNOR Cell

There are various full adders which can be designed using XOR .The number of transistors decreased to get low power consumption. The logic functions used in full adder [18] can be given by these equations-

$$SUM = A \textbf{ XOR } B \textbf{ XOR } C \quad (1)$$
$$C_{out} = (A \textbf{ XOR } B)\, C + AB \quad (2)$$

From above equations, it is clear that for designing of full adder, the basic gates needed are AND, OR, XOR, XNOR .The basic gates can be achieved by using two transistor and one inverter and their diagram are shown above. The truth table of full adder is shown in table 3. The circuit verifies at all the inputs.

Table 3: Truth table of full adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A full adder can be constructed from two half adders by connecting *A* and *B* to the input of one half adder, connecting the sum from that to an input to the second adder, connecting *C* to the other input and OR the two carry outputs. The critical path of a full adder runs through both XOR-gates and ends at the sum bit. The critical path of a carry runs through 1 XOR-gate in adder and through 2 gates (AND and OR) in carry-block.

4.1 Design 1

To implement the function of full adder described in eq. 1 & 2 the full adder can be designed using two XOR/XNOR & MUX. The design is shown in fig 7. Fig 7 (a) shows the full adder using XOR gate. The designing of full adder also change all the parameters. The best performance can't be

decided by only design. It can be decide by simulating the circuit

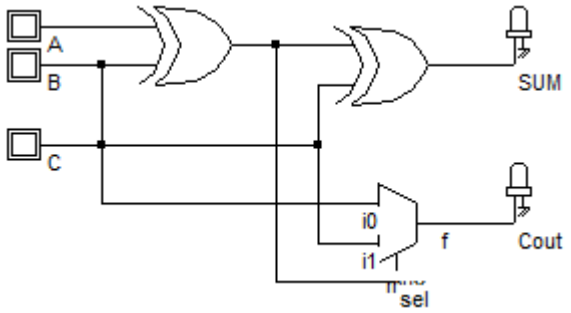

Figure 7(a): XOR based full adder

Fig 7 (b) shows the full adder using XNOR gate .All the designing is same as of the XOR gate. In this two XNOR and MUX is taken to design the full adder. There are three inputs A, B, C and two output sum and carry. The carry will be taken out from MUX and Sum will be from XNOR.

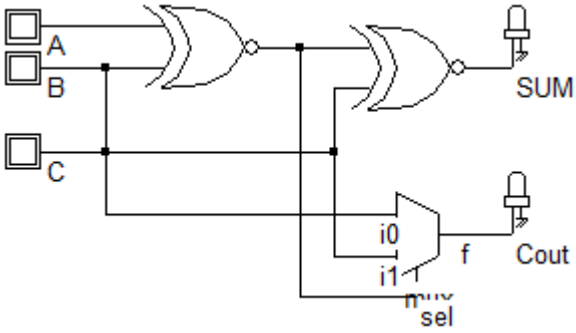

Figure 7(b): XNOR based full adder

4.1.1 10T Full adder

The full adder can be designed using both XOR/ XNOR. Both the gates increase the performance of the full adder. XOR/XNOR can be implemented using four transistors. MUX can be implemented using two transistors. The full adder is designed by using design 1. The two XOR/XNOR cell are cascaded. For carry one MUX is connected to it. The output of first cell is given to second cell and MUX. The output of second cell is sum and output of MUX is carry which is shown in fig 8.

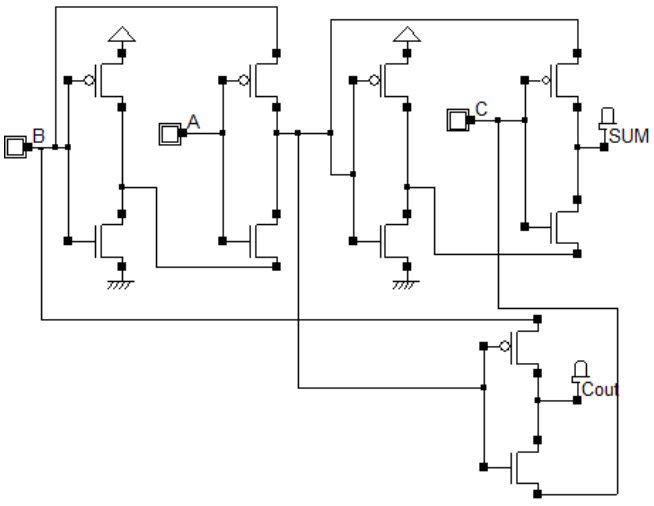

Figure 8: 10T full adder using XOR GDI cell

The output of first XOR / XNOR cell is given to next XOR/XNOR cell. . The output of second cell is generating SUM. C_{out} can be calculated by another cell. The 10T full adder designed by using XNOR is shown in fig 9.

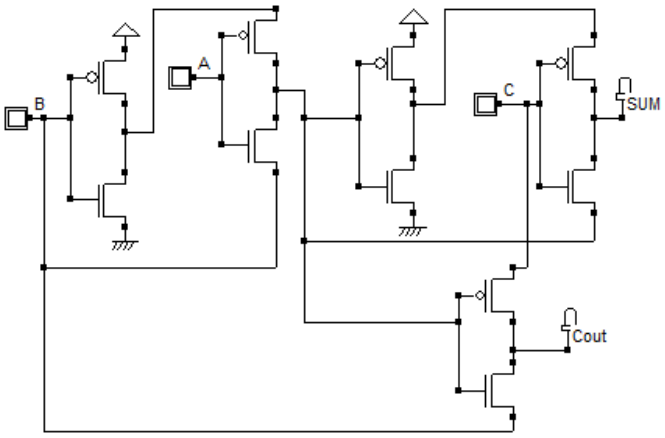

Figure 9: 10T full adder using XNOR GDI cell

The layout of 10T full adder is shown in fig 10. The number of transistors is reduced using GDI technique which directly decreases the chip area. As the chip area decreases the complexity of designing also decreases. It will also affect the power consumption.

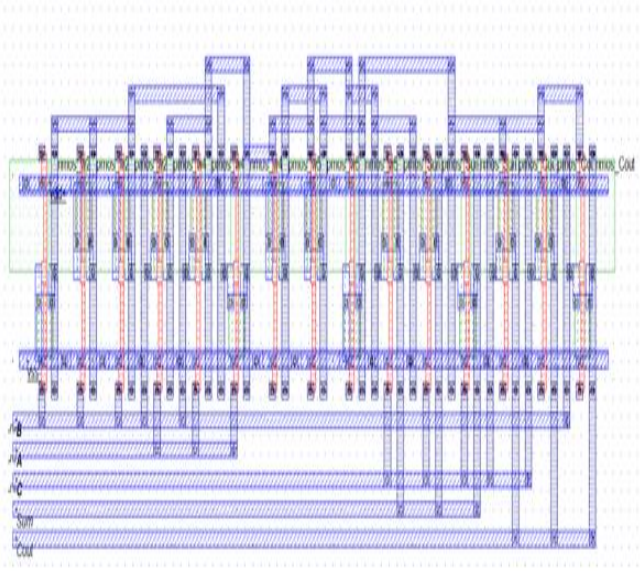

Figure 10: Layout of 10T full adder

4.1.2 9T Full adder –For designing of 9T full adder, only 9 transistors are needed. As the transistor cont become less so the power consumption is also low. Here, in first XOR cell only three transistors are used. There are two Pmos and one Nmos while in second cell there are four transistors. This is the proposed circuit which is shown in fig 11.

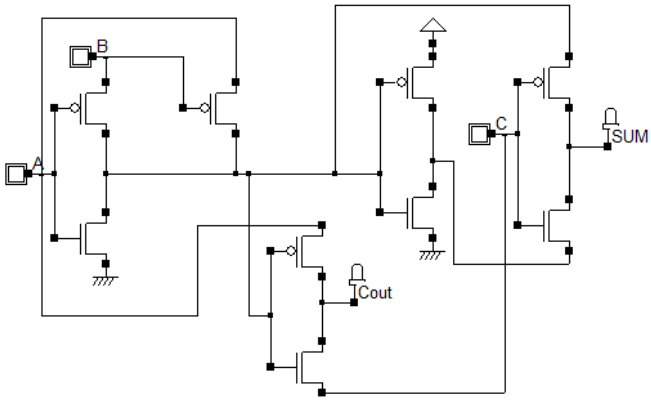

Figure 11: 9T full adder using XOR GDI cell

In XNOR, the three transistor XNOR is made by using two Nmos and one Pmos and second cell consists of four transistors. The layout of 9T full adder is shown in fig 12. The area of this adder is less than in comparison to other.

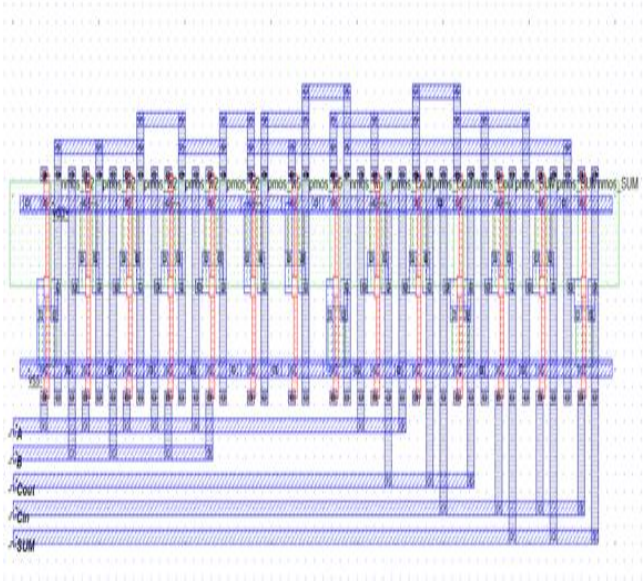

Figure 12: Layout of 9T full adder

4.2. Design 2

To implement the function of full adder described in eq. 1 & 2 the full adder can be designed using XOR/XNOR & two MUX. The design is shown in figure 13. Fig 13 (a) shows the full adder using XOR gate .Fig 13 (b) shows the full adder using XNOR gate.

The design 2 is only a redesigning of full adder. The designing of full adder also change all the parameters. The best performance can't be decided by only design. It can be decide by simulating the circuit.

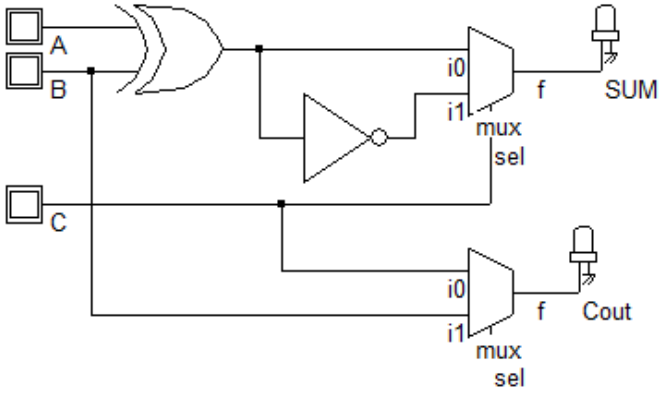

Figure 13(a): XOR full adder

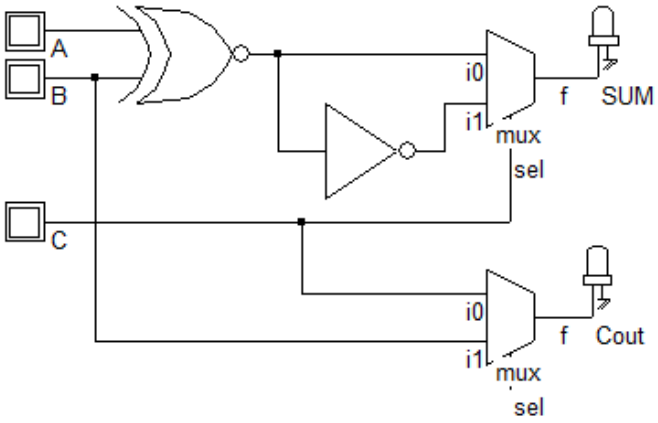

Figure 13(b): XNOR full adder

4.2.110T Full adder

In this the full adder is made by design 2. In design 2, the transistors count is same. There is XOR, NOT & two MUX which is shown in fig 14.

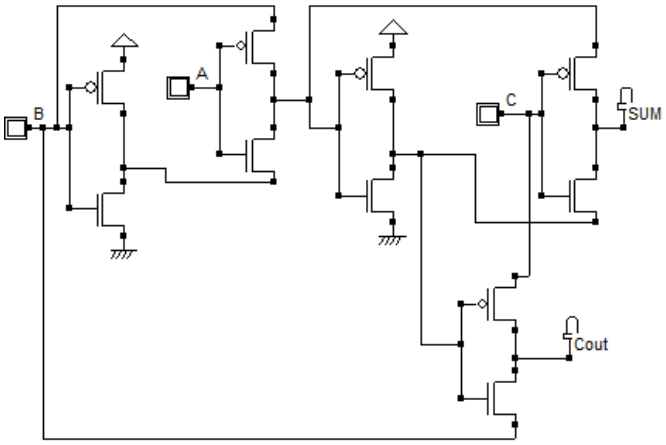

Figure 14: 10T full adder using XOR GDI cell

The output of first XOR / XNOR cell is given to next XOR/XNOR cell. The output of second cell is generating SUM. C_{out} can be calculated by another cell which can be seen in fig 14.The XNOR full adder can also be designed by using design 2 which is shown in fig 15..

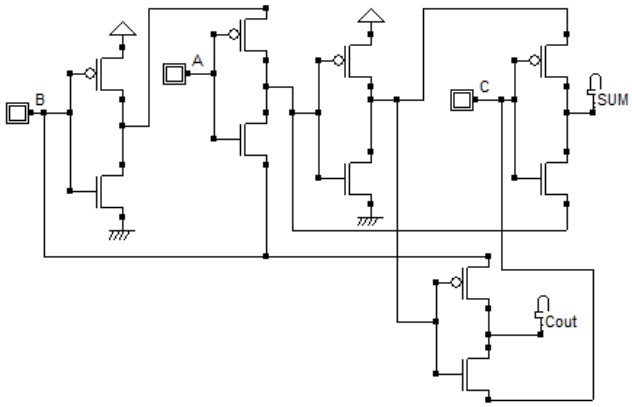

Figure 15: 10T full adder using XNOR GDI cell

4.2.2 9T Full adder

The 9T full adder is made by design 2. In design 2, the transistors count is same as above design. There is XOR, NOT & two MUX. This is also proposed design as shown in fig 16.

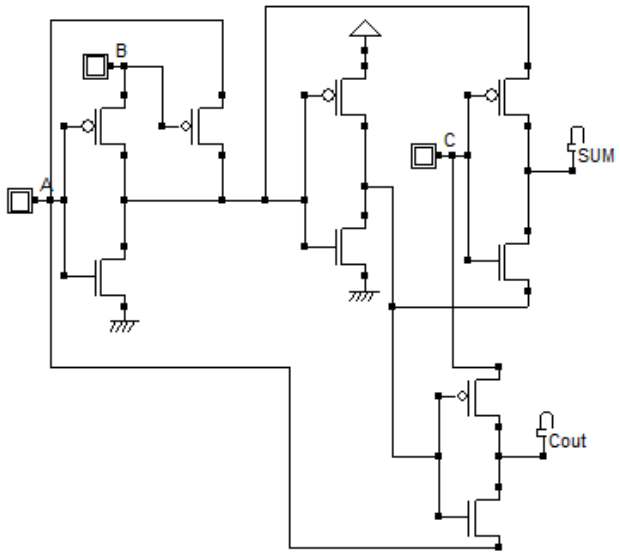

Figure 16: 9T full adder using XOR GDI cell

5. Simulation Result & Comparison

In this paper, 9T full adder is proposed using design 1 and design 2. The comparison is made between them. The full Adders designed by using different basic gates made with the help of GDI cell are discussed in this paper. Their performance is compared in respect of power consumption, delay and number of transistors. The simulation result of full adder is shown in fig 17.

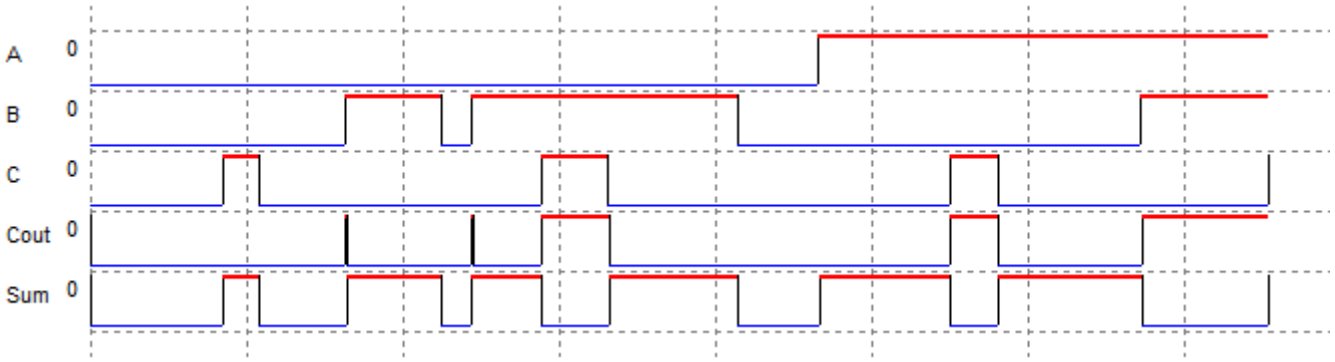

Figure 17: Waveform of full adder

The conventional CMOS design consumes more power due to more number of transistors. The other design style like CPL logic and hybrid adders also contains more number of transistors. The adder designed by GDI technique contains less number of transistors. So power consumed is also low. The layout area is also less than other logics. The performance parameters for all the full adders are power consumption, delay, no. of transistor etc. are discussed in sub sections.

5.1 Delay

The maximum delay is counted as a worst delay. The delay is measured by relating the time taken from the input voltage to the output voltage for each transition. The delay of full adder can be seen in table. The minimum delay is of 9T full adder designed by using design 1 in comparison to others.

5.2 Power Consumption

The Power consumed by the full adders is computed through simulation. The proposed full adder will consume less power in comparison to 10T. The power consumption decreases as the number of transistors decreases. The power consumption is less of 9T full adder designed by using design.

5.3 Number of transistor

The transistor count is also the important issue. As the number of transistor count increases, the power also increases. So the full adder with less number of transistors is best.

Table 4: Comparison of full adders using GDI cell

Full Adder Using GDI Cell	Design 1			Design 2			Transistor Count
	Power (µw)	Delay (ns)	PDP (fj)	Power (µw)	Delay (ns)	PDP (fj)	
10T (XNOR)	31.86	0.300	9.55	32.50	0.350	11.375	10
10T(XOR)	29.18	0.118	3.44	20.04	0.175	3.507	10
9T(XOR)	13.13	0.050	0.65	17.94	0.075	1.34	9

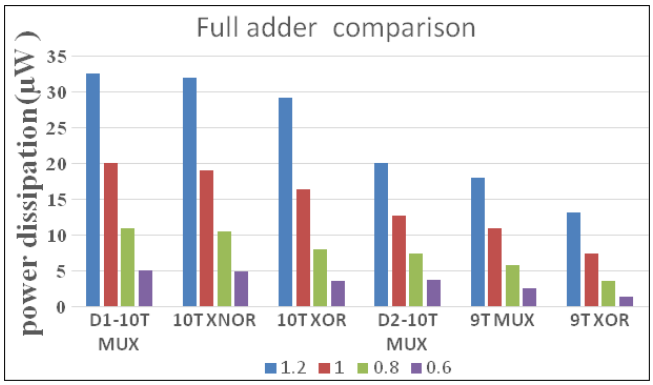

Figure 18: Comparison of Power Dissipation

6. Conclusion

In this paper, a new approach is proposed to design a low power full adder using GDI cell. The advantages of Gate Diffusion technique is less number of transistor count and in-cell swing restoration under some operating condition. The GDI cell also allows implementation of various logic functions using two transistors. In this 1 bit full adder is designed by using GDI cell with different designs. Due to less number of transistor count, the low power is used. The performance comparison of 9T & 10T full adder is done. The 9T low power full adder designed by using design 1 has low power consumption, low delay, low power delay product and less number of transistors as compared to other full adders. The result shows that 9T full adder is the best among all the full adders in every aspect. The performance analysis of full adder is done at 120 nm CMOS technology and at 1.2V supply. The analysis and simulation is done by using DSCH and MICROWIND 3.1 simulator.

This designing approach can be used for designing different circuits with low power consumption and less surface.

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Author Profile

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