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Scan Insertion on Multi Clock Design in Modern SOC's

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Abstract: ***These instructions provide you guidelines for preparing papers for International Journal of Science & Research (IJSR). Use this document as a template and as an instruction set. Please submit your manuscript by IJSR Online Submission Module. VLSI technology is an emerging field in the current technological due to its advancements in fields of systems architecture, design for testability (DFT) techniques for testing modern digital circuits. DFT techniques are required in order to improve the quality and reduce the test cost of the digital circuit, while at the same time simplifying the test, debug and diagnose tasks. The existing Ad Hoc Approach has the most compact design but takes longer computation time and low-observability. The time critical applications use Structured Approach, Scan design the most widely used structured DFT methodology, attempts to improve testability of a circuit by improving the controllability and observability of storage elements in a sequential design. In this paper different scan architectures are analyzed to study the operation of Full-Scan design. The proposed design includes Full-Scan design using Muxed-D scan cell. Scan control logic is spread across the blocks, based on the scan architecture. Scan enable, scan clocks, length of scan chains, number of EDT channels are required constraints for scan insertion. The Muxed-D scan cell is composed of a D flip-flop and a multiplexer. The designs are synthesized using Synopsys design compiler Software.***

Keywords: Design for Testability, Scan Design, Data Input, Scan Input, Scan Enable.

1. Introduction

VLSI testing includes test generation and test application. Test generation is used to produce test patterns for efficient testing [1]. Test application is the process of applying these test patterns to the circuit under test (CUT) and analyzing the output responses. Test application is done by either automatic test equipment (ATE) or test facilities on the chip itself. Test engineers usually construct test vectors after the design is completed. This requires a substantial amount of time and effort that avoid if testing is considered early in the design flow to make the design more testable. As a result, integration of design and test, referred to as design for testability (DFT). To test circuits, we need to control and observe logic values of internal lines. Unfortunately, some nodes in sequential circuits can be very difficult to control and observe; for example, activity on the most significant bit of an nbit counter can only be observed after 2^{n-1} clock cycles.

Testability measures of controllability and observability were first defined to help find those parts of a digital circuit that will be most difficult to test and to assist in test pattern generation for fault detection.

Testing is usually performed by applying a set of test stimuli to the inputs of the circuit under test and analyzing the output responses, as illustrated in Figure 1. Circuits that produce the correct output responses for all input stimuli are considered to be fault-free. Those circuits that fail to produce a correct response during the test are assumed to be faulty. Testing is performed at various stages in the lifecycle of a VLSI device, including during the VLSI development process, the electronic system manufacturing process, and, in some cases, system-level operation.

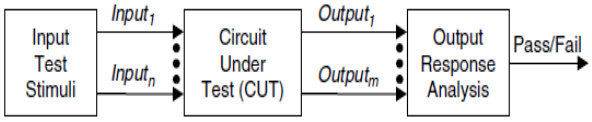

Figure 1: Basic Testing Approach

2. Existing Techniques for DFT

In Electronics, The first challenge facing DFT engineers was to find simpler ways of exercising all internal states of a design and reaching the target fault coverage goal.

2.1 Ad Hoc Approach

Ad hoc testability enhancement methods were proposed and used in the 1970s and 1980s to exercise all internal states of a design and reaching the target fault coverage goal [2].

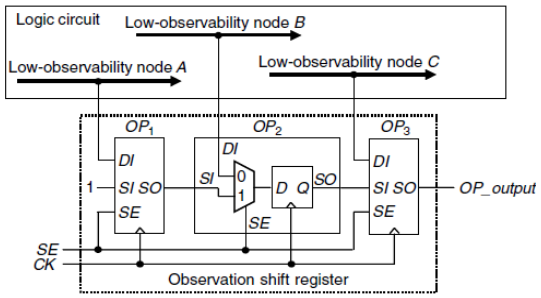

Figure 2: Ad Hoc Approach Observation Point Insertion

Initially, many ad hoc techniques were proposed for testability. These techniques rely on making local modifications to a circuit so that was considered to result in testability improvement. While ad hoc DFT techniques result

in some tangible testability improvement, their effects are local and not systematic.

Furthermore, these techniques are not done according to a systematic or established procedure, in sense that they have to be repeatedly applied on new designs, often with unpredictable results. Due to the ad hoc nature, it is also difficult to predict how long it would take to implement the DFT features.

2.2 Structured Approach

The structured approach for testability was introduced to allow DFT engineers to follow a systematic or established process for improving the testability of a design [3]. A structured DFT technique can be easily incorporated and budgeted for as part of the design flow and can yield the desired results. Furthermore, structured DFT techniques are much easier to automate. Scan design, is accomplished by converting the sequential design into a scan design with three modes of operation: normal mode, shift mode, and capture mode. Circuit operations with associated clock cycles conducted in these three modes are referred to as normal operation, shift operation, and capture operation, respectively. Scan design is accomplished by first converting selected storage elements in the design into scan cells and then stitching them together to form one or more shift registers, called scan chains.

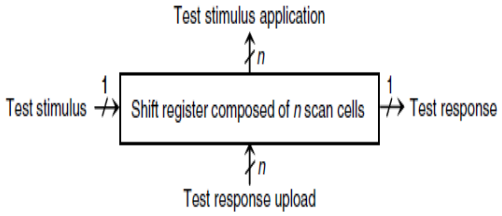

Figure 3: Scan Design Concept

In the scan design illustrated in Figure 3, the n storage elements are now configured as a shift register in shift mode. Any test stimulus and test response can now be shifted into and out of the n scan cells in n clock cycles, respectively.

2.3 Muxed-D Scan Cell

A D flip-flop is an edge-triggered D storage element, and a D latch is a level-sensitive D storage element. The most widely used scan cell replacement for the D flip-flop is the muxed-D scan cell [4]. Figure 4 shows an edge triggered muxed-D scan cell design. This scan cell consists of D flip-flop and a multiplexer. The multiplexer consists of a scan enable (SE) input to select between the data input (DI) and the scan input (SI).

Advantages of Muxed-D Scan Cell

- Muxed-D scan cells are compatibility to modern designs using single-clock D flip-flops
- Comprehensive support provided by existing design automation tools.

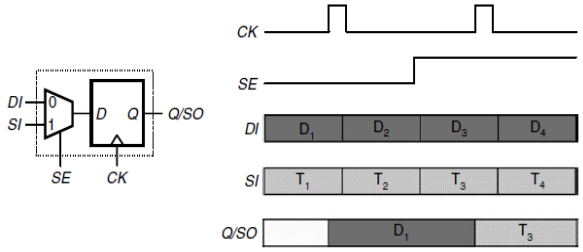

Figure 4: Edge-triggered muxed-D scan cell Design and Operation

Disadvantages of Muxed-D Scan Cell

- Each muxed-D scan cell adds a multiplexer delay to the functional path.

2.4 Clocked-Scan Cell

Clocked-scan cell has a data input DI and a scan input SI; but, in the clocked-scan cell, input selection is done by using two independent clocks [5], data clock DCK and shift clock SCK, as shown in Figure 5

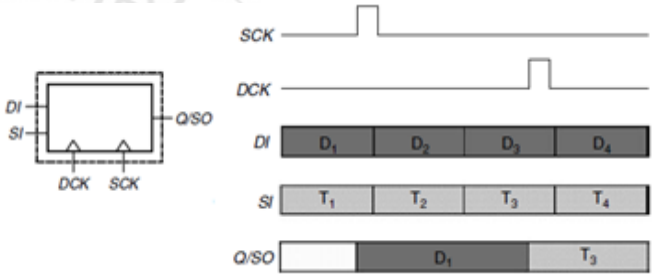

Figure 5: Clocked-scan Cell Design and Operation

Advantages of Clocked-Scan Cell

- Clocked scan cell has no performance degradation on the data input.

Disadvantages of Clocked-Scan Cell

- Clocked-Scan cell requires additional shift clock routing.

2.5 LSSD Scan Cell

An LSSD scan cell is used for level-sensitive, latch-based designs [6]. Figure 6 shows a polarity-hold shift register latch (SRL) that can be used as an LSSD scan cell. This scan cell contains two latches, a master D latch L_1 and a slave D latch L_2. Clocks C, A, and B are used to select between the data input D and the scan input I to drive $+L_1$ and $+L_2$.

Advantages of LSSD Scan Cell

- LSSD scan cell allows us to insert scan into a latch-based design.
- LSSD are guaranteed to be race-free.

Disadvantages of LSSD Scan Cell

- LSSD Scan cell requires routing for the additional clocks, which increases routing complexity.

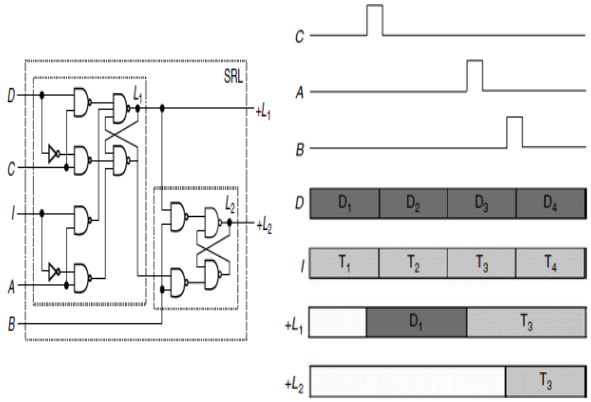

Figure 6: Polarity-hold SRL Design and Operation

3. Different Methods / Approaches for Scan Insertion

3.1 Full Scan Design

In full-scan design, all storage elements are replaced with scan cells, which are then configured as one or more shift registers (also called *scan chains*) during the operation. As a result, all inputs to the combinational logic, including those driven by scan cells, can be controlled and all outputs from the combinational logic, including those driving scan cells, can be observed. The main advantage of this design is that it converts the difficult problem of sequential ATPG into the simpler problem of combinational ATPG [7].

Full Scan Architecture is again divided into three types
1) Muxed-D Full-Scan Design
2) Clocked Full-Scan Design
3) LSSD Full-Scan Design

1. Muxed-D Full-Scan Design:

In this all the flip-flops are replaced with muxed-D scan cell. The data input DI of each scan cell is connected to the output of the combinational logic same as in the original circuit. To form a scan chain, the scan input SI of SFF2 is connected to the output Q of the previous scan cell SFF1 and SI of SFF3 is similarly connected to Q of SFF2. In addition, the scan input SI of the first scan cell SFF_1 is connected to the primary input SI, and the output Q of the last scan cell SFF_3 is connected to the primary output SO. Hence, in shift mode, SE is set to 1, and the scan cells operate as a single scan chain, which allows us to shift in any combination of logic values into the scan cells. In capture mode, SE is set to 0.

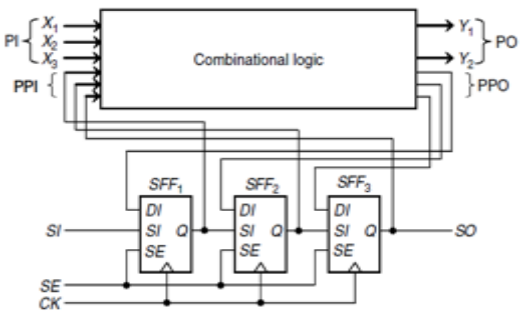

Figure 7: Muxed-D Full Scan Circuit

In general, combinational logic in a full-scan architecture has two types of inputs: primary inputs (PIs) and pseudo primary inputs (PPIs). Primary inputs are the external inputs to the circuit, and pseudo primary inputs are the outputs to the scan cell. Both PIs and PPIs can be set to any required logic values. The only difference is that PIs are set directly in parallel from the external inputs, and PPIs are set serially through scan chain inputs. Similarly, the combinational logic in a full-scan circuit has two types of outputs: primary outputs (POs) and pseudo primary outputs (PPOs). Primary outputs are the external outputs of the circuit, and pseudo primary outputs are the inputs to the scan cell. Both POs and PPOs can be observed. The only difference is that POs are observed directly in parallel from the external outputs, while PPOs are observed serially through scan chain outputs.

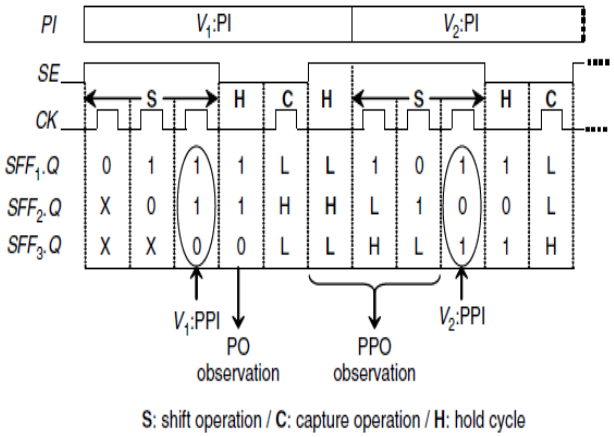

Figure 8: Muxed-D Full Scan Circuit Test Operation

2. Clocked Full-Scan Design:

In this all the flip-flops are replaced with clocked-scan cell.

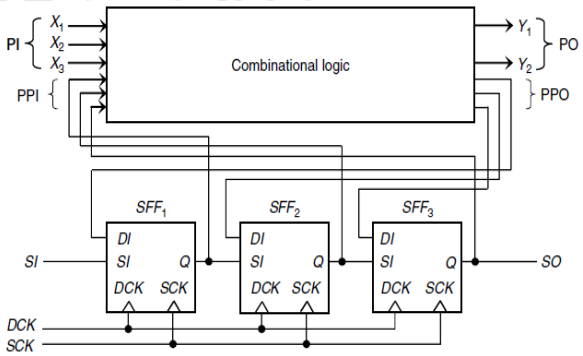

Figure 9: Clocked Full Scan Circuit

In the clocked full-scan circuit shown in Figure 9, these two operations are distinguished by properly applying the two independent clocks *SCK* and *DCK* during shift mode and capture mode, respectively.

3. LSSD Full-Scan Design:

In this all the flip-flops are replaced with clocked-scan cell. It is possible to implement LSSD full-scan designs [8], based on the polarity-hold SRL design, using either a single-latch design or a double latch design. A set of clock primary inputs must exist from which the clock ports of all SRLs are

controlled either through a single clock tree or through logic that is gated by SRLs and/or non-clock primary inputs.

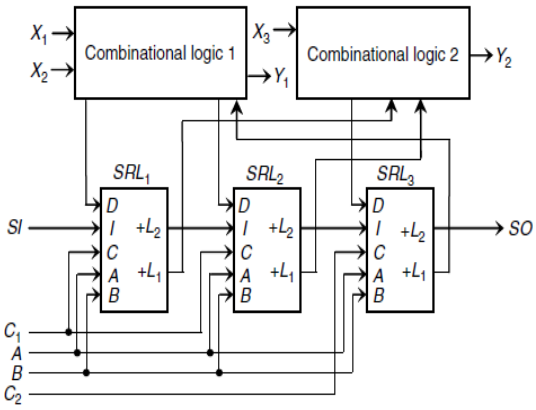

Figure 10: LSSD Single-Latch Full-Scan Design

3.2 Partial-Scan Design

In partial-scan design only requires that a subset of storage elements be replaced with scan cells and connected into scan chains.

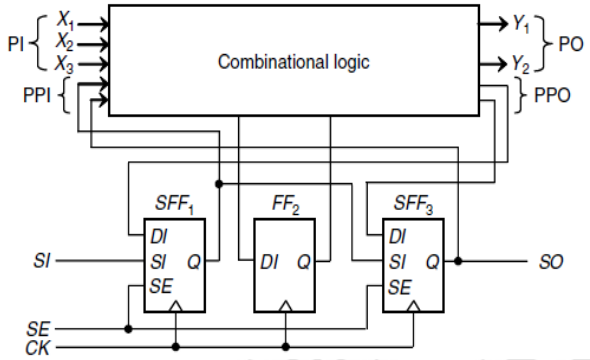

Figure 11: Partial-Scan Design

Storage elements on the data path portion cannot afford too much delay increase, especially when replaced with muxed-D scan cells, they are left out of the scan cell replacement process [9]. On the other hand, storage elements in the control portion may be replaced with scan cells. This approach makes it possible to improve fault coverage while limiting the performance degradation due to scan design.

3.3 Random-Access Scan Design

Traditional RAS design is illustrated in Figure 12. All scan cells are arranged into a two-dimensional array, where they can be accessed individually for reading and writing in any order. This full-random access capability is obtained by decoding address with a row (X) decoder and a column (Y) decoder [10]. A [log$_2$n]-bit address shift register, where n is the total number of scan cells, is used to identify which scan cell to access.

The RAS design significantly reduces test power dissipation and simplifies the process of performing delay tests. Its major disadvantage, is high overhead in scan cell design and routing required to set up the addressing mechanism.

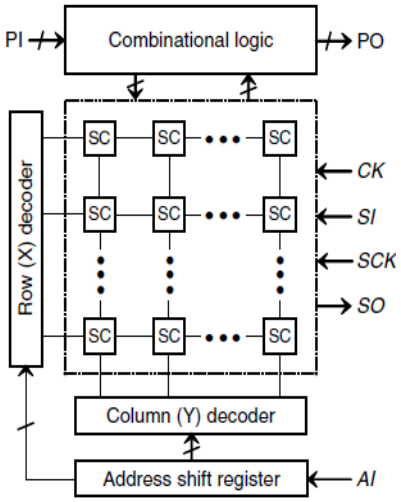

Figure 12: Random-Access Scan Design

4. Simulation Results and Comparison

Scan insertion has been done by using Synopsys design compiler Software. Area and cell count for Pre – Scan and Post – Scan has been calculated for Muxed-D Full-Scan Design. Table. I shows the comparison of area for scan insertion.

Table 1: Comparison of Cell count

Cell Count	*Pre-Scan*	*Post-Scan*
Combinational Cell Count	474495	477948
Sequential Cell Count	110424	111027

The result analysis shows that Combinational cell count increased in post – scan because of extra combinational logic introduced beacause of EDT and due to the addition of OR gate and marked buffers. Sequential cell count count increased because of EDT and addition of observe only flops.

Table 2: Comparison of Area

Cell Count	*Pre-Scan*	*Post-Scan*
Combinational Cell Count	474495	477948
Sequential Cell Count	110424	111027

The result analysis shows that the area has increased due to the conversion of D-flip-flops to scan flops. Area has increased because of combinational cells and sequential cells introduced in the design due to EDT. This increase can be ignored. The graphical representation of comparison of area for pre – scan and post – scan is shown in Fig.14.

The chart explains the comparison of power in pre – scan and post – scan for switching power, internal power and dynamic power.

Switching power has increased due to the fact that the scan chain acts as a shift register where the scan input values and clock are continuously changing. But the increase is very less and it is due to change in only clock valve and the scan input values are not changed too frequently.

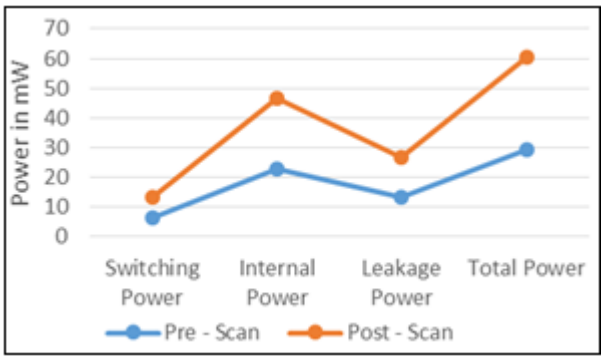

Figure 13: Comparisons of power in Pre-Scan and post-Scan

We can also observe an increase in internal power because of the increase in cell count. An increase in both switching power and internal power which accounts to increase in total power.

QOR Report

Table 3: Comparison of QOR

Timing Path Group 'FCLK'	Pre - Scan	Pre - Scan
Levels of Logic:	42.00	5.00
Critical Path Length:	200.96	200.96
Critical Path Slack:	44.16	44.16
Critical Path Clk Period:	500.00	500.00
Total Negative Slack:	0.00	0.00
No. of Violating Paths:	0.00	0.00
Worst Hold Violation:	0.00	0.00
Total Hold Violation:	0.00	0.00
No. of Hold Violations:	4825.00	0.00
Timing Path Group 'TO_GCLK'		
Levels of Logic:	38.00	25.00
Critical Path Length:	382.94	382.94
Critical Path Slack:	75.32	75.32
Critical Path Clk Period:	500.00	500.00
Total Negative Slack:	0.00	0.00
No. of Violating Paths:	0.00	0.00
Worst Hold Violation:	-4.95	-4.95
Total Hold Violation:	-34.46	-34.46
No. of Hold Violations:	3334.00	7.00

Scan summary Report

Table 4: Comparison of Scan Summary

Parameters	Pre - Scan	Post - Scan
Total number of Scan Cells	64187	64187
Total number of Non Scan Cells	30698	30698
Scan Coverage Percentage	67.647 %	97.348 %
Total Number of dedicated wrappers	0	0
Total Number of shared wrappers	18170	18170
Total number of ports not wrapped	504	504
Total number of Short Chains in Extest Compression mode	0	0
Max Short Chain Length in Extest Compression mode	0	0
Total number of Scan Channels in Extest Mode	47	47
Total number of Scan Channels in Intest Mode	262	262

Table 4: Comparison of all parameters for pre – scan and post - scan

Parameters	Pre - Scan	Post - Scan
No. of combinational cells	474495	477948
No. of sequential cells	110424	111027
Combinational area	108392.078749	109423.0146 sqmm
Non- Combinational area	142584.897398	143205.2183 sqmm
Total area	252230.392562	253881.6763 sqmm
Switching power	6.517mW	6.977mW
Internal power	23.012mW	23.719mW
Leakage power	13.2757mW	13.4414mW
Total power	29.512mW	30.739mW
No. of Hold Violations (FCLK)	4825	0
No. of Hold Violations (TO_GCLK)	3334	0
Scan Summary	67.647 %	97.348 %

5. Conclusion

Scan insertion is a successful part of a design methodology by paying attention to practical considerations. Scan insertion is done using Synopsys design compiler Software. The results show that we try to get the maximum coverage by considering all the scenarios which can result in failure of the chip in late stage. We do this in the context of the design of Server SOC. Scan Coverage is achieved for a given logic with minimum effect on the functional timing and area.

6. Future Scope

In the current design multi bit latches are not part of scan chain. At present, these multi bit latches are included in the non scan list as there is no corresponding MDT model available in the library. Because of this scan coverage is less.

The library can be upgraded and there by multi bit latches can be scanned to increase scan coverage.

In some channel centered tiles, repeaters are placed where the clock goes from one tile to another tile. Since these repeaters are placed apart, it is creating scan timing issue. So, these repeaters are placed in separate scan chains.

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