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Minimization of Leakage Current of 6T SRAM using Optimal Technology

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Abstract: ***Leakage components are very important for estimation and reduction of leakage current, especially for low power applications. This provides the motivation to explore the design of low leakage SRAM cells. High leakage currents in deep submicron regimes are becoming a major contributor to total power dissipation of CMOS circuits as the threshold voltage, channel length and gate oxide thickness are scaled. Memory leakage suppression is critically important for the success of power-efficient designs, especially for ultra- low power applications. As the channel length of the MOSFET reduces, the leakage current in the SRAM increases. One method is to reduce the standby supply voltage (VDD) to its limit, which is the Data retention voltage (DRV), leakage power can be substantially reduced. Also, lower operating voltage will lower the stability of SRAM cell. Two schemes are employed; one in which the supply voltage is reduced and the other in which the ground potential is increased. Microwind Simulations are performed with 65nm and 120nm CMOS technology process file and the leakage currents of all the cells And analysis of read speed of 6T SRAM cell are measured and compared. Simulation results revealed that there is a significant reduction in leakage current for this proposed cell with the SVL circuit reducing the supply voltage.***

Keywords: CMOS Gate leakage current, Sub-threshold current, Voltage level switch, SRAM, Stand-by power

1. Introduction

Design techniques for low-power circuits, for example, for use in battery-driven mobile phones, are not only storage circuits (such as flip-flops, register files, and memories) but also needed for logic circuits (such as very fast adders and multipliers). An integrated static random access memory (SRAM) is proposed to reduce leakage power at circuit and architectural level [1]. There are several techniques for reducing standby power. One of the method is multi threshold-voltage CMOS (MTCMOS), This technique reduces the power supply through the use of nMOSFET switches with higher threshold Vthn voltage and pMOSFET switches with higher threshold voltage Vthp. However, it has serious drawbacks such as the need for additional fabrication processes for higher Vthp and higher Vthn and the fact that storage circuits based on this technique cannot retain data. To solve this drawback, a self-controllable voltage level switch, which can decrease stand-by power, while maintain the high speed performance [2]. There is a significant increase in the sub-threshold leakage due to its exponential relation to the threshold voltage, and gate leakage due to the reducing gate-oxide thickness [3]. The sub threshold leakage current is exponentially dependent on the gate-to-source voltage of a MOSFET [4]. When the SRAM circuit are in active mode, the SVL switch generated maximum supply voltage (e.g. VD = 0.7V) and the minimum ground level voltage (Vs = 0V) to them through switches that are turned on. So the SRAM circuit can operate quickly. On the other hand when the SRAM circuit are in stand-by mode, it generates slightly lower supply voltage and relatively higher ground level voltage. The present work describes such an analysis and shows that use of SVL switch for reducing supply voltage yields the maximum reduction in leakage currents especially when the pre charge. Transistors are put in cut-off state during the stand-by mode. An SVL switch can be used either to reduce the supply voltage to the SRAM cell or increase the potential of ground level and the two approaches can be combined as well. Although a technique similar to use of SVL for raising the ground potential has already been reported to yield significant reduction in gate leakage currents [5]. An analysis of leakage currents in 6T SRAM cell has been carried out and techniques for suppressing it are compared. A number of techniques have been reducing the impact of leakage power dissipation such as gate-Vdd scheme [6], Dual-Vt SRAM [7] etc. As a result, even though supply voltage has also been reduced with new generations of technology, the magnitude of leakage current has increased gradually and is likely to become comparable in future CMOS devices [8]. In this 6T SRAM cell comparison with 65 nm technology. The 6T SRAM cell consists of six transistors, in which two inverters (M1, M3 and M2 and M4 are connected in cross coupled manner, transistors M5 and M6 are write access transistor as shown in Fig. 1.

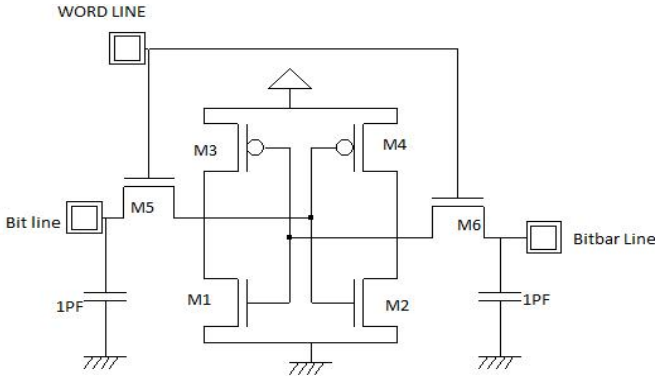

Figure 1: Schematic of 6T SRAM

2. Leakage Control in 6T SRAM Bit Cell

It was described earlier that self- controllable switch can be used either at the upper end of the cell to reduce supply voltage (USVL technique) or at the lower end of the cell to raise the voltage of the ground node (LSVL technique). The switching energy, the short-circuit energy, and the power dissipation are assumed to remain constant under the same power supply. The impact of these techniques on power dissipation is described in the next sections.

2.1 Leakage Control Using USVL

An SRAM cell consisting USVL techniques is shown in Fig.2 In this technique, a full supply voltage is applied to SRAM cell in active mode, while the supply voltage level to SRAM is reduced to voltage level 'Vd' in stand -by mode. Since transistor M3 is in on state, voltage at the drains of M1 and M3 is also reduced to 'Vd'. As before let us consider first the impact on gate leakage currents. As a result of a decrease in gate voltage of transistor M2, gate leakage current through it is sharply reduced. A decrease in drain voltage of transistor M1 results in lower gate-drain voltage across it and thus gate leakage current through it is also reduced. A decrease in source voltage of M6 results in a decrease in one component of EDT (Edge direct tunneling) leakage across it while leaving the other unchanged Gate leakage across transistor M5 remains unchanged. Transistor PU1 being a PMOS transistor does not result in any significant added leakage current as a result of transistors used in USVL circuit. LSVL technique has a better effect on power dissipation reduction. However, this technique is inferior with respect to sub threshold leakage current. While, sub threshold leakage through transistors M1 and M4 is reduced, further, a new sub threshold leakage current appears in transistor M6 as a result of reduction in its source voltage. To summarize, the USVL technique, while more successful in reducing power dissipation, still leaves two gate leakage current component in access transistor is unchanged.

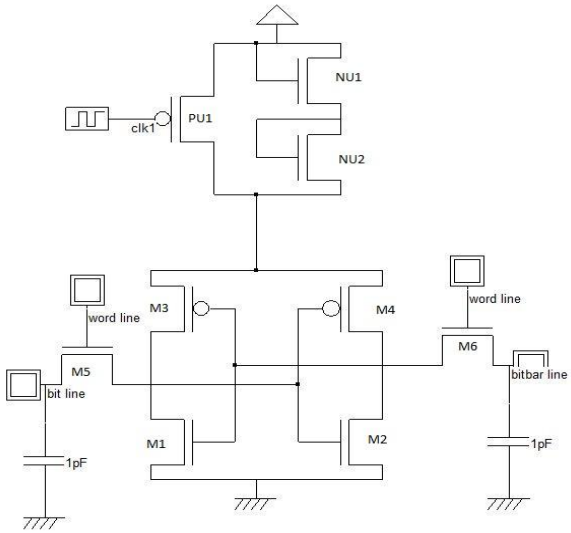

Figure 2: Schematic of 6T SRAM cell after applying USVL technique

2.2 Leakage Control Using LSVL

Fig. 3 shows a schematic of 6T SRAM cell in which LSVL technique is applied. The switch provides '0' Volt at the ground node during the active mode and an increased ground voltage (virtual ground) during the stand -by mode. This technique is similar to the diode footed cache design scheme proposed to control gate and sub -threshold leakages in SRAM cell, in which a diode designed with high Vt MOS transistors, was used to increase the ground voltage of SRAM in the stand-by mode [9].

Let us consider the effect of this technique on power dissipation. An increase in the virtual ground voltage (Vs) therefore decrease of gate-source and gate-drain voltages of transistor M1 and gate-drain voltage of transistor M2 and results in sharp reduction in gate leakage currents of these two transistors. An SVL can be used either to reduce the supply voltage to the SRAM cell or increase the potential of ground node and the two approaches can be combined as well. However, there is no improvement in gate leakage currents for transistors M5 and M6.In fact, as a result of increase in drain voltage of M2. Incorporation of SVL results in another new gate leakage current through NMOS transistor NL1 in the SVL switch. As far as sub threshold leakage currents are concerned, LSVL approach is successful in reducing currents through M1, M4 and M5 as well. To summarize, one note that while all power dissipation are reduced using LSVL approach, it is only partially successful.

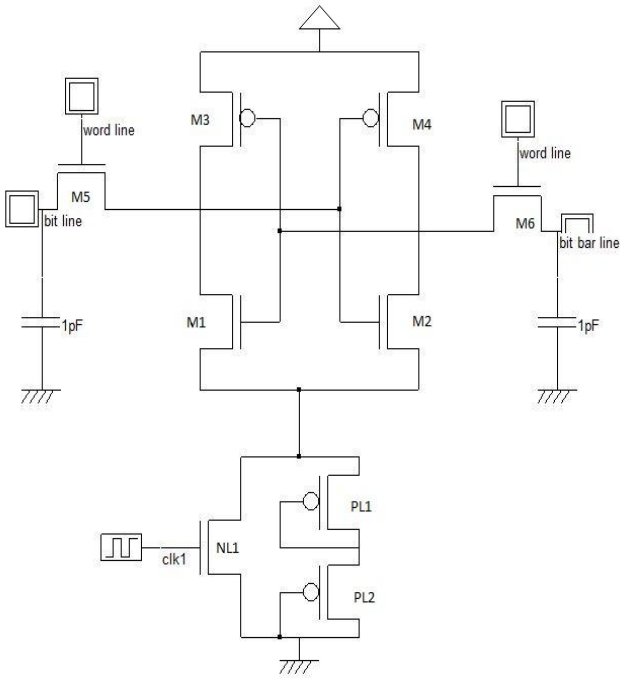

Figure 3: Schematic of 6T SRAM cell after applying LSVL technique

2.3 Leakage Control Using Combined Technique (USVL & LSVL)

Fig.4 shows the schematic of mixed technique (e.g. LSVL & USVL) [9],[10] .In this seven transistors SRAM. By using this technique supply voltage is reduced. Technique LSVL

and USVL both are connected to the conventional 6T SRAM.

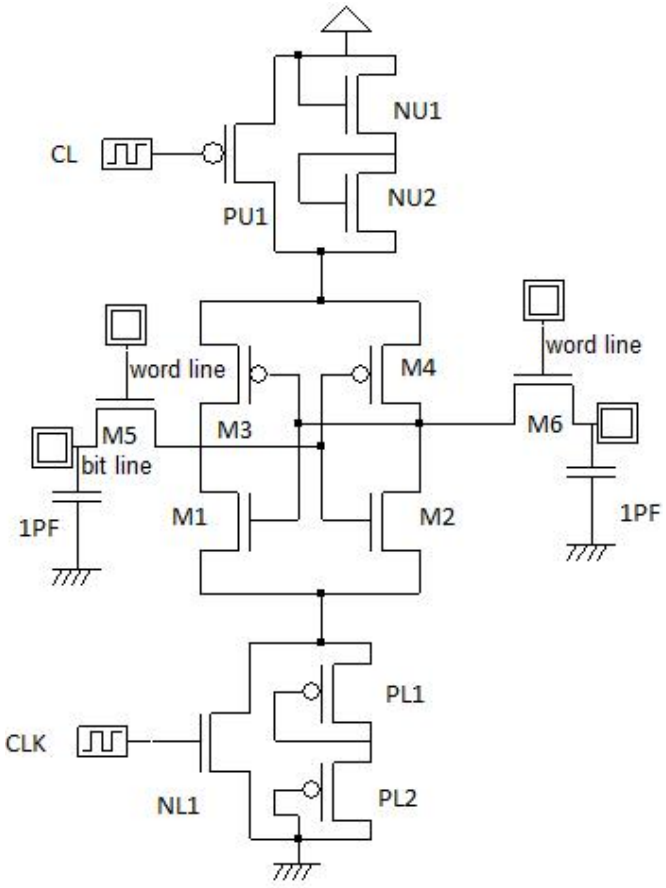

Figure 3: Schematic of 6T SRAM cell after applying USVL& LSVL technique

3. Advantage of SVL Techniques

There are very important advantages of the SVL circuit. When the SRAM circuit are in active mode, the SVL circuit supplies maximum drain-source voltage to the on MOS through on Switch, thus the SRAM circuit can operate quickly. On the other hand, when the SRAM circuit are in stand-by mode, it supplies slightly lower Vd and slightly higher Vs to MOS transistor through “weakly on switch”, thus the SVL circuit not only retains data but also produces high noise immunity with minimal overheads in terms of silicon area. Furthermore the Vth increase and consequently sub threshold current (Isub) of the “off MOS” transistor decrease, so stand-by power is greatly reduced.

4. SRAM Basics

The memory circuit is said to be static if the stored data can be retained indefinitely, as long as the power supply is on, without any need for periodic refresh operation. The data storage cell, i.e., the one-bit memory cell in the static RAM arrays, invariably consists of a simple latch circuit with two stable operating points. Depending on the preserved state of the two inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '0' or as logic '1'. To access the data contained in the memory cell via a bit line, we need at least one switch, which is controlled by the corresponding word line as shown in Fig. 5.

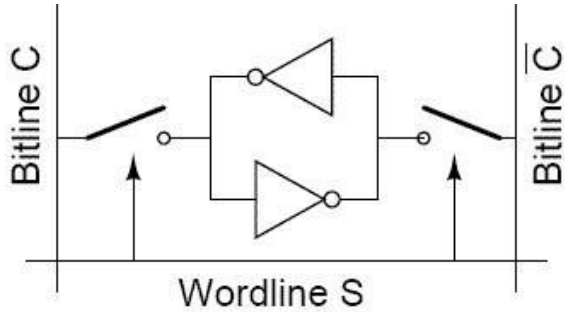

Figure 5: Basic SRAM cell

4.1 Read Operation

The voltage levels in the CMOS SRAM cell at the beginning of the "read" operation [11], [12] are depicted in Fig.6 Here, the transistors M2 and M3 are turned off, while the transistors Ml and M4 operate in the linear mode. Thus, the internal node voltages are V1= 0 and V2 = VDD before the cell access (or pass) transistors M5 and M6 are turned on. After the pass transistors M5 and M6 are turned on by the row selection circuitry, the voltage level of column C will not show any significant variation since no current will flow through M6. On the other half of the cell, however, M5 and Ml will conduct a nonzero current and the voltage level of column C will begin to drop slightly. Note that the column capacitance Cc is typically very large; therefore, the amount of decrease in the column voltage is limited to a few hundred millivolts during the read phase. The data read circuitry to be examined for detecting this small voltage drop and amplifying it as a stored "0 " .While M1 and M5 are slowly discharging the column capacitance, the node voltage V, will increase from its initial value of 0 V. Especially if the (W/L) ratio of the access transistor M5 is large compared to the (W/L) ratio of Ml, the node voltage V may exceed the threshold voltage of M2 during this process, forcing an unintended change of the stored state. The key design issue for the data-read operation is then to guarantee that the voltage V, does not exceed the threshold voltage of M2, so that the transistor M2 remains turned off during the read phase, i.e.

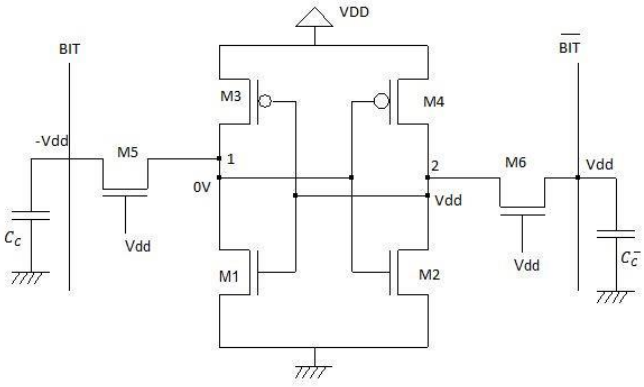

Figure 6: Read 0 operation of 6T SRAM cell.

$$(V_1)_{max} \leq (V_T)_2 \ldots\ldots\ldots\ldots \text{(4.1.1)}$$

Hence M5 operate in saturation region while M1 operate in Linear region

$$\frac{K_{n,5}}{2}\left(0 - V_{DD} - V_{T,p}\right)^2 \leq \frac{K_{n,1}}{2}\left(2\left(V_{DD} - V_{T,n}\right)V_{T,n} - V_{T,n}^2\right) \ldots\ldots (4.1.2)$$

$$\frac{K_{n,5}}{K_{n,1}} \leq \frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}-2V_{T,n})^2} \ldots\ldots(4.1.3)$$

4.2 Write operation

Now consider the write "0" operation,[13] assuming that a logic "1" is stored in the Fig.7. Voltage levels in the SRAM cell at the beginning of the "write" operation. SRAM cell initially, the transistors M1 and M4 are turned off, while the transistors M2 and M3 operate in the linear mode. Thus, the internal node voltages are V1=VDD and V2= 0V before the cell access (or pass) transistors M5 and M6 are turned on data The column voltage Vc is forced to logic "0" level by the data-write circuitry; thus, we may assume that Vc is approximately equal to 0 V. Once the pass transistors M5 and M6 are turned on by the row selection circuitry, we expect that the node voltage V2 remains below the threshold voltage of M1, since M2 and M6 are designed according to condition (4.1.1). Consequently, the voltage level at node (2) would not be sufficient to turn on Ml. To change the stored information, i.e., to force V1, to 0 V and V2 to VDD, the node voltage V1, must be reduced below the threshold voltage of M2, so that M2 turns off first. When V 1= VT, the transistor M5 operates in the linear region while M3 operates in saturation.

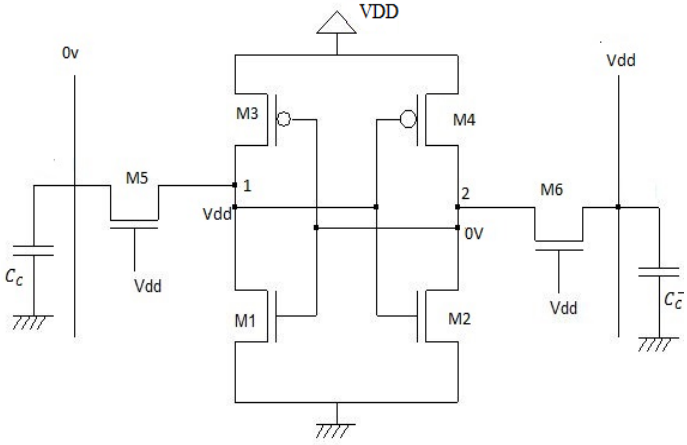

Figure 7: Write0 operation of 6T SRAM cell

$$\frac{Kp,3}{2}(0-V_{DD}-V_{T,n})^2 \leq \frac{Kn,5}{2}(2(V_{DD}-V_{T,n})V_{T,n}-V_{T,n}{}^2) \ldots (4.2.1)$$

Rearranging this condition result in:

$$\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_5} \leq \frac{\mu_n}{\mu_p}\frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}+V_{T,n})^2} \ldots\ldots\ldots(4.2.2)$$

4.3 Standby Operation

If the word line is not asserted, the access (Pass) transistors will be disconnect the cell from the bit lines. The two cross coupled inverters formed the two inverter connected back to back reinforce each other as long as they are disconnected from the outside world. And they will retain the data which they have already stored in the memory cell.

5. Simulation Result and Discussion

The simulation of 6T SRAM cell has been done using Micro wind tool at 65 nm and 120 nm technology. Although the circuit is simulated under ideal condition, there are various constrains on simulation parameter like transistor length and width, temperature effect, on the 6T SRAM Cell. The leakage currents in conventional 6T SRAM cell and by using USVL and LSVL technology. This bar graph show that comparison between among this technology with 80°C, show in Fig.8.

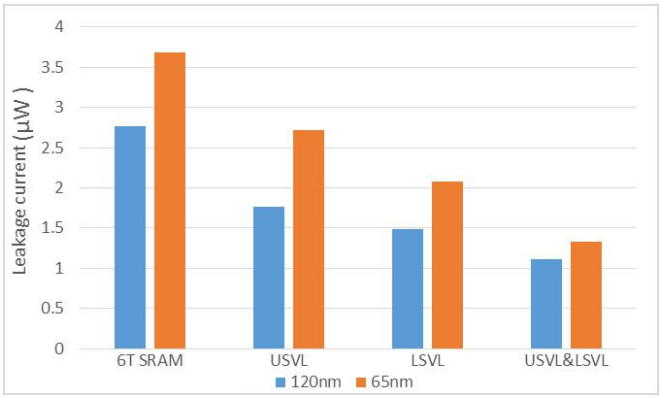

Figure 8: Comparison of leakage current

Simulation result of read '0' operation

Before the read operation, the WL remains at VDD and the read bit-lines (BL and BLB) is initially pre-charged to VDD. During the read operation, the WL is given a low voltage and pulled to ground. If the storage node V1 stores a low voltage, and BLB will remain at VDD during the read operation. The storage node V1 stores a high voltage, and BL will be pulled low. A small voltage difference between the bit-lines will be developed and can be sensed by the differential sense amplifier. On the other hand if the storage nodes V1 and V2 store high and low voltage respectively the BLB will remain at VDD and it will be pulled low. Read 0 operation shown in Fig.9, and Read 1 operation shown in Fig.10.

Simulation result of read 0

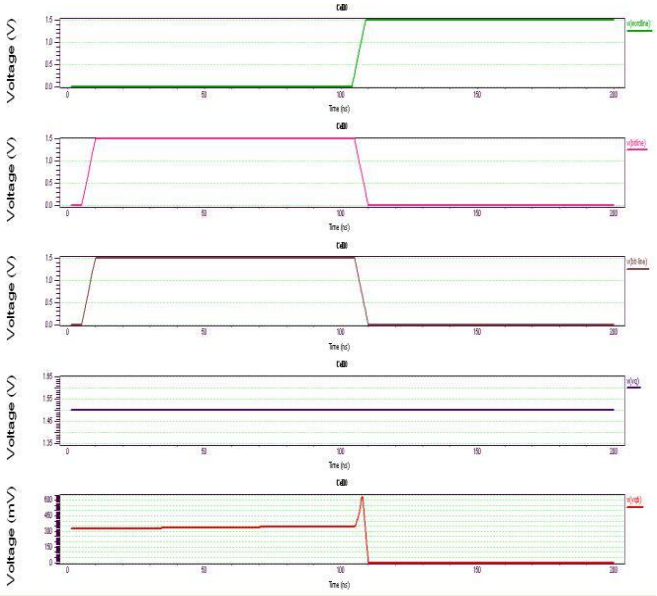

Figure 9: Simulation result of '0' operation when VDD=1.5 volt

Simulation result of '1' operation

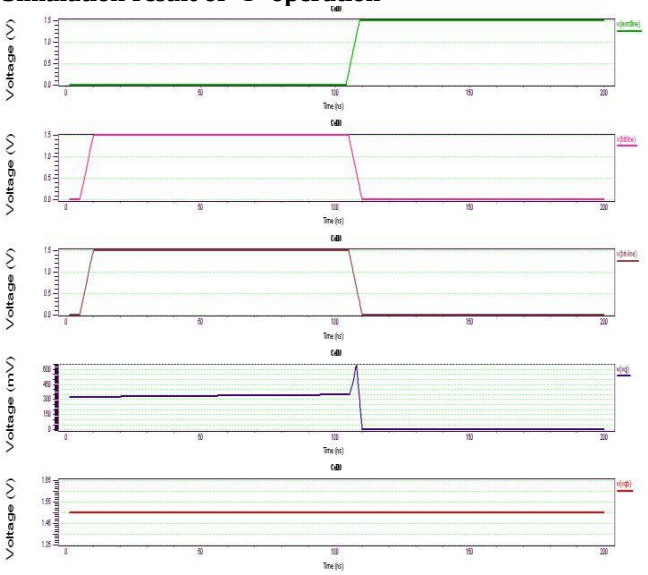

Figure 10: Simulation result of '1' operation when VDD=1.5 volt

We have varies the W/L ratio of access transistor as 1.5, 2.2 and 1.0 and fixed the W/L ratio of driver transistor as 1.5 and find the saturation current We varies the W/L ratio of access transistor and note down the spike on V1 during read 0 and V2 during read 1, through simulation result and calculate the I5 saturation current of each different W/L ratio and find the almost similar result by the software, but their small changed in spike on voltage node V2 and V1, all the calculated value shown in table 1 and table 2 respectively.

Table 1: Comparison table of read 0 operation in 6T SRAM

Power Supply (Volt)	$\left(\frac{w}{l}\right)_5$	$\Delta t_{(ns)}$	$\Delta V_{(mv)}$	$I_{5(\mu amp)}$
1.8	2.2	1.4	0.3	211.2
	1.5	1.7	0..25	144
	1.0	3.6	0.35	
1.5	2.2	1.2	0.2	161.7
	1.5	2.2	0.3	109.5
	1.0	4.08	0.25	73.5
1.2	2.2	1.8	0.3	161.7
	1.5	3.17	0.35	110.25
	1.0	4.08	0.3	73.5

Table 2: Comparison table of read 1operation in 6T SRAM

Power Supply (Volt)	$\left(\frac{w}{l}\right)_5$	$\Delta t_{(ns)}$	$\Delta V_{(mv)}$	$I_{5(\mu amp)}$
1.8	2.2	1.8	0.4	211.2
	1.5	2.08	0.3	144
	1.0	4.1	0.4	96
1.5	2.2	2.4	0.4	161.7
	1.5	2.7	0.3	109.5
	1.0	3.4	0.25	73.5
1.2	2.2	1.2	0.2	161.7
	1.5	4.5	0.5	110.25
	1.0	2.04	0.15	73.5

6. Conclusion

As technology scales down, the supply voltage must be reduced such that dynamic power can be kept at reasonable levels and power delivery can still be performed within the functional requirements. However, as a result of scaling, power dissipation due to leakage currents has also increased dramatically and is a major source of concern especially for low power applications. This paper introduces how to control the leakage current in SRAM cell and optimizes the power. The amount of embedded SRAM in modern micro - processors and systems -on-chips (SOCs) increases to meet the performance requirements in each new technology generation SRAM cells for a 65 nm, 120 nm technology shows that leakage currents contribute significantly to overall leakage power dissipation in stand-by mode. Reduction in supply voltage and increase in ground voltage using self-controllable voltage level switches for reducing An analysis of leakage currents in 6T, leakage currents in 6T SRAM with USVL and LSVL technology .It is found that while the LSVL approach is better in terms of reduction in leakage current (Isub), the USVL approach performs better with respect to gate leakage currents (Igate). However, both these techniques are found to be inadequate for reduction of leakage currents through access transistors. An offers reduced leakage currents in caches. The novel SRAM design exploits the fact that most of the bits stored in caches are zeroes. Simulation results show that 33% reduction in 65nm ,and 23% in 120nm the total leakage currents was minimized at 80°C with marginal degradation in the performance compared to the conventional 6T SRAM cell.

7. Acknowledgement

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References

[1] Zhang, L., Wu, C., Mao, L., & Zheng, J. (2012). Integrated SRAM compiler with clamping diode to reduce leakage and dynamic power in Nano-CMOS process. *Micro & Nano Letters, 7*(2), 171–173.

[2] Enomoto, T., Oka, Y., Shikano, H., & Harada, T. (2002). A self- controllable voltage-level (SVL) circuit for low-power, high-speed CMOS circuits. In *Proceedings of European solid-state circuits conference* (pp. 411–414). Firenze, Italy

[3] Birla, S., Singh, R. K., & Pattanaik, M. (2011). Static noise margin analysis of various SRAM topologies. *IACSIT International Journal of Engineering and Technology, 3* (3), 304–309

[4] Birla, S., Shukla, N., Pattanaik, M., & Singh, R. K. (2010) Device and circuit design challenges for low leakage SRAM for ultra-low power applications. *Canadian Journal on Electrical and Electronics Engineering, 1* (7), 11–15, 156– 167.

[5] Agarwal, A., & Roy, K. (2003). A noise tolerant cache design to reduce gate and sub -threshold leakage in the nanometer regime. In *ISPLED'03* (pp. 18–21).
[6] Agarwal, A., Li, H., & Roy, K. (2002). DRG-cache: A data retention gated-ground cache for low power. In *Proceedings of the 39th design automation conference* (pp. 473–478
[7] Hamzaoglu, F., Ye, Y., Keshavarzi, A., Zhang, K., Narendra, S., Borkar, S., Stan, M., & De, V. (2000). Dual Vr SRAM cells with full-swing single-ended bit line sensing for high-performance on-chip cache in 0.13um technology generation. In Proceedings of the 2000 international symposium on low power electronics and design (pp. 15–19).
[8] Hamzaoglu, F., & Stan, M. (2002). Circuit-level techniques to control gate leakage for sub-100 nm CMOS. In *ISPLED'02* (pp. 60-63). Monterey, CA, USA
[9] Ho, Y., Chang, C., & Su, C. (2012). Design a sub threshold-supply bootstrapped CMOS inverter based on an active leakage-current reduction technique. *IEEE Transactions on Circuits and Systems, 59*(1), 55–59
[10] Hong Zhu and Volkan Kursun "A Comprehensive Comparison of Data Stability Enhancement Techniques with Novel Nanoscale SRAM Cells under Parameter Fluctuations" IEEE transactions on circuits and system, regular papers, vol. 61, no. 5, may 2014
[11] S. M. Kang, Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis Design", TATA McGraw- Hill Publication, 2e, 2003
[12] Adel S. Sedra, Kenneth C.Smith, "Microelectronic circuits", Oxford University Press,5e, 2003
[13] K.S. Yeo, K. Roy, "Low- Voltage, Low-Power VLSI Subsystems", 2e, 2009.

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