International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391

Reduction of Total Harmonics Distortion in PV based Three-Level Neutral Point Clamped Inverter using Space Vector Modulation

R. Kiruthiga[1], S. Komalachitra[2]

[1,2]Assistant Professor, Department of EEE, Sri Sairam Institute of Technology

Abstract: ***In this paper the space vector modulation technique is applied to the three-level neutral Point Clamped (NPC) inverter, resulting to a significant reduce of ripple and total harmonics distortion. Additionally solar PV source integrated with battery storage is used as the source. Three-level neutral point clamped inverters have been widely used in medium voltage applications. This type of inverters have several advantages over standard two-level VSI, such as greater number of levels in the output voltage waveforms, less harmonic distortion in voltage and current waveforms and lower switching frequencies. This paper emphasizes the derivation of switching states using the Space Vector Pulse Width Modulation (SVPWM) technique and further reducing the total harmonic distortion. The control scheme is implemented using Matlab/Simulink. Experimentally the results are compared using the steady-state performance of the proposed control strategy.***

Keywords: space vector modulation, multi-level inverter, total harmonic reduction, solar and battery integration

1. Introduction

Due to the world energy crisis and environmental problems caused by conventional power generation, renewable energy sources such as photovoltaic (PV) and wind generation systems are becoming more promising alternatives to replace conventional generation units for electricity generation. Advanced power electronic systems are needed to utilize and develop renewable energy sources. In solar PV or wind energy applications, utilizing maximum power from the source is one of the most important functions of the power electronic systems. In three-phase applications, two types of power electronic configurations are commonly used to transfer power from the renewable energy resource to the load: single-stage and double-stage conversion. In the double-stage conversion for a PV system, the first stage is usually a dc/dc converter and the second stage is a dc/ac inverter. The function of the dc/dc converter is to facilitate the maximum power point tracking (MPPT) of the PV array and to produce the appropriate dc voltage for the dc/ac inverter. The function of the inverter is to generate three-phase sinusoidal voltages or currents to transfer the power to the load in a stand-alone system. In the single-stage connection, only one converter is needed to fulfill the double-stage functions, and hence the system will have a lower cost and higher efficiency, however, a more complex control method will be required. One of the major concerns of solar and wind energy systems is their unpredictable and fluctuating nature. -connected renewable energy systems accompanied by battery energy storage can overcome this concern. This also can increase the flexibility of power system control and raise the overall availability of the system Usually, a converter is required to control the charging and discharging of the battery storage system and another converter is required for dc/ac power conversion; thus, a three phase PV system connected to battery storage will require two converters. This paper is concerned with the design and study of a three-phase solar PV system integrated with battery storage using only one three-level converter having the capability of MPPT and ac-side current control, and also the ability of controlling the battery charging and discharging. This will result in lower cost, better efficiency and increased flexibility of power flow control.

The remainder of the paper is organized as follows. Section II describes the structure of a three-level inverter. Section III describes the space vector modulation technique. Section IV presents the proposed topology to integrate solar PV and battery storage and its associated control. Section V describes the simulation of the proposed topology and comparison. Section VI concludes the paper

2. Structure of Three Level NPC Invertor

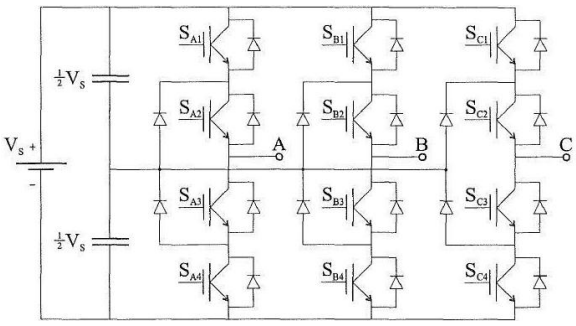

Figure 1: Three-level neutral point clamped inverter

Figure 1 shows the diagram of three-level neutral point clamped inverter. The operating status of the switches in the NPC inverter can be represented by the switching states shown in Table 1. In case of a two-level inverter there are a total of eight switching-states (six result into active vectors and two result into zero vector). The number of switching states for n level NPC inverter is given by

Number of switching-states = n3

Hence, in case of a three-level NPC inverter, there are 27 switching-states and among them, three result in zero vector and 24 result in non-zero (active) vectors. Each switching state (combination of phase/leg switches) produces a defined set of three-phase voltages (eventually, voltage space vector), which can be represented in a hexagon form. The SVPWM method is an advanced, computation intensive PWM method and is possibly the best among all the known PWM techniques for variable-frequency drive applications.

Table 1: Switch States of A Three-Level NPC Inverter

Switch States				
S_1	S_2	S_3	S_4	Output Voltage
ON	ON	OFF	OFF	$+1/2\ V_s$
OFF	ON	ON	OFF	0
OFF	OFF	ON	ON	$-1/2V_s$

The principle of the SVPWM method is that the command voltage vector is approximately calculated by using three adjacent vectors. The duration of each voltage vectors obtained by vector calculations:

T1V1 +T2V2 + T3V3
=TSV* T1 + T2 + T3 = TS

Where 1 2 V, V and 3 V are vectors that define the triangle region in which * V is located. 1 2 T, T and 3 T are the corresponding vector durations and s T is the sampling time. In a three level inverter similar to a two-level inverter, each space vector diagram is divided into 6 sectors. For simplicity here only the switching patterns for sector A will be defined so that calculation procedure for the other sector will be similar. Sector A is divided into 4 regions where all the possible switching states for each region are given as well. SVPWM for three level inverter can be implemented by using the steps of sector determination, determination of the region in the sector, calculating the switching times Ta, Tb, Tc and finding the switching states.

3. Space Vector Modulation

A. Principle of working

The working principle of the conventional 6 switch 3 phase inverter is explain under the following space vector modulation technique.

Space Vector Modulation (SVM)
Space Vector Modulation (SVM) is quite different from the PWM methods. With PWMs, the inverter can be thought of as three separate push-pull driver stages, which create each phase waveform independently.

SVM, however, treats the inverter as a single unit, specifically, the inverter can be driven to eight unique states. The concept of space vector is derived from the rotating field of ac machine which is used for modulating the inverter output voltage. If three phase sinusoidal and balanced voltages are applied to a three-phase induction motor, it can be shown that the space vector with magnitude Vm rotates in a circular orbit at angular velocity ω where the direction of rotation depends on the phase sequence of the voltages.

SVM is a digital modulating technique, where the objective is to generate PWM load line voltages that are in average equal to a given load line voltage. This is done in each sampling period by properly selecting the switch states of the inverter 0and the calculation of the appropriate time period for each state.

The SVM for a three leg voltage source inverter is obtained by sampling the reference vector at the fixed clock frequency 2fs. All the eight possible switching combinations of the switching network are mapped into an orthogonal plane. The results are six non-zero vectors and two zero vectors. The six non-zero switching vectors form a hexagon as shown below.

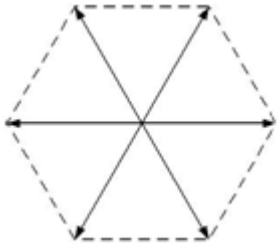

Figure 2: Vector Representation

To implement the space vector PWM, the voltage equations in the a-b-c reference frame can be transformed into the stationary d-q reference frame that consists of the horizontal (direct) and vertical (quadrature) axes.

Then it involves decomposing a desired voltage space vector V into voltage vector components that can be generated using a typical three-phase inverter.

There are eight possible combinations of ON and OFF patterns for the three upper power switches. The ON and OFF states of the lower power devices are opposite to the upper one and so are easily determined once the states of the upper power switches are determined.

Modulation Scheme

There are four steps to perform the space vector modulation:

First, the reference signals for phase A, B and C are mapped into the orthogonal d-q coordinates, and are represented by a reference vector Vref.

Second, switching vectors are selected, including non-zero and zero vectors to synthesize the reference vector Vref for one switching cycle.

Third, the time durations for all selected switching vector are calculated by a simple trigonometric algorithm. The objective is to make the averaged switching vector in one switching cycle equal to the reference vector Vref.

Fourth, the switching vectors are sequenced and dispatched to the switching network.

B. Balanced Capacitors Voltage

The converter has two capacitors in the dc side to produce the three-level ac-side phase voltages. Normally, the capacitor voltages are assumed to be balanced, since it has been reported that unbalance capacitor voltages can affect the ac side voltages and can produce unexpected behavior on system parameters such as even-harmonic injection and power ripple

Various strategies have been proposed to balance the capacitor voltages using modulation algorithms such as sinusoidal carrier based PWM (SPWM) or space vector pulse width modulation (SVPWM)

In SPWM applications, most of the strategies are based on injecting the appropriate zero-sequence signal into the modulation signals to balance the dc-link capacitors. In SVPWM applications, a better understanding of the effects of the switching options on the capacitor voltages in the vector space has resulted in many strategies proposed to balance capacitors voltages in the three-level NPC inverter. In vector control theory, ideally, the inverter must be able to generate the voltage output instantaneously, following the reference vector (*V*ref). However, because of the limitation of the switches in the inverter, it is not possible to guarantee that any requested vector can be generated; as a matter of fact, only a limited number of vectors (27 vectors for three-level inverter) can be generated. To overcome such difficulties, in space vector modulation the reference vector *V* ref is generated by selecting the appropriate available vectors in each time frame in such a way that the average of the applied vectors must be equal to the reference vector.

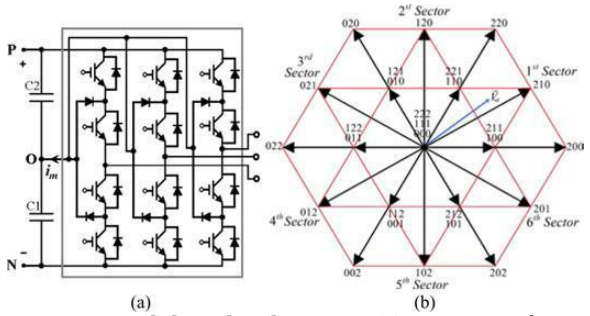

Figure 3: Typical three-level inverter (a) structure of circuit, and (b) three-level inverter space vector diagram

4. Proposed Topology to Integrate Solar PV and Battery Storage Using an Improved Unbalanced DC Functionality of a Three-Level Inverter

Based on the discussions in Sections I and II, two new configurations of a three-level inverter to integrate battery. Storage and solar PV shown in Figure are proposed, where no extra converter is required to connect the battery storage to the grid connected PV system. These can reduce the cost and improve the overall efficiency of the whole system particularly for medium and high power applications.

Fig. (a) shows the diagram of the basic configuration. In the proposed system, power can be transferred to the grid from the renewable energy source while allowing charging and discharging of the battery storage system as requested by the control system. The proposed system will be able to control the sum of the capacitor voltages (VC1 + VC2 = Vdc) to achieve the MPPT condition and at the same time will be able to control independently the lower capacitor voltage (VC1) that can be used to control the charging and discharging of the battery storage system. Further, the output of the inverter can still have the correct voltage waveform with low total harmonic distortion (THD) current in the ac side even under unbalanced capacitor voltages in the dc side of the inverter.

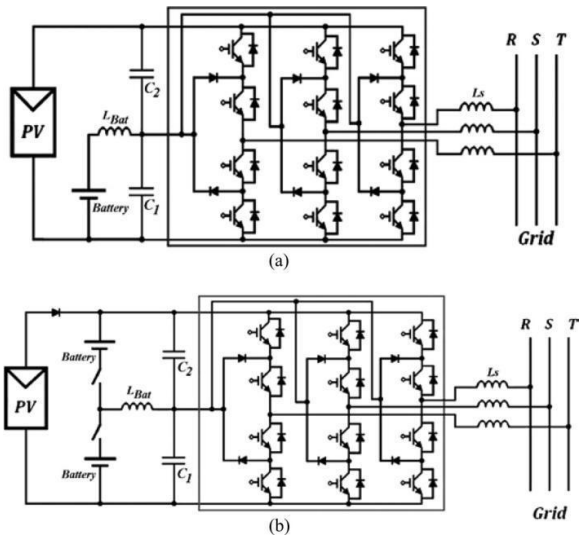

Figure 4: Proposed configurations for integrating solar PV and battery storage: (a)basic configuration; (b) improved configuration.

Although this configuration can operate under most conditions, however when the solar PV does not produce any power, the system cannot work properly with just one battery.

Fig. (b) shows the improved configuration where two batteries are now connected across two capacitors through two relays. When one of the relays is closed and the other relay is open, the configuration in Fig (b). When the renewable energy is unavailable, both relays can be closed allowing the dc bus to transfer or absorb active and reactive power to or from the grid. It should be noted that these relays are selected to be ON or OFF as required; there is no PWM control requirement.

5. Simulation Results

A. Proposed System

The simulation results for space vector modulation technique are given below.

The input solar DC voltage waveform, switching pulses for positive leg inverters for one cycle, the output voltage waveform, the output current waveform and FFT analysis simulation results of space vector width modulation are shown in fig. 6.a, b, c , d and e respectively

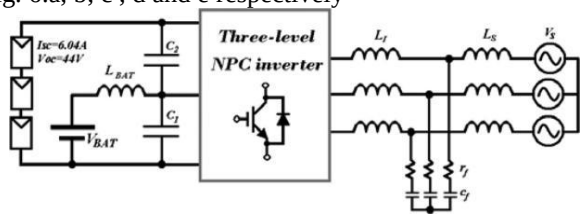

Figure 5: above shows the block diagram of simulation system.

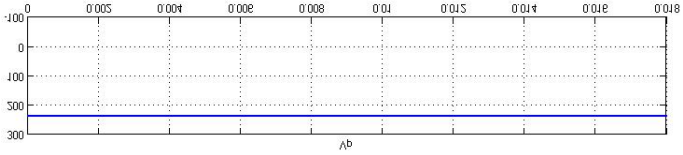

Figure 6 (a): Output voltage of solar PV

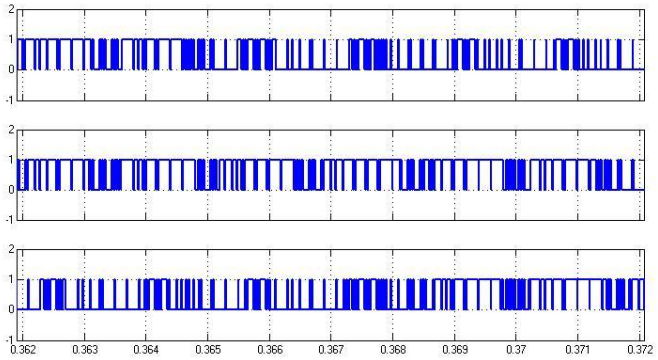

Figure 6 (b): Switching pulse for M1, M3, M5

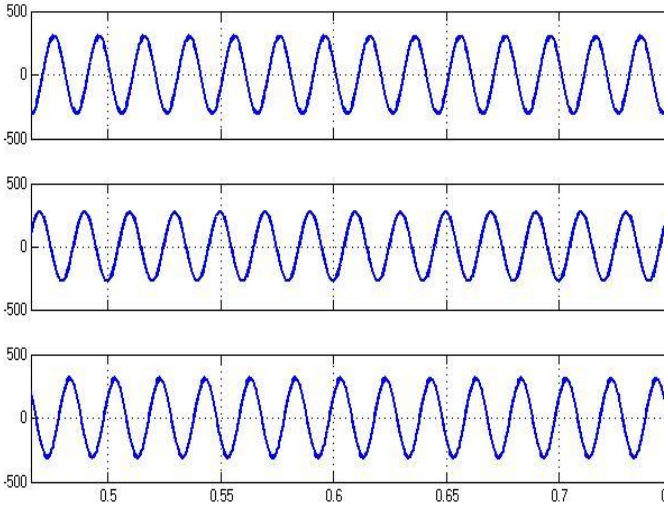

Figure 6 (c): Output voltage

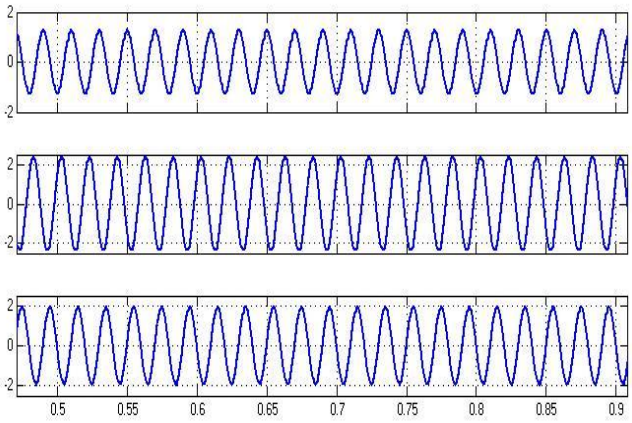

Figure 6 (d): Output current

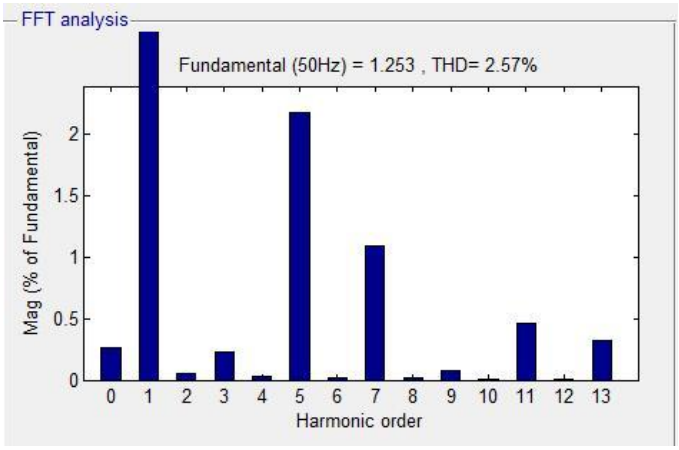

Figure 6 (e): THD

B. Existing System

The simulation results for single pulse width modulation technique are given below.

The input solar DC voltage waveform, switching pulses for positive leg inverters for one cycle, the output voltage waveform, the output current waveform and FFT analysis simulation results of single pulse width modulation are shown in fig. 7.a, b, c, d and e respectively

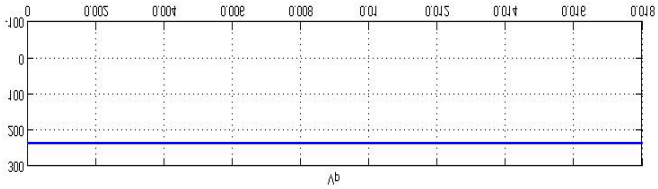

Figure 7 (a): Output voltage of solar PV

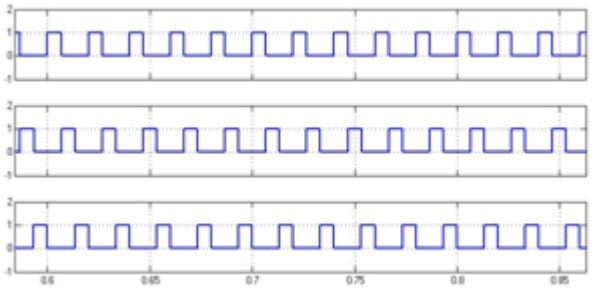

Figure 7 (b): Switching pulse for M1, M3, M5

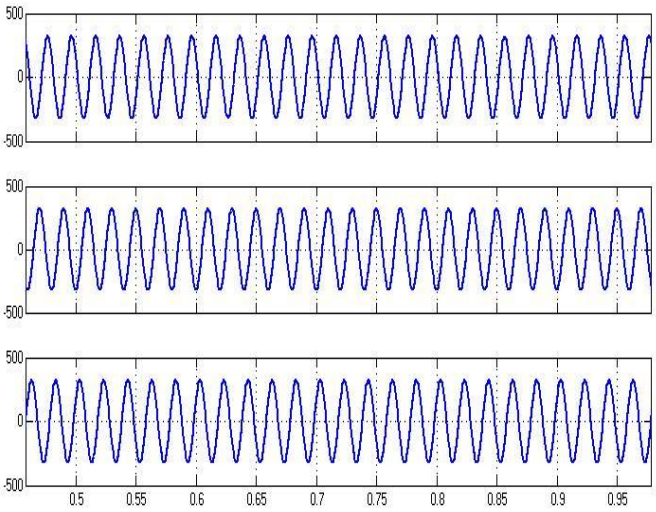

Figure 7 (c) Output voltage

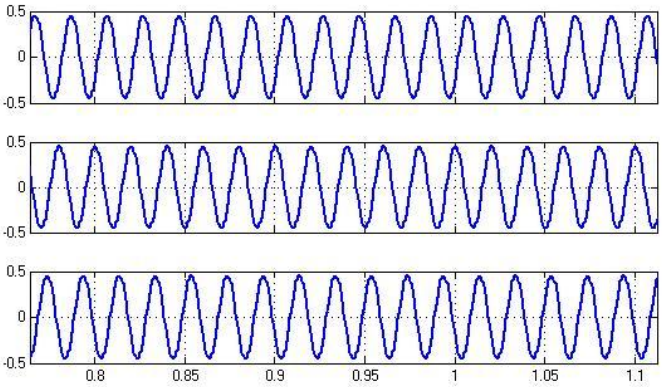

Figure 7 (d): Output current

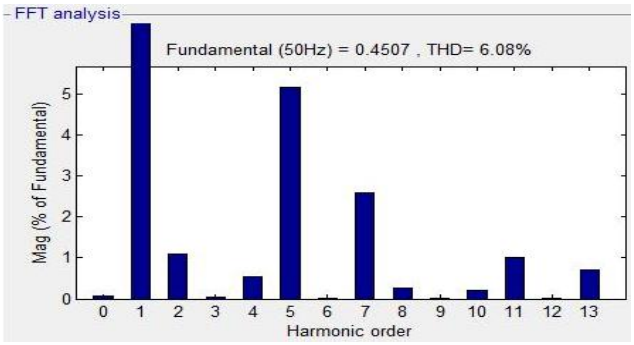

Figure 7 (e): THD

C. Comparison of THD

From the FFT analysis we get a 3.51% reduction in the Total Harmonic Distortion (THD).

NPC Inverter	THD
Single PWM	6.08%
SVM	2.57%

6. Conclusion

A novel topology for a three-level NPC voltage source inverter that can integrate both renewable energy and battery storage on the dc side of the inverter has been presented. A theoretical framework of a novel extended unbalance three-level vector modulation technique that can generate the correct ac voltage under unbalanced dc voltage conditions has been proposed. A new control algorithm for the proposed system using SVM has been presented that greatly reduces the harmonics and hence increases efficiency. The proposed system can be extended to grid connected renewable energy systems with battery storage. The effectiveness of the proposed topology was tested using simulations and results are presented.

References

[1] Z. Jian-Yong, S. Zhang-Liang, M. Jun, and L.-f. Wang, "An improved neutral-point voltage balancing algorithm for the npc three-level inverter based on virtual space vector PWM," in *Proc. Int. Conf. Elect. Control Eng.*, Jun. 2010, pp. 3283–3287.

[2] Hamid R. Teymour , Danny Sutanto , Kashem M. Muttaqi, "Solar PV and Battery Storage Integration using a New Configuration of a Three-Level NPC Inverter With Advanced Control Strategy" in IEEE Transactions of energy conversion, vol. 29, no. 2, june 2014.

[3] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-vector pulsewidth modulation for three-level npc converter with the neutral point voltage control," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5076–5086, Nov.2011.

[4] J. Pou, D. Boroyevich, and R. Pindado, "New feedforward space-vector PWM method to obtain balanced AC output voltages in a three-level neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1026–1034, Oct. 2002.

[5] S. Busquets-Monge, S. Somavilla, J. Bordonau, and D. Boroyevich, "Capacitor voltage balance for the neutral-point-clamped converter using the virtual space vector concept with optimized spectral performance," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1128–1135, Jul. 2007. *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 123–131, Jan. 2005.

[6] Z. Huibin, S. Jon Finney, A. Massoud, and B. W. Williams, "An SVM algorithm to balance the capacitor voltages of the three-level npc active power filter," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2694–2702, Nov. 2008.

[7] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 305–314, Feb. 2009.
[8] A. Yazdani and R. Iravani, Voltage-Sourced Converters in Power Systems. New York, NY, USA: Wiley, 2010.