International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391

An Ultra-Low-Power Frequency Multiplier based on Mixed-Mode DLL with Output Frequency from 4 to 6 GHz

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Abstract: ***An Ultra-Low-Power frequency multiplier based on Mixed-Mode DLL is presented in this paper. The operating frequency range is between 100 and 150 MHz which enables to produce output signals in the frequency range from 4 to 6 GHz. NAND-based delay cells are used in the digital part of the delay line due to their wide operating frequency range and small intrinsic delay. The analogue part of the delay line is based on the inverter delay chain with biasing circuit. It was added into the system to overcome the resolution problem and improve jitter performance. The total locking time changes from 10 to 14 clock cycles based on the operating frequency. The simulated peak-to-peak jitter is 21 ps and 1.95 ps for the generated clock operating at 5 GHZ and output clock of DLL operating at 125 MHz respectively.***

Keywords: mixed-mode DLL, frequency generation, phase selection, jitter.

1. Introduction

In high-performance system on chip (SoC), more than one frequency generation block is necessary to derive the various clocks and LO frequencies. These multiple frequencies are generated with Phase Locked Loops (PLLs) due to the given good phase noise and output spectrum. However, PLLs have some drawbacks which makes it unstable and difficult to design like high order loop filter characteristic and jitter accumulation. For conventional PLLs, it is common to use LC-type voltage controlled oscillators (VCOs) which occupy large area and consume high power. That is why using multiple PLLs is not very practical under these circumstances. Instead of PLLs, Delay Locked Loops (DLLs) are alternative for frequency generation. Unlike PLLs DLLs do not accumulate jitter over each clock cycle and have lower power consumption [1]. It is the first order system which makes it easy to design and stable in most cases. Since DLLs occupy small area, multiple of them can be used in complicated systems without area penalty. Furthermore, PLLs have some pulling effect between their VCOs which makes difficult to use multiple of them in the same design but in case of DLL pulling effect is avoided due to the absence of VCO.

The DLL is mainly classified into three different categories which are analogue, digital and mixed-mode DLL [4]. The typical analogue DLL has voltage controlled delay line (VCDL) to delay the input signal and create equidistant multiple phases which can be used to generate higher frequency. Furthermore, it zcontains a phase detector (PD) to measure and detect the phase difference between the input and output signals and a charge pump to charge or discharge the loop filter (LF) capacitor based on the PD output signals (UP/DOWN). This adjusts the control voltage Vctrl to determine the total delay time of VCDL. Although analogue DLLs have good jitter performance, they consume more power, have long locking time and very large area. On the other hand, digital DLLs show very good performance in terms of power consumption and locking time. Digital bits to control the digitally controlled delay line (DCDL) [5]. Since the digital DLL is easy to scale down as the technology improves, its area can be decreased further for future advanced process technologies. However the main drawback of it is the limited resolution which results in worse jitter performance compared to analog DLLs due to the phase difference between input and output clocks. That is why the mixed-mode DLL was proposed to overcome these difficulties and combine both sides advantages into one system. It combines both DCDL and VCDL in its delay line, which is directly controlled by analogue and digital controllers. In that way it has both fast locking time and good phase resolution which leads to better jitter performance but does not solve the size and power consumption issue. In this paper, the proposed frequency multiplier based on mixed-mode DLL solves area and power consumption problems of conventional designs with relatively short locking time and good jitter performance in order to generate high output frequencies. Up to now most of the DLL with edge combiner can only generate output clock operating at 10 times of their input frequency due to the phase error between the input and output clocks and the mismatch problem between each cells in their delay lines [3]. However the proposed system overcomes this limitation and is able to generate output clock operating at 40 times of its input frequency with reasonable jitter and spectrum performance by introducing new types of delay cells combined of both digital and analog part with among their controllers. Since it has very small area and low power consumption, multiple of them can also be placed easily into a more complex system.

2. Architecture of Previous Frequency Multipliers

The DLL-based clock generator is composed of a DLL core and the proposed frequency multiplier, as shown in Fig. 1.

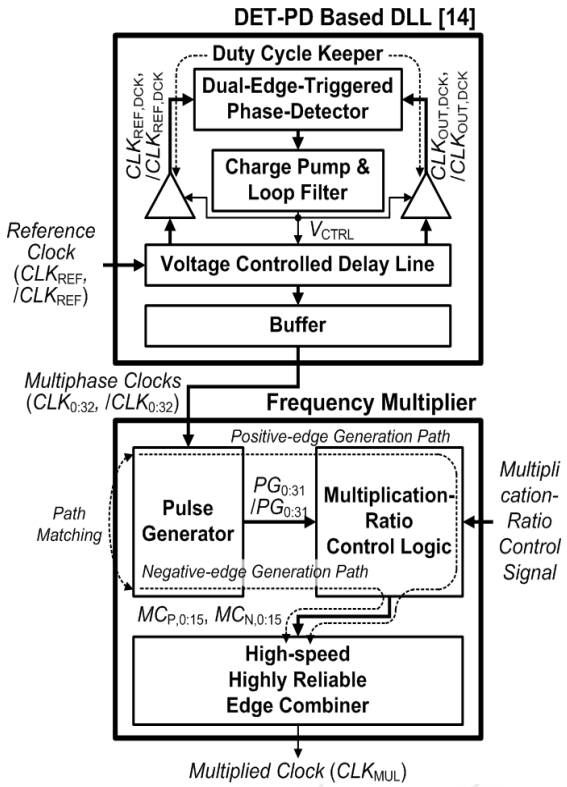

Figure 1: Structure of the DLL-based frequency multiplier.

To enhance the lock time, which is an important design parameter in the clock generator, a dual-edge-triggered phase- detector-based DLL core [7] is adopted. Similar to previous frequency multipliers, the proposed frequency multiplier is also composed of a pulse generator, a multiplication-ratio control logic, and an edge combiner.

The DLL-based clock generator is composed of a DLL core and a frequency multiplier, and the frequency multiplier is generally divided into two blocks: 1) a pulse generator and 2) an edge combiner. If variable frequency multiplication is required, a multiplication-ratio control logic is added.

3. Proposed frequency multiplier

Fig. 2 shows the block diagram of the proposed mixed-mode DLL. Whereas its digital part consists of a modified successive approximation register (MSAR) [2], a D-type flip-flop (DFF), frequency divider, and digitally controlled delay line (DCDL) for coarse tuning, the analogue part has a Phase Detector (PD), a Loop Filter, Voltage Controlled Delay Line (VCDL) for fine tuning. The edge combiner is the last part of this system which combines all phases coming from the delay line to generate high frequency output signals [3].

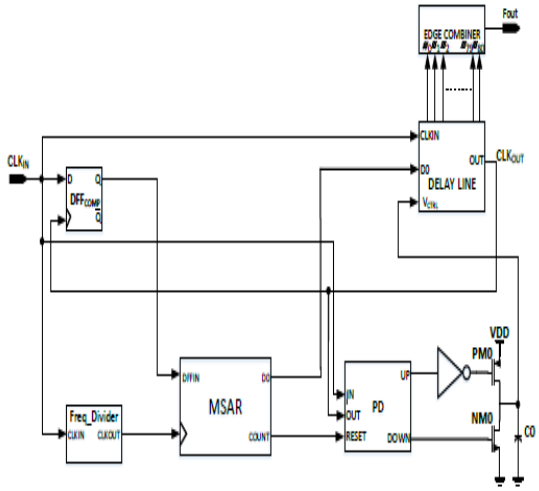

Figure 2: Block diagram of the proposed mixed-mode DLL.

When the input signal (CLKIN) rises, the phase difference between the output of the delay line (CLKOUT) and CLKIN is compared by the DFF and the result is sent to the MSAR to determine its digital control bit D0 to control the delay time of the DCDL in each delay cell for coarse tuning. After the digital part has finished, the Count signal rises to enable the PD. PD determines the remaining phase difference between CLKOUT and CLKIN, and sends UP or DOWN signal to the charge pump. These signals are used to charge or discharge the loop filter capacitor to determine Vctrl which adjusts the total delay time of the VCDL for fine tuning. When the phase difference between the two signals becomes so small that it falls into the dead-zone of the PD, it stops responding and Vctrl stays constant and the locking point is reached. All 80 equidistant phases are sent to the edge combiner to generate the output frequency.

A. Modified Successive Approximation Register (MSAR)

MSAR is the main controller of the digital part of the proposed DLL. It is used to control the DCDL. The MSAR consists of one MSAR unit which is assigned to single control bit (D0). The complete MSAR architecture is shown in Fig. 3. The other one OR gate and two DFFs are used to enable or disable the MSAR unit and trigger COUNT signal which will be used as a RESET function to enable PD.

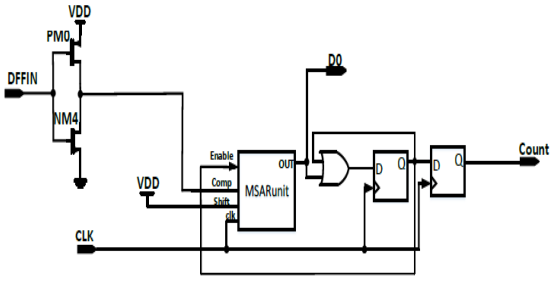

Figure 3: Schematic of the designed MSAR.

In the MSAR unit, which is shown in Fig. 4, the locking process is divided into two parts: At first, while the Enable signal is still 0, the shift signal which is connected to VDD in this case keeps the AND1 gate at logic 1 because OUTINVT and the inverted version of the Enable signals are still 1.

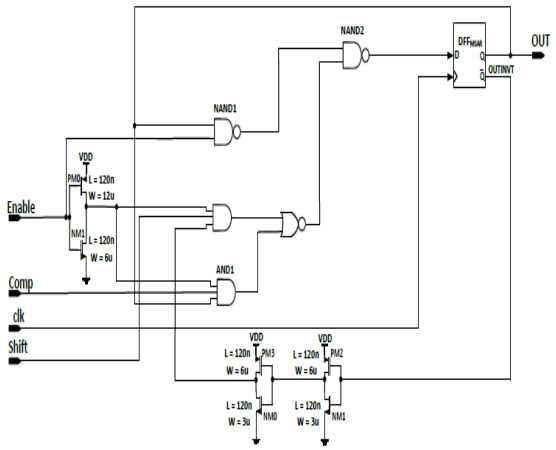

Figure 4: Signal flow graph for SR-FFT

Naturally, the NOR gate responses with logic 0.The output of the NAND1 gate is always 1 as long as Enable is 0. The output of the NOR gate keeps out of NAND2 gate at logic 1 which will be used as a data signal by the DFFMSAR. When the Clock signal rises, the output of the DFFMSAR becomes 1 and Comp which is sent by DFFCOMP by comparing CLKOUT and CLKIN is checked to whether the output should be kept at 1 or changed to 0. If Comp signal is at logic 1, that means output clock lags the input one so that the output of the DFFMSAR should be changed to 0 to decrease the total amount of the delay time in the DCDL. If Comp is 0, the input clock lags the output clock. Thus, control bit will remain the same at 1. After Enable is signal pulled up to VDD, the Comp signal will be disregarded and the output will be fixed as long as the input clock does not change.

B. Phase Detector (PD)

The Phase Detector (PD) is one of the most important parts of the proposed DLL. As shown in Fig. 5, the proposed architecture is a modified version of a conventional PD where the RESET signal comes from the MSAR as a COUNT signal to enable it. Until the RESET signal is pulled to VDD, the UP and DOWN signals are kept at logic 1 and 0, respectively. In that way Vctrl is kept at VDD via the charge pump and the loop filter capacitor which gives the minimum delay time in the VCDL. After the PD is enabled, Vctrl starts decreasing to adjust the total delay time to find the correct locking point.

Since the sensitivity of the PD determines the phase difference between the input and output clocks, the dead-zone of it is minimised to obtain good output jitter performance. Based on layout-extracted simulation results, the dead-zone of the PD is less than 1 ps for all four-corner cases.

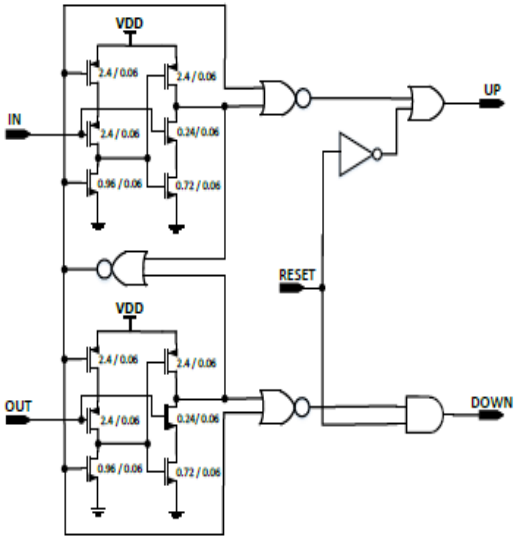

Figure 5: Schematic of the designed phase detector

C. Delay line

In terms of design, the delay line is the most critical part of the proposed DLL. It consists of 80 delay cells which gives equidistant phases to the edge combiner to generate the higher frequencies. The cell structure is shown in Fig. 5. Each cell has two different parts: a digital and analogue part i.e the DCDL and VCDL, respectively. For the DCDL part, a NAND-based delay line is preferred due to its advantage in terms of wide frequency range and small intrinsic delay time compared to an inverter-based one.Since one of two inputs of the NAND gates is at logic 1, When the control bit (D0) is 0, both of them start acting like a common inverter. In this situation, CLKIN follows the shortest path and the total delay will be two NAND gates and it is called minimum delay time. The rest of the NAND gates are not counted so they can not add any additional delay on CLKIN. If D0 is pulled up to 1 (VDD), since the input of the first NAND Gate is kept at logic 0 due to the inverted version of D0, its output will be at logic 1 and hence CLKIN is routed through the longest path which results in more than 3 times of the individual delay time of a single NAND gate.

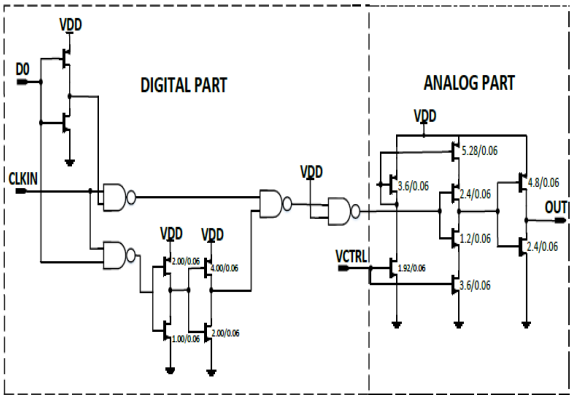

Figure 6: Schematic of one cell of the mixed Delay Line.

This delay directly depends on the number of NAND gates that are placed in each part. A larger number leads to a wider operating frequency range. The total delay time of the complete digital parts cannot exceed the period of the input signal. Therefore, there is always a residual phase difference

between the input and the output clocks after the digital part is settled.

Now the analogue part starts working to adjust the correct delay time to find the exact locking point. Vctrl controls the delay of the inverters in each cell via the biasing circuit. After the correct Vctrl is settled, the total delay time for one complete cell will be equal to half a period of the output frequency generated by the edge combiner.

4. Design and Simulation Results of Proposed Frequency Multiplier

A ultra-low-power frequency multiplier based on mixed-mode delay-locked-loop (DLL) in MOS technology was designed and simulated using Tanner EDA. The circuit design and simulation results are shown in Fig. 7(a), 7(b) and 7(c).

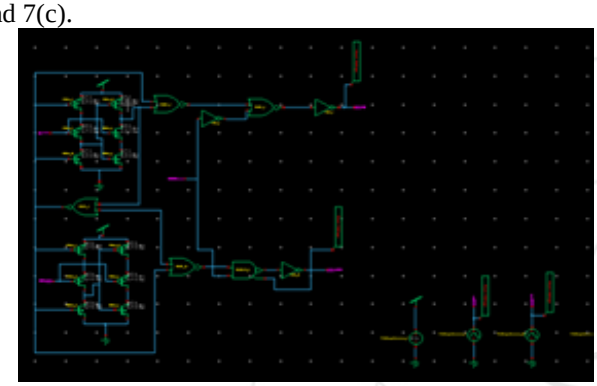

Figure 7: (a)

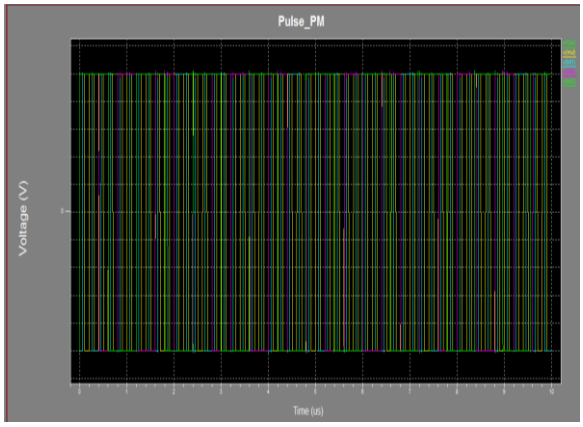

Figure 7 (b)

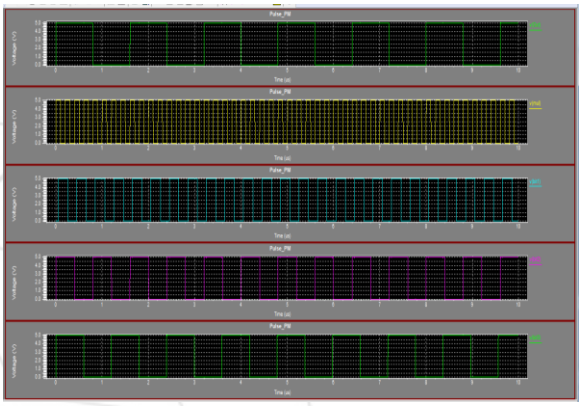

Figure 7(c)

Figure 7(b) & 7(c) Transient analysis of proposed mixed-mode DLL based frequency multiplier.

Table 1: Performance Summary And Comparison With Previous Works

Parameters	Existing System				Proposed System
	[6]	[7]	[8]	[9]	
V_{DD}	1.2 V	1.8 V	1.8 V	1.2 V	1.2 V
Multiplication ratio	4	4	8	16	32
Power Consumption of FM	4.8mW@2GHz	17mW@1.7GHz	17mW@1.7GHz	6.8mW@2GHz	4.5mW@4-6GHz
Jitter (rms/peak-to-peak)	3.2/19ps@1GHz	2.6/16.8ps@1.7GHz	N/A	1.9/13.6ps@3.3GHz	1.9/21ps @5GHz

Conclusion

The proposed mixed-mode DLL achieves low power consumption and good jitter performance because of the combination of both analogue and digital part of DLLs. While MSAR enables to achieve short-locking time and wide operating frequency with DCDL, analogue voltage (Vctrl) gives good resolution in overall delay line by controlling VCDL for fine tuning. It consumes 4.5mW power and can reach the lock state around 10 clock cycles. Its peak-to-peak jitter is 21 ps for 5 GHz generated output frequency (F_{OUT}).

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