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Low-Power and High–Performance Design Techniques for CMOS 4-bit ALU by using CPL, DPL, DVL

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Abstract: ***High-performance adder, subtractor and multiplier are one of the most fundamental components of ALU. This paper describes low-power, high performance design techniques such as :CPL, DPL, DVL for implementing adder, subtractor and multiplier circuit for achieving improved performance per watt or energy efficiency as well as silicon area efficiency. By considering all these aspect Dual value logic (DVL) is found to be the most energy efficient, high performance design technique which consumes low power, while the Double pass transistor logic (DPL) is shown to improve circuit performance at low supply voltage and Complementary pass-transistor logic (CPL) consume less chip area. By combining these techniques, the addition and subtraction time of a cmos ALU test chip is fabricated in 180 nm using cadence spectra simulator. These circuit design techniques and is capable of an simulation time of 1000ns at a supply voltage of 1.8v.***

Keywords: CPL, DPL, DVL, CMOS, figures of merit

1. Introduction

The in-corporative demand for low-power, high performance very large scale integration (VLSI) can be addressed at different design levels, such as the architecture, circuit design, layout design, and by selecting proper logic style[1]. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used become important, disallowing the formulation of universal rules for optimal logic styles. Investigations of logic styles reported in the literature so far, however, have mainly focused on particular logic cells, namely full-adders, full subtractor, multiplier used in some arithmetic circuits. In this work, these investigations are extended to a much wider set of logic gates, and with that, to arbitrary combinational circuits.

1.1Complementary CMOS Logic Style

Logic gates in conventional or complementary CMOS are built from an NMOS pull-down and a dual PMOS pull-up logic network. Any logic function can be accomplished by NMOS pull-down and PMOS pullup networks connected between the gate output and the power lines.

Advantages of the CMOS logic style are:

- Its strength against voltage scaling and transistor area (high noise margins) and thus reliable operation at low voltages and arbitrary (even minimal) transistor sizes.
- Input signals are connected to transistor gates only, which alleviates the usage and characterization of logic cells.
- The layout of CMOS gates is efficient due to the complementary transistor pairs.
- Basically, CMOS fulfills all the obligations regarding the ease-of-use of logic gates. [2]
- An often mentioned disadvantage of complementary CMOS is:
- The significant number of large PMOS transistors, resulting in high input loads. However, the best gate performance is achieved with a PMOS/NMOS width ratio of only about 1.5 (= $\sqrt{\frac{\mu n}{\mu p}}$), and this ratio will decrease even further in deep-submicron technologies, where the carrier drift velocities in NMOS and PMOS transistors become almost equal due to velocity saturation [2, 3].
- And also weak output driving capability due to series transistors in the output stage (delay increases).
- This, however, can be corrected by additional output buffers/inverters which are intrinsic in other logic styles series of up to three transistors between power line and gate output), thus disallowing the usage of pass-gates.

2. Logic Design and Its Technology

2.1. Using CMOS Technique:

2.1.1 CMOS 4- bit adder

Achieving design characteristics such as high performance with small size has been examined particularly for all logic designs mentioned here. The schematic diagram of a conventional static CMOS full adder cell is illustrated in figure 2.1.1.The signals noted with '-' are the complementary signals. The p-MOSFET network of each stage is the dual network of the n-MOSFET with minimum design risk. In this design serial nMOSFET or pMOSFET transistors (Fig. 2.1.1) are having increased width to obtain a reasonable conducting current for driving capacitive loads. This results in significant area overhead, and also causes high gate input capacitance leading to give more loads on previous stage. For which it results in increase in delay and high power dissipation.

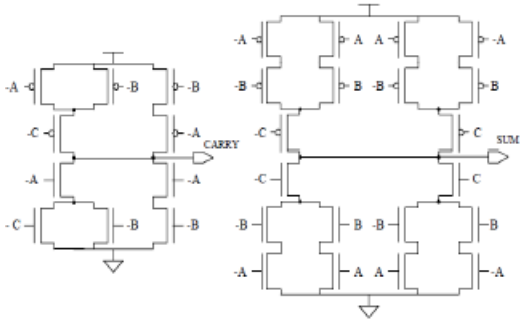

Figure 2.1.1: CMOS 4-bit adder

It is possible to design a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. Note that the first (and only the first) full adder may be replaced by a half adder.

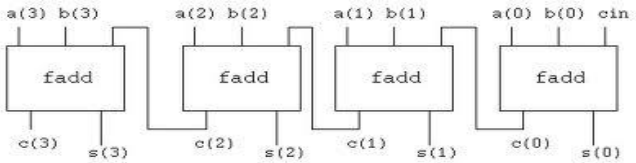

Figure 2.1. 2: basic block diagram of CMOS 4-bit adder

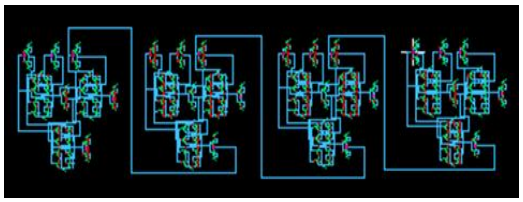

Figure 2.1.3: schematic of 4 -bit CMOS adder

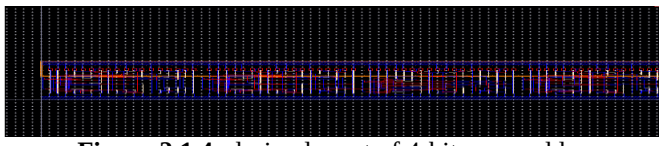

Figure 2.1.4: design layout of 4-bit cmos adder

2.1.2 CMOS 4-bit subtractor

It is possible to design a logical circuit using multiple full subtractors to subtract N-bit numbers. Each full subtractor inputs a D_{in}, which is the D_{out} of the previous subtractor. Note that the first (and only the first) full subtractor may be replaced by a half subtractor.

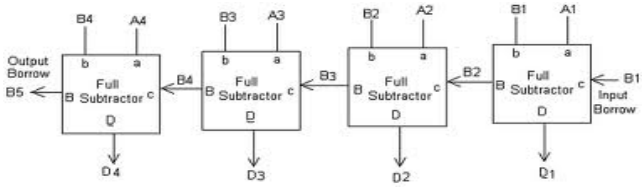

Figure 2.1.5: block diagram of 4-bit CMOS subtractor

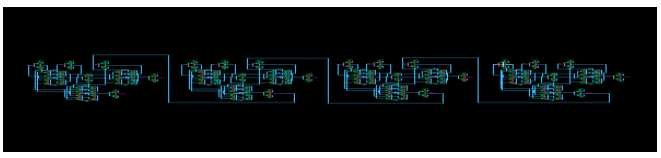

Figure 2.1.6: schematic of 4-bit CMOS subtractor

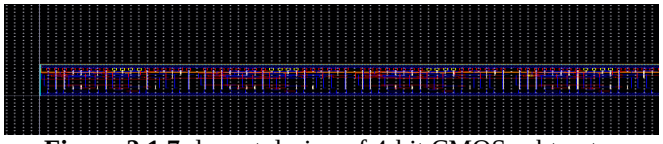

Figure 2.1.7: layout design of 4-bit CMOS subtractor

2.1.3 CMOS 4-bit multiplier

A binary multiplier is a circuit used to multiply two binary numbers. It is built using binary adders.A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of partial products, and then summing the partial products together. This process is similar to the method for conducting long multiplication on base-10 integers, but has been modified here for application to a base-2 (binary) numeral system.

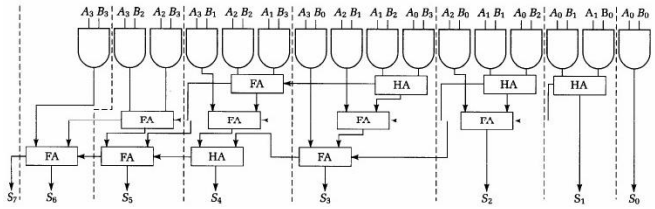

Figure 2.1.8: block diagram of 4×4 CMOS multiplier

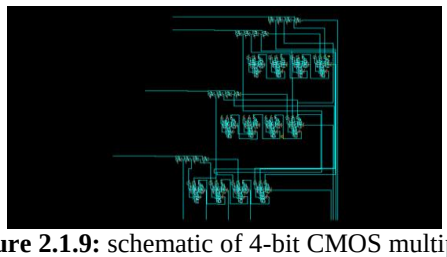

Figure 2.1.9: schematic of 4-bit CMOS multiplier

2.2. Using CPL Technique: (Complementary Pass-Transistor Logic)

Complementary pass-transistor logic consists of complementary inputs/outputs, a NMOS pass-transistor network, and CMOS output inverters. Due to its low input capacitance and reduced transistor count CPL has traditionally been applied to the arithmetic building blocks and results in high-speed operation.[4, 5]

Yho *et al.* described a **logic** technique in which a Boolean function is implemented using a network of nMOSFET pass transistors. When comparing with full static CPL implementation utilizes only half as many transistors and it avoids the design problem of appropriately sizing series connected transistors in the pull-up or pull-down planes**.** Therefore in CPL, when the outputs of the nMOSFET pass transistor network logically high, at vdd - vt**,** which results in the incomplete turn-off of pMOSFET's in the inverters.This results in a high static through current. To decrease the through current in CPL, a weak pMOSFET feedback device, is added across the output inverter stage to pull the output node of the pass-transistor network to full **Vdd.** However, this MOSFET pull-up increases the propagation delay of the CPL gate.[4, 6] A low-power high performance CPL can be created by combining the two CPL gates but it introduces increase in delay at the output.

2.2.1 CPL ADDER:

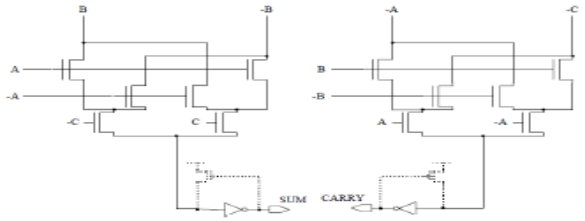

Figure 2.2.1: block diagram of CPL adder

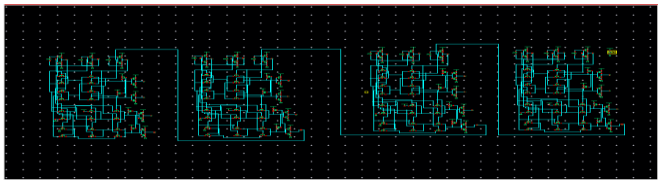

Figure 2.2.2: schematic of 4-bit CPL adder

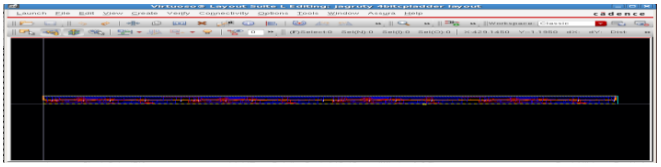

Figure 2.2.3: layout design of 4-bit CPL adder

For the implementation of logic functions, CPL uses only an n-MOSFET network, thus resulting in low input capacitance and high-speed operation [7]. The schematic diagram of the CPL full adder circuit is shown in figure 8. The high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, because of this, the signals have to be amplified by using CMOS inverters at the outputs.

2.2.2CPL Full Subtractor:

In this analysis, different sub micron feature size has been taken which gives a reduced power consumption and reduced power dissipation. The proposed subtractor circuit is very much useful for sensing the wanted/unwanted signal for the signal propagation.

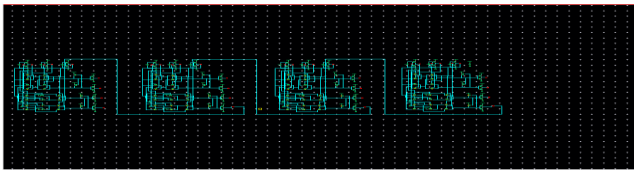

Figure 2.2.4: schematic of 4-bit CPL subtractor

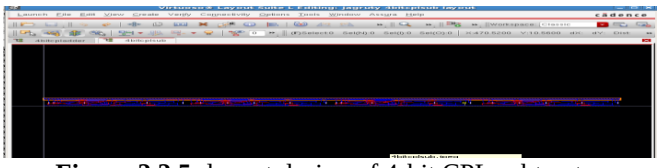

Figure 2.2.5: layout design of 4-bit CPL subtractor

2.2.3CPL Multiplier

This paper described a fast 4 X 4 multiplier using a new differential CMOS logic family, CPL. In CPL, differential logic is constructed without PMOS latchng load, achieving a speed more than twice as fast as conventional CMOS. The power dissipation is also lower due to lower input capacitance. The multiplier is the fastest ever re- ported at both 300 K and 77 K, proving that the half- micrometer CMOS technology fully utilizing CPL has a speed which is at least competitive with those of other fast devices with a much smaller power dissipation. [8]These results also exhibit that half-micrometer CMOS devices fully utilizing CPL have a performance potential of a 100-MHz repetition rate by carefully optimizing the multiplier architecture for high-speed operation.

The power dissipation of CPL multiplier was slightly more than CMOS multiplier due to having more number of transistors in the design. The performance of CMOS multiplier is more stabilized as the supply voltage is reduced when compared to other multipliers.[8, 9] At low voltages the CPL multiplier is next better in performance.

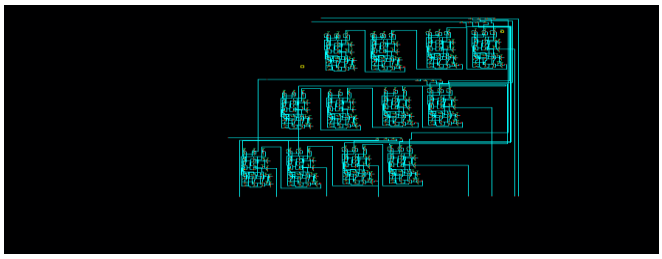

Figure 2.2.6: schematic of 4×4 CPL multiplier

2.3 Using DPL Technique (Double Pass-Transistor Logic)

In the DPL style both NMOS and PMOS logic networks are used in parallel. This provides full swing on the output signals and therefore circuit robustness is high. However, the number of transistors especially large PMOS transistors and the number of nodes is quite high (Area increases, Power increases), leading to considerable capacitive loads (Delay increase, Power increases). The combination of large PMOS makes DPL not competitive compared to other pass-transistor logic styles and to complementary CMOS.

A double pass-transistor logic (DPL) which is a modified version of CPL. DPL relieve the CPL problems of noise margin and speed degradation at low supply voltages. By having both pMOSFET and nMOSFET pass gates DPL implementation avoids the series sizing (and high gate capacitance) issues of the full static circuits as well as the nMOSFET threshold voltage drop issue of the CPL design. Similar to, by combining the two gates into a single gate (except that DPL does not need the feedback pMOSFET), a low-power DPL can be created.

The CPL gate consists of only NMOS transistors, resulting in low input capacitance and high-speed operation. However, the above problems are caused by the high output signal level which is lower than the supply voltage V& by the NMOS threshold voltage Vth**.** The normal way to avoid this is to use CMOS pass-transistor logic. Full-swing operation is attained by simply adding PMOS transistors in parallel with the NMOS transistors. However, this addition results in increased input capacitance.

2.3.1 DPL FULL ADDER:

We examined the speed advantage of the DPL gate using a full adder. The sum output portion consists of XOR/XNOR gates, a multiplexer, and a CMOS output buffer. The carry output portion consists of OR/NOR gates, AND/NAND gates, a multiplexer, and a CMOS output buffer. The bold lines shows the current paths for the outputs when A, B, and *C* are all low, for example, are shown in the figure. These current paths include two pass transistors, and there are two current paths for each output.

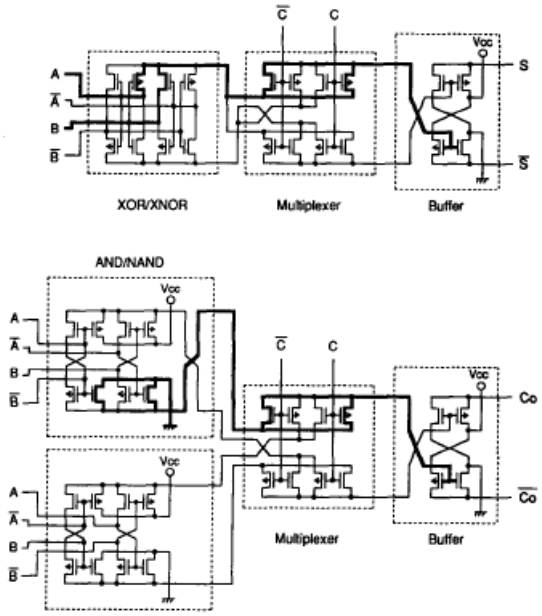

Figure 2.3.1: DPL full adder

The DPL full adder is as fast as CPL, 37% faster than CMOS and 18% faster than the conventional pass-transistor logic.[6, 7] As for the carry output delays *(C* - CO and A - CO*)* that determine the ALU speed, the DPL full adder is the fastest of all. Under these circumstances, the pass-transistor architectures show slightly higher power dissipation than CMOS because they have dual rail structure and double the load capacitance. The load capacitance determines which architecture dissipates the lowest power. In the DPL gate, there are two types of pass transistors: one is controlled by A and the other by B. The A-controlled pass transistors operate in the same way as CPL and CMOS. For the B-controlled pass transistors, when B is low, A is passed, and A is passed when B is high. As a result, there are always two current paths driving the buffer stage.

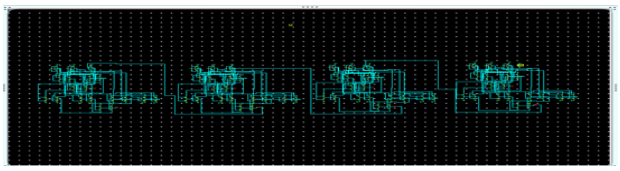

Figure 2.3.2: schematic of 4-bit DPL adder

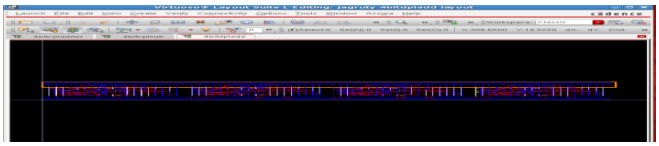

Figure 2.3.3: layout design of 4-bit DPL adder

2.3.2 DPL Subtractor:

With independently controlled transistor, the circuit design of DPL full subtractor has been demonstrated and the impact on figures of merit for power consumption, delay, leakage behavior and area of fabricated devices was presented. It was shown that the transistor count and the area respectively can be significantly reduced for logic gates; therefore the logic density per area increases. Where both transistor gates are on the same potential, offering less leakage current for low power, high performance circuits patterns. However the delay will be increased due to the lower drive current in the mode of operation.

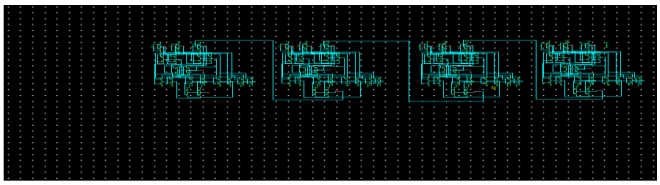

Figure 2.3.4: schematic of 4-bit DPL subtractor

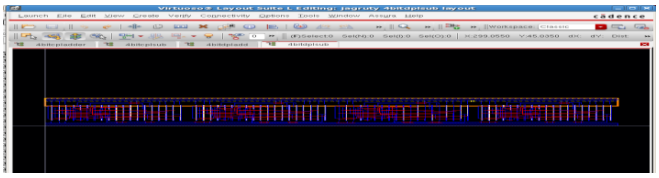

Figure 2.3.5: layout design of 4-bit DPL subtractor

2.3.3 DPL Multiplier:

One of the most heavily used circuits is the multiplier. The maximum delay of any operation determines the clock frequency. Therefore, the time consumed by the multiplier has a great effect on the speed of the processing element. The fastest known multiplier is the 'DPL multiplier'.

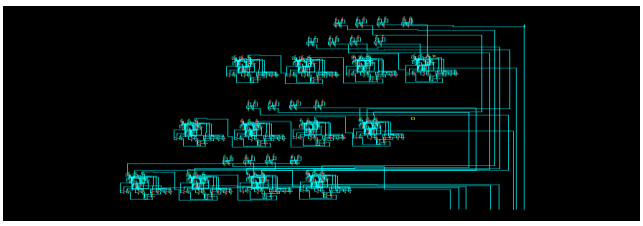

Figure 2.3.6: schematic of 4×4 DPL multiplier

2.4 Using DVL Technique: (Dual Value Logic)

The new logic gate represents an improvement over DPL family achieved by the elimination of the redundant branches and re-arrangement of signals. Disadvantages of DPL gates which are:

a) Compensation of speed degradation due to the use of PMOS transistors.
b) Straightforward full swing operation.

This simplification is achieved by in two steps:

1)Elimination of the redundant branches
2) Selection of the faster halves

DVL logic family has been developed which has advantages over standard CMOS as well as new pass transistor families such as DPL and CPL. However, the exact speed improvement is dependent on each particular circuit. The power consumption is also reduced for 30- 50% over conventional CMOS [9].Generation of DVL is supported by an automated synthesis tool based on the algorithm developed in the course of this work.

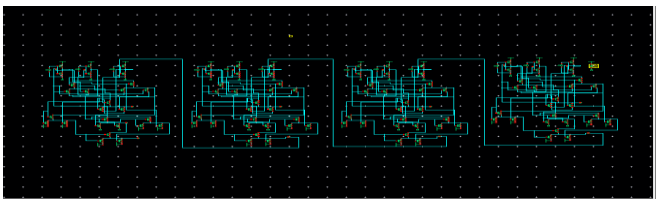

Figure 2.4.1: schematic of 4-bit DVL adder

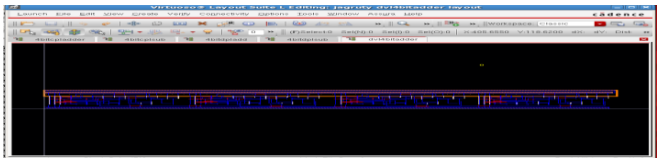

Figure 2.4.2: layout design of 4-bit DVL adder

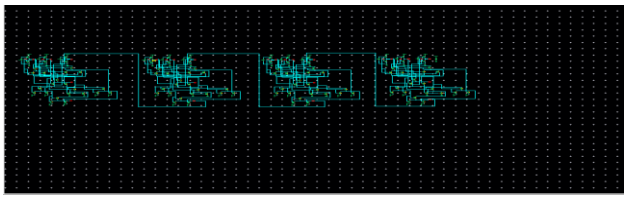

Figure 2.4.3: schematic of 4-bit DVL subtractor

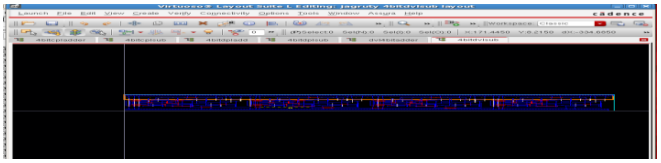

Figure 2.4.4: layout design of 4-bit DVL subtractor

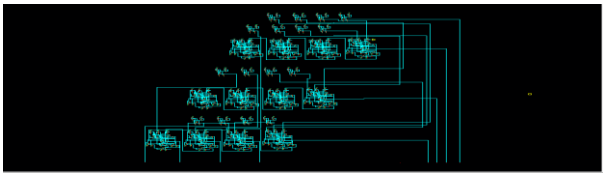

Figure 2.4.5: schematic of 4×4 DVL multiplier

3. Conclusion

Though using of transistors is fewer in CPL design than the other static and dynamic circuit styles to implement the same logic functions, the partial swing at the intermediate nodes results in more than 50% of the power being wasted. Reduction in the Vt of the nMOSFET pass transistors has been proposed to ease this problem [4], but at low supply voltages it will reduce the noise margin to an unacceptable level. An additional feedback pMOSFET device in the inverter stage combined with both the low-power CPL and the high performance version and the technique in, yields an improvement by a factor of 2.62 in energy efficiency and a 59% reduction in area, compared to the original CPL., All nodes in DPL have a full voltage swing and there is no static short-circuit current problem, because of the presence of both nMOSFET and pMOSFET devices. Dual current paths in DPL implementation also improve performance. With the similar techniques applied in CPL (except for feedback pMOSFET), the optimized DPL's energy efficiency is increased by a factor of 1.55 with a 58% area reduction when compared to the original DPL.

But DVL logic family has been developed which has advantages over standard CMOS as well as new pass transistor families such as CPL and DPL. However, the exact speed improvement is dependent on each particular circuit. The power consumption is also reduced for 30- 50% over conventional CMOS. Generation of DVL is supported by an automated synthesis tool based on the algorithm developed in the course of this work.

References

[1] Uming Ko; Balsara, P.T.; Wai Lee, "Low-power design techniques for high-performance CMOS adders, " Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.3, no.2, pp.327, 333, June 1995

[2] Suzuki, M.; Ohkubo, N.; Shinbo, T.; Yamanaka, T.; Shimizu, A.; Sasaki, K.; Nakagome, Y., "A 1.5-ns 32-b CMOS ALU in double pass-transistor logic, " Solid-State Circuits, IEEE Journal of, vol.28, no.11, pp.1145, 1151, Nov 1993

[3] Zimmermann, Reto; Fichtner, Wolfgang, "Low-power logic styles: CMOS versus pass-transistor logic, " Solid-State Circuits, IEEE Journal of, vol.32, no.7, pp.1079, 1090 doi: 10.1109/4.597298, Jul 1997

[4] Oklobdzija, V.G.; Duchene, B., "Pass-transistor dual value logic for low-power CMOS," VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical Papers, 1995 International Symposium on, vol., no., pp.341, 344, 31 May-2 Jun 1995

[5] A. P. Chandrakasan and R. W. Brodersen, Low Power Digital CMOS Design, Kluwer, Norwell, MA, 1995.

[6] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings", IEEE J. Solid-State Circuits, vol. 32, pp. 62–69, Jan. 1997

[7] C. Nagendra, R. M. Owens and M. J. Irwin, "Power-delay characteristics of CMOS **adders."** IEEE ***Trans. VU1 Syst.,*** vol 1, 1994

[8] J.M. Rabaey, *Digital Integrated Circuits*, PrenticeHall, Englewood Cliffs, N. Arora, *MOSFET Models for VLSI Circuit Simulation*, Springer-Verlag, Wien, Austria, 1993NJ, 1996*J. Solid-State Circuits*, vol. 22, pp. 528–532, Aug. 1987

[9] Santanu Maity, Bishnu Prasad De, Aditya Kr. Singh, "Design and implementation of low power high performance carry skip adder" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-1, Issue-4, April 2012