

Cascaded Multilevel Inverter with Reduced Number of Switches

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Abstract: A multilevel inverter is a power electronic device that is used for high voltage and high power applications. Now a days growth of interest in multilevel inverter has been increasing because of their enormous applications. In this paper new 15-level cascaded multilevel inverter is proposed and it requires less number of switches than the conventional topology. Therefore with less number of switches, there will be reduction in gate drive circuits. This inverter is comprised of a series connection of basic unit and is able to generate positive levels at the output. In-order to generate positive and negative levels at the output, an H-bridge will be added to this inverter. All the details regarding circuit schematic, modes of operation and simulation results are presented in this paper.

Keywords: Basic unit, cascaded multilevel inverter, H-bridge

1. Introduction

A Multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. Multilevel converters have become one of the most widely used power converters in electrical field. The basic level inverter starts from two level inverter. The two level inverter need to be operated at high frequency by using pulse width modulation (PWM) technique. Thus the switches undergo high switching losses. In-order to overcome this disadvantage multilevel inverter has been proposed. With increasing number of DC voltage sources in the input side, sinusoidal like waveform can be generated at the output. Compared to two-level inverter, the multilevel inverters have several advantages which mainly include: Reduction in the total harmonic distortion (THD), output waveform quality increases, lower switching losses, high efficiency, lower dv/dt and better electromagnetic capability.

Multilevel inverters are divided into three main categories: Diode Clamped multilevel inverter. The main concept of this inverter is to use diodes to limit the voltage stress on the power devices. The diode clamped inverter more focus on low frequency applications. It is also known as Neutral Point Clamped inverter. The voltage over each capacitor and each switch is V_{dc} . An 'n' level inverter needs (n-1) voltage sources, 2(n-1) switching devices and (n-1) (n-2) diodes.

Flying capacitor multilevel inverter: This inverter uses capacitors to limit the voltage stress on the power devices. The configuration of the flying capacitor multilevel inverter is similar to diode clamped multilevel inverter except that capacitors are used to divide the input DC voltage. The voltage over each capacitor and each switch is V_{dc} .

Cascaded multilevel inverter: A cascaded multilevel inverter is a series connections of H-bridge (single-phase, full-bridge) inverter. The output voltage is the sum of the voltage that is generated by each H-bridge. The number of output voltage levels are $2n+1$, where 'n' is the number of

cells. The advantage of cascaded multilevel inverter is that it needs less number of components compare to the Diode clamped or the flying capacitor.

These three multilevel inverters requires large number of switches, diodes, capacitors, voltage sources hence total harmonic distortion and electrical stress on device increases. In order to increases number of output levels by using less number of switches, a new basic unit is proposed. By connecting the basic units in series we will get cascaded multilevel inverter. These basic units generates only positive levels, to generate all positive and negative voltage levels at the output, H-bridge will be added to this inverter.

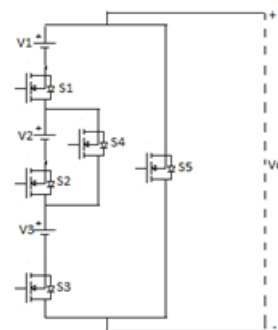


Figure 1: Proposed basic unit

Table I: On and Off States of the Switches in Proposed Basic Unit

States	Switches State					V_0
	S_1	S_2	S_3	S_4	S_5	
1	off	off	off	Off	on	0
2	on	off	on	On	off	V_1+V_2
3	on	on	on	Off	off	$V_1+V_2+V_3$

2. Proposed Topology

Figure 1 shows the proposed basic unit. It consists of three DC sources and five switches (MOSFETs). In the proposed basic unit switches (S_2, S_4), (S_1, S_3, S_4, S_5), and (S_1, S_2, S_3, S_5) should not turn simultaneously to avoid short circuit of dc voltage sources. The TABLE I shows the turn ON and OFF the switches. The basic unit

generates three voltage levels 0, (V_1+V_2) and $(V_1+V_2+V_3)$ at the output. By connecting 'n' number of basic units in series we will get cascaded multilevel inverter. This inverter will not generate voltage level V_1 , in order to generate V_1 voltage level, an additional DC voltage source with two switches are connected in series with proposed

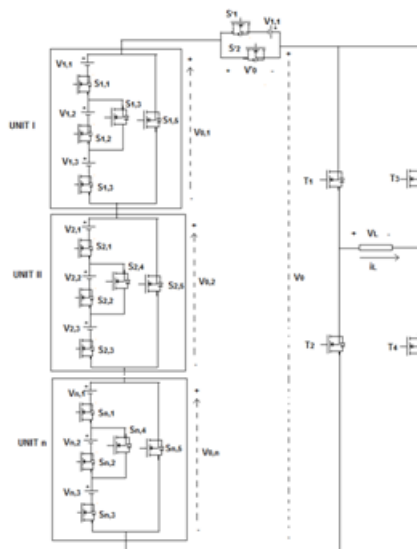


Figure 2: Developed topology

cascaded multilevel inverter. The output voltage of each basic unit is indicated as $V_{0,1}$, $V_{0,2}$, ..., $V_{0,n}$ and V_0 . The output voltage of proposed inverter is given by

$$V_0(t) = V_{0,1}(t) + V_{0,2}(t) + \dots + V_{0,n}(t) + V_0(t) \quad (1)$$

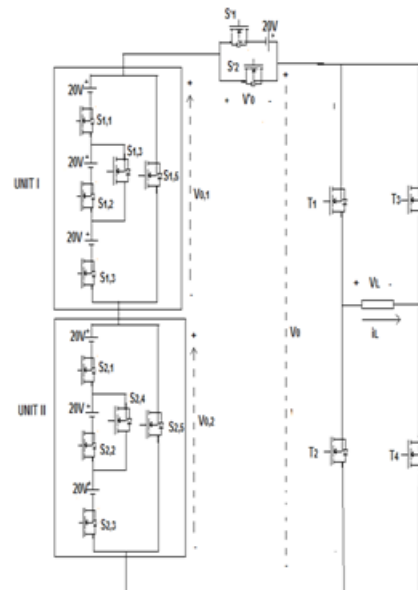


Figure 3: Proposed cascaded 15-level inverter

Table II: Output Voltage Levels Based On the On and Off State of the Switches

$S_{1,1}$	$S_{1,2}$	$S_{1,3}$	$S_{1,4}$	$S_{1,5}$	$S_{2,1}$	$S_{2,2}$	$S_{2,3}$	$S_{2,4}$	$S_{2,5}$	V_0
0	1	1	1	1	0	0	1	1	1	$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,2}+V_{2,3}$
0	1	1	1	1	0	0	1	0	1	$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,3}$
0	1	0	0	0	0	1	1	1	0	$V_{2,1}+V_{2,2}+V_{2,3}$
0	1	0	0	0	0	1	1	0	1	$V_{2,1}+V_{2,3}$
0	1	1	1	1	0	0	0	0	0	$V_{1,1}+V_{1,2}+V_{1,3}$
0	1	1	0	1	1	0	0	0	0	$V_{1,1}+V_{1,3}$
1	0	0	0	0	0	1	0	0	0	V_1
0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	0	$-V_1$
0	1	1	0	1	1	0	0	0	0	$-(V_{1,1}+V_{1,3})$
0	1	1	1	1	0	0	0	0	0	$-(V_{1,1}+V_{1,2}+V_{1,3})$
0	1	0	0	0	0	1	1	0	1	$-(V_{2,1}+V_{2,3})$
0	1	0	0	0	0	1	1	1	0	$-(V_{2,1}+V_{2,2}+V_{2,3})$
0	1	1	1	1	0	0	1	0	1	$-(V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,3})$
0	1	1	1	1	0	0	1	1	0	$-(V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,2}+V_{2,3})$

The proposed inverter generates only positive levels. Therefore H-bridge with four switches T_1 - T_4 is added to this proposed topology which is shown in Figure 2. If switches T_1 and T_4 are turned on the inverter will provide positive voltage V_0 at the output. If switches T_2 and T_3 are turned on the inverter will provide negative voltage $-V_0$ at the output.

For the proposed inverter the number of switches N_{switch} , the number of DC voltage sources N_{source} , number of levels N_{levels} and maximum output voltage V_{max} are given by the following equations.

$$N_{\text{switch}} = 5n+6 \quad (2)$$

$$N_{\text{source}} = 3n+1 \quad (3)$$

$$V_{\text{max}} = (3n+1) V_{\text{dc}} \quad (4)$$

$$N_{\text{levels}} = 6n+3 \quad (5)$$

Where 'n' is number of basic units used in the circuit. In proposed inverter unidirectional switches are used. The MOSFETs are used as switch; number of power diodes and driver circuit are equal to number of MOSFETs used in the circuit. In the proposed inverter, the amplitude of the output voltage is depends on the value of DC voltage sources used in the input. The complete work is done on cascaded multilevel inverter which is shown in Figure 3. This inverter consists of two proposed basic units and one series connected dc voltage source, it uses 7dc voltage

sources with amplitude of 20v and 12 unidirectional power switches. This inverter is able to generate 15-levels (seven positive levels, seven negative levels and one zero level). If switches T_1 and T_4 are turned on the inverter will provide positive voltage V_0 at the output. If switches T_2 and T_3 are turned on the inverter will provide negative

voltage $-V_0$ at the output. The maximum amplitude of output voltage is 140v. The output voltages based on the ON and OFF state of the switches which is shown in TABLE II. The modes of operations of the cascaded 15-level inverter are shown in Figure 4.

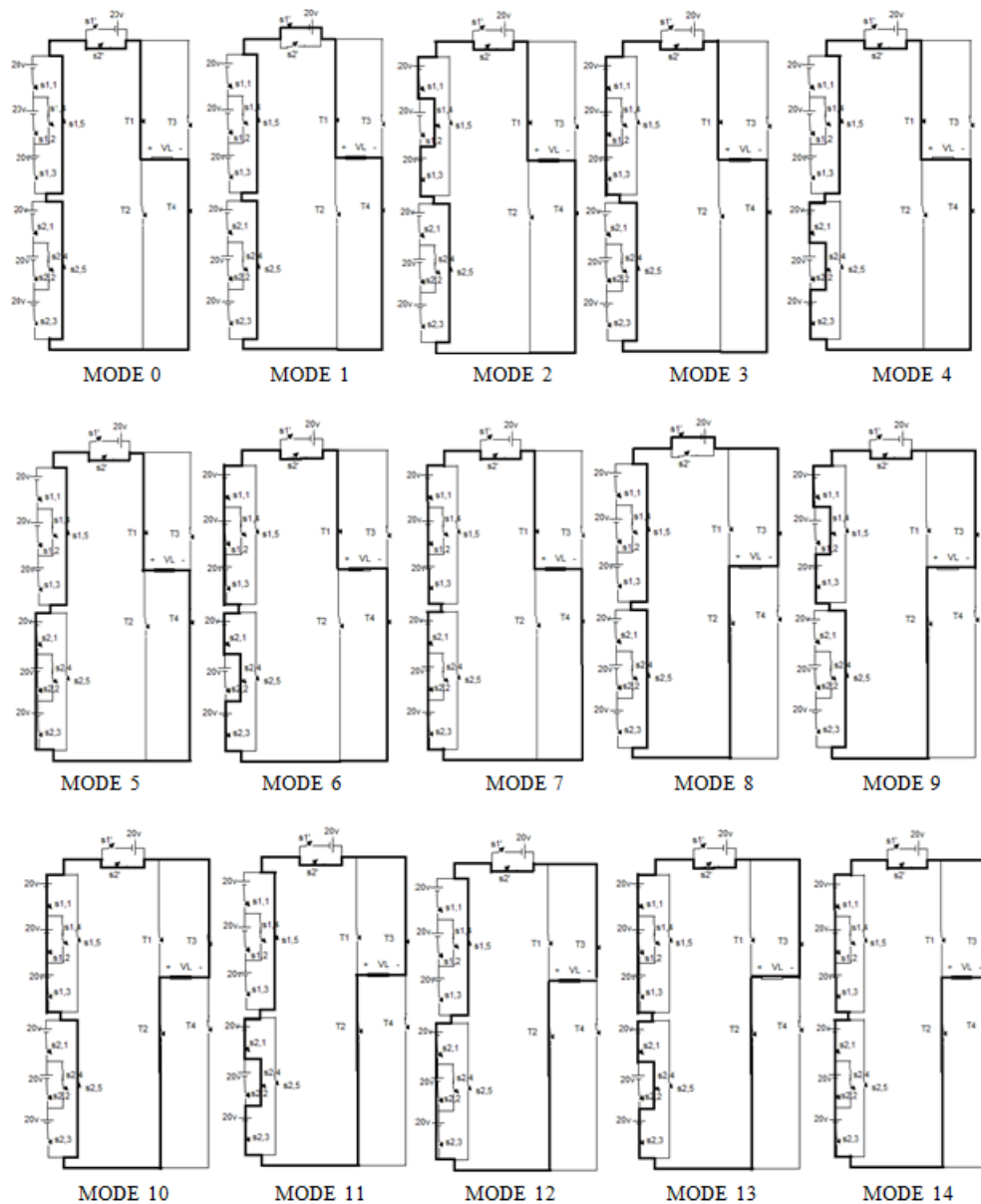


Figure 4: Modes of operation of the proposed cascaded 15-level inverter

3. Simulation Results

The simulation is being done in MATLAB/SIMULINK version 7.10.0.499(R2010a) for the proposed cascaded 15-level inverter by using 16 MOSFETs and 7 DC sources with V_{dc} as 20v shown in Fig 5. This inverter generates 15-levels (seven positive levels, seven negative levels and one zero level) with the maximum amplitude of 140v at the output.

Figure 6 and Figure 7 indicates that each basic unit generates the output voltage levels of 0v, 40v and 60V. Figure 8 shows the added dc voltage source that generates voltage level V1 with the amplitude of 20v. The proposed

inverter only generates positive levels at the output which is shown in Figure 9. By adding H-bridge, this inverter will generate all positive and negative voltage levels. Figure 10 shows waveforms of load voltage and load current. This inverter generates a 15-level step waveform with maximum amplitude of 140v.

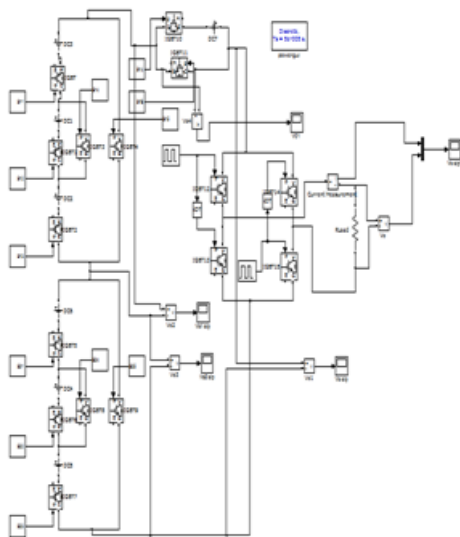


Figure 5: MATLAB/SIMULINK model of proposed cascaded 15-level inverter

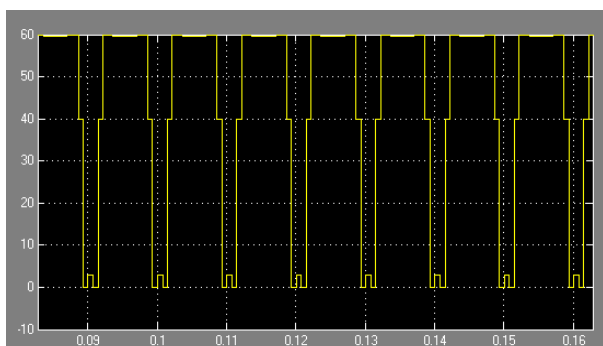


Figure 6: Output voltage waveform of basic unit 1 ($V_{o,1}$)

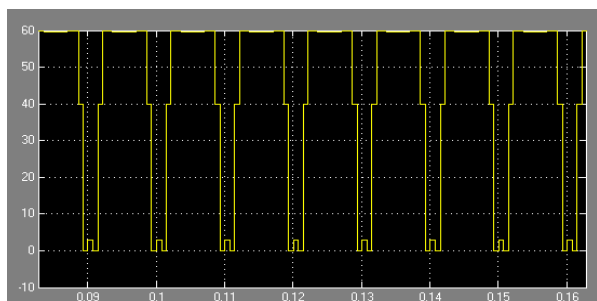


Figure 7: Output voltage waveform of basic unit 2 ($V_{o,2}$)

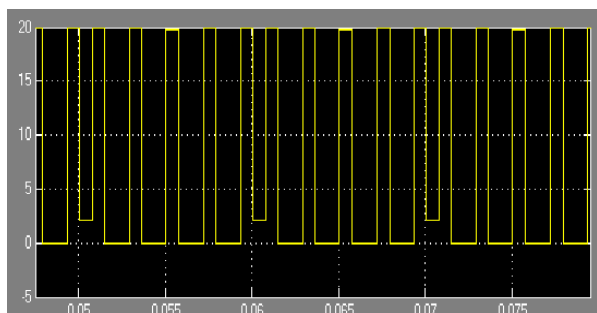


Figure 8: Output waveform added dc voltage source (V_0)

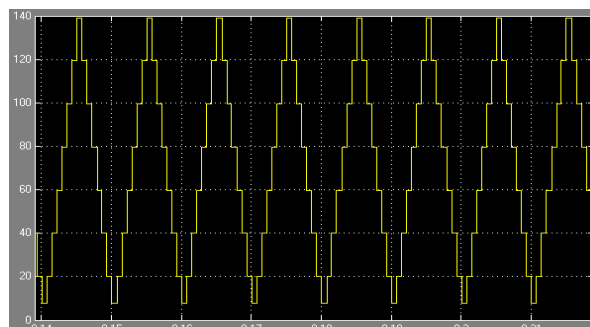


Figure 9: output voltage waveform (V_0)

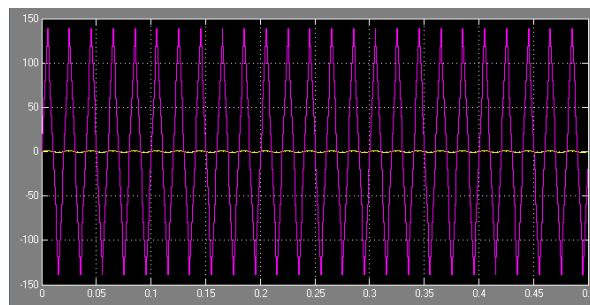


Figure 10: waveforms of load voltage and current

4. Conclusion

In this paper, new basic unit is proposed for cascaded multilevel inverter. This inverter only generates positive levels at the output. In-order to generate all positive and negative voltage levels, an H-bridge is added to the proposed inverter. The proposed topology requires less number of MOSFETs, power diodes, driver circuits, and DC voltage sources. That, leads to reduction in the installation space and total cost of the inverter. The Cascaded 15-level inverter is designed and simulated on MATLAB/SIMULINK. Finally, the performance of the developed cascaded 15-level inverter is verified by simulation results.

References

- [1] Ebrahim, "A single Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Switches" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 62, NO. 2, FEBRUARY 2015.
- [2] T V V S Lakshmi , Noby George, Umashankar S and Kothari D P "Cascaded seven level inverter with reduced number of switches using level shifting PWM technique" 2013 International Conference on Power, Energy and Control (ICPEC) 978-1-4673-6030-2/13/\$31.00 ©2013 IEEE.
- [3] Seyed Hossein Hosseini1, Amir Farakhor, and Saeideh Khadem Haghighian "New Cascaded Multilevel Inverter Topology with Reduced Number of Switches and Sources"
- [4] Ahmed Salem, Student Member, IEEE, Emad M. Ahmed, Member, IEEE, Mohamed Orabi, Senior Member, IEEE, and Mahrous Ahmed, Member, IEEE "New Three-Phase Symmetrical Multilevel Voltage Source Inverter" IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND

SYSTEMS, VOL. 5, NO. 3, SEPTEMBER 2015.

- [5] Rahul Nair, Mahalakshmi R, Dr. Sindhu Thampatty K.C.” Performance of Three Phase II-level Inverter with reduced number of switches using different PWM Techniques” 2015 IEEE International Conference on Technological Advancements in Power & Energy 978-1-4799-8280-6/15/\$31.00 ©20 15 IEEE.
- [6] R.Anand¹, M.Kamatchi² “A Fifteen Level Cascaded H-Bridge Multilevel Inverter with Reduced Number of Switches” International Journal of Advanced Engineering Research and Science (IJAERS) Vol-2, Issue-11, Nov- 2015] ISSN: 2349-6495.
- [7] Zahra Bayat, Ebrahim Babaei “A New Cascaded Multilevel Inverter with Reduced number of switches” IEEE Catalog Number: CFP121IJ-ART ISBN: 978-1-4673-0113-8/12/\$31.00 ©2012 IEEE.
- [8] Muhammad H. Rashid “Power electronics circuits, devices and application” text book.
- [9] Ahmed Salem, IEEE, Emad M. Ahmed, Mohamed Orabi, and Mahrous Ahmed “New Three-Phase Symmetrical Multilevel Voltage Source Inverter” IEEE Journal On Emerging And Selected Topics In Circuits And Systems, Vol. 5, No. 3, September 2015.
- [10] Seyed Hossein Hosseini¹, Amir Farakh², and Saeideh Khadem Haghighian “New Cascaded Multilevel Inverter Topology with Reduced Number of Switches and Sources”