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Towards New Error Detection Circuits Using QCA

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Abstract: ***Quantum-dot cellular automata nanotechnology has achieved world-wide attention for their prominent features such as low power consumption, small size and fast switching speed as compared to the conventional CMOS transistors. Reliable data transmission over telecommunication network systems is an increasing demand at nano-scale. Several QCA based nano-devices have been implemented to detect errors during data transmission. In this paper, an efficient even parity generator and checker has been proposed using QCA. The simplest and effective technique used to detect errors in the message word. An optimal number of QCA cells have been used for the design and implementation of the parity logic circuits. A detailed performance evaluation analysis is performed in different aspects to authenticate the proposed bit preservation circuits has superb performance in comparison to previously reported works. The functionality and simulation results of the proposed circuits have been verified using QCADesigner tool Ver. 2.0.3.***

Keywords: Nanotechnology, Transmission, Error, Parity Generator, Parity Checker.

1. Introduction

Very Large Integrated Circuits (VLSI) technology has encountered serious challenges in terms of power consumption, doping fluctuations, and leakage current [1]. These deficiencies have led to significant efforts to find appropriate alternatives and among the proposed solutions, nano-scale technologies such Nano-wire Field-effect Transistors (NWFETs), single electron tunneling (SET) and Quantum Cellular Automata (QCA) have received considerable attention [2-3].

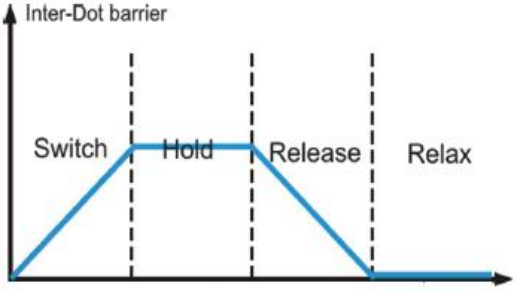
QCA has achieved significant interest to researchers due to its attractive characteristics such as high device density, low power consumption, and small dimensions. QCA circuits are made up of QCA cells; each cell consists of four quantum dots, in which two electrons are loaded antipodal sides. The binary information is encoded by these two electrons rather than current or voltage levels (CMOS is current based). Based on various arrangements of the QCA cells widespread range of QCA logic gates and circuit designs are realizable [4-10].

Parity bit generator/checker is one of the most effective techniques for error detection in data transmission networks. It is the simplest method for checking binary data; it is employed in communication for reliable data transmission operations. Parity is prone to errors due to its status as a "pass-fail" sum-based method for error detection. Several, architectures of parity preservation circuits have been proposed in [11-14]. Recently a new serial communication architecture has been presented in [15]. Hence, designing efficient QCA parity generator and checker is a key issue in communication for reliable data transmission.

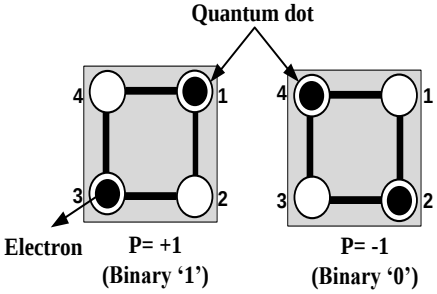
In this paper, we propose an efficient QCA based odd and even parity, generator, and parity checker using explicit interactions between QCA cells, ignoring the conventional designing methods. A detailed comparison with regard to various characteristics of these designs is also presented. Keeping in view the efficiency of data preservation circuits, an optimal use of QCA cell counts, area, and clock delay have been used. The most frequent components used for designing even parity, generator and checker is 3-input Exclusive-OR (TIEO) [3] based 2-input XOR. The circuit functionality of the proposed parity, generator and checker has been testified using QCADesigner tool.

2. QCA Background

QCA digital systems and methods are generalized in [16]. Coulombic energy between neighboring cells is used for circuit operation. No voltage or current is used in QCA. QCA clock is required for circuit synchronization [17-18], as shown in Fig. 1(a). Each clock has four phases (switch, Hold, Release and Relax) is required for control signals and circuit synchronizations. In QCA cell polarization is used to encode information [1-2], as shown in Fig. 1(b). QCA cells act as wire, is used for signal propagation [2-4], as shown in Fig. 1(c). The 3-input Memory gate and Inverter is used for designing of QCA circuits and is based on new processing technique [1-2], as shown in Fig. 1(d) & (e). Two-input logic AND gate and OR gate can be implemented by programming Majority gate. AND gate & OR gate can be implementing by setting one- input permanently to a "0" or "1" value of Majority gate, respectively [1-2].



(a)



(b)

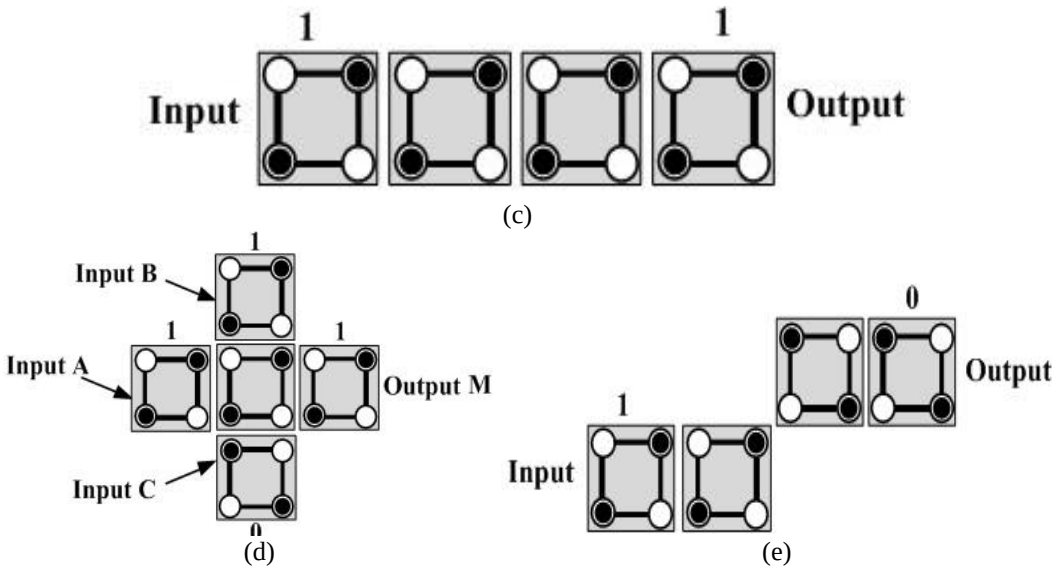


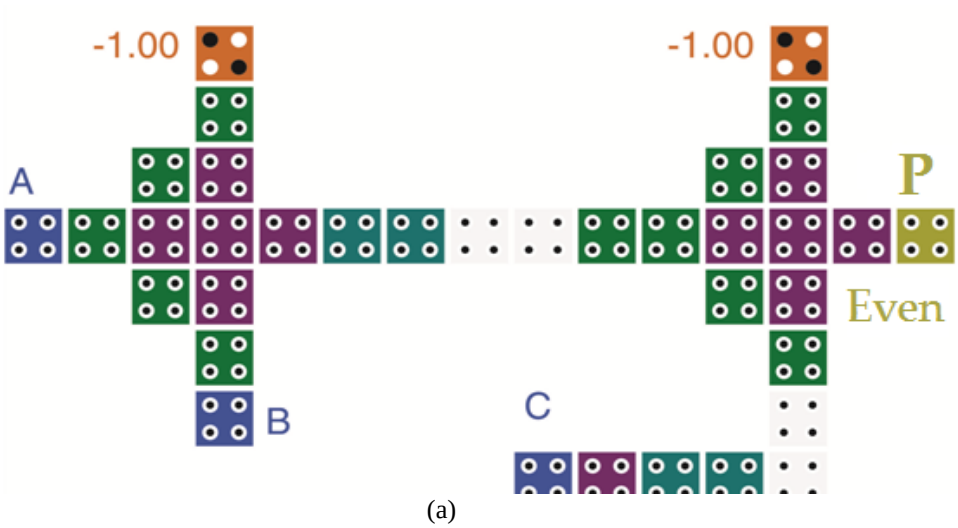
Figure 1: QCA terminology: (a) Clock (b) Two polar states (c) QCA wire (d) 3-input majority gate (e) Inverter.

3. QCA Implementations

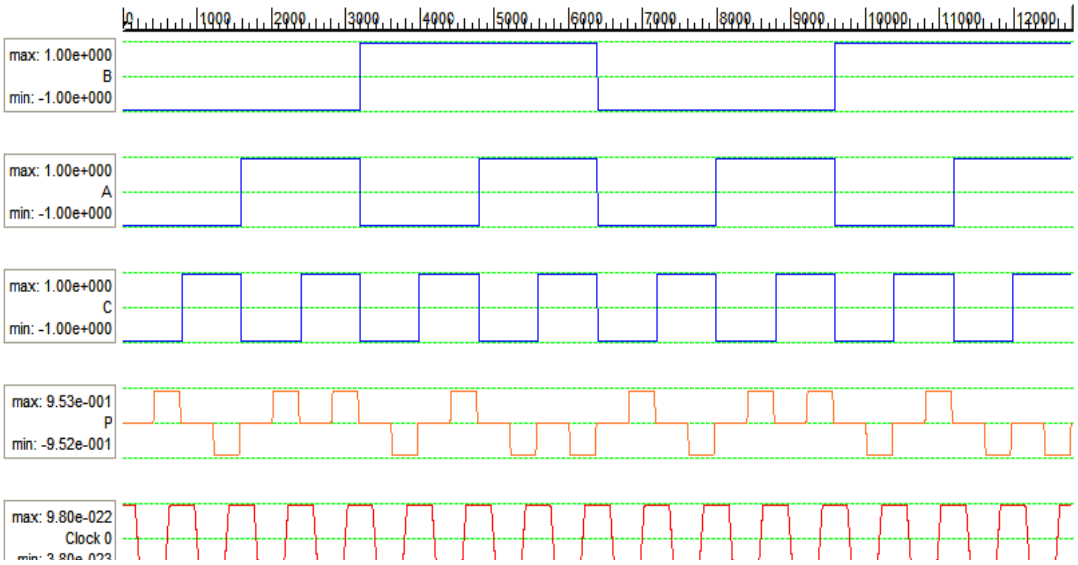
3.1 The QCA Layout of Even Parity Generator/Checker

The Parity bit (for Even parity) is added to a data word in order to enable error detection over a noisy communication channel. XOR gates are popularly used to generate and check parity bits. There is an ever increasing demand for reliable data transmission over telecommunication networking systems. In this work proposed QCA 2-nput XOR gates based on TIEO [3] have been used in parity generator and checker. It generates the parity bit 'P" at the transmitter. This bit is added to the data word in order to make the number of 1's Even for Even parity.

The proposed QCA-parity generator obviously works at nano-scale. The QCA layout of the proposed Parity Generator is shown in Fig. 2(a). It uses circuit complexity of 36 cells, an area of 0.05 um^2 and latency of 1.5 clock delays. The simulation results are shown in Fig. 2(b).



(a)



(b)

Figure 2: (a) The QCA layout of even parity generator (b) Simulation results.

The parity bit along with the data word is transmitted to the receiver. At the receiver, the parity of the received data word is again calculated and then compared with parity bit received. In the case of a mismatch, an error is assumed to have occurred in the original data word.

The QCA layout of Even Parity Checker is shown in Fig. 2(c). It uses circuit complexity of 50 QCA cells, area 0.07 um^2 and latency 1.5 clock delays. Fig. 2(d) outlines the simulation results of the proposed Parity Checker.

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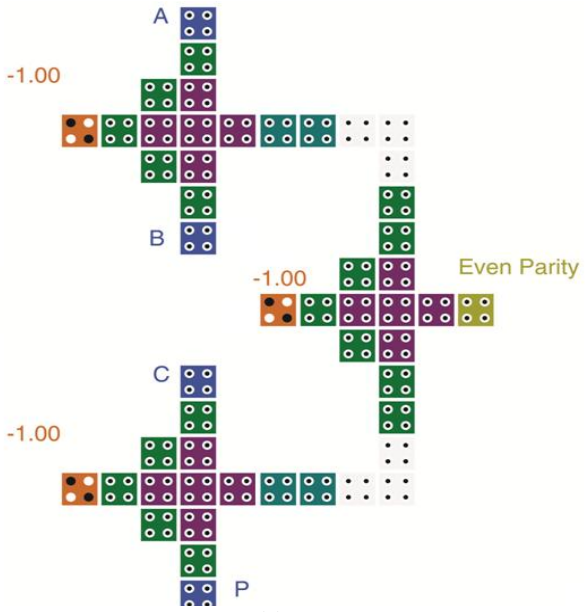
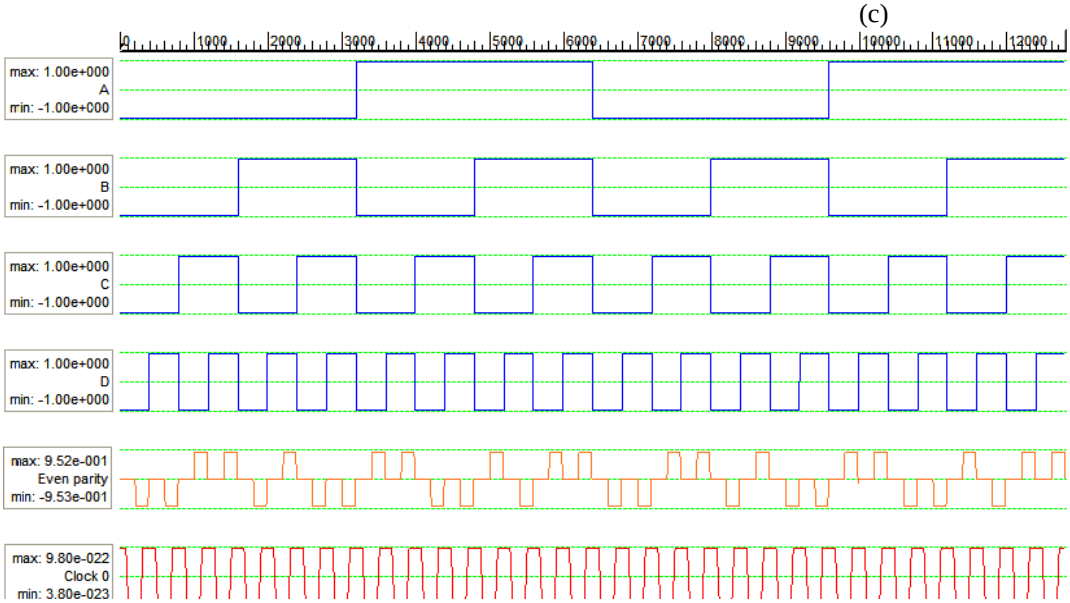


(c)



(d)

Figure 2: (c) The QCA layout of Even Parity Checker (d) Simulation results.

In order to prove the merit and advantage of the proposed Even Parity Generator/Checker, a comparison of the proposed circuits has been performed (with regards to various QCA circuit parameters) with the conventional QCA Even circuits available in the literature [11-14]. The QCA-circuit parameters including area, latency and circuit complexity have been chosen for the said comparison. The comparison of circuit parameters of the proposed Even Parity Generators/Checkers circuits with those of such circuits available in various works of literatures has been presented in Table-1.It can be observed from the Table-1 that the proposed even parity generators/checker has a general advantage in terms of area, clock delays, and circuit complexity over the existing such circuits.

Table 1: Comparison Parameters of Even Parity Generators/Checkers

Structures	*References*	*Circuit Parameters*		
		Complexity (No of cells)	*Area (um^2)*	*Latency (clock delay)*
Conventional Even Parity Generator/Checker	PG [11]	64	0.09	2.75
	PC [11]	94	0.11	1.75
	PC [11]	94	0.13	1.75
	PG [12]	99	0.17	2
	PC [12]	145	0.28	3
	PG [13]	60	52488 nm =0.052488	2
	PC [13]	117	135432nm =0.135432	2.25
	PG [14]	135	739.23nm X 291.59nm= 0.2155520757	Simple
	PC [14]	197	602.13nmX487.69nm = 0.2936527797	Simple
Proposed Even Parity Generator/Checker	**PG Fig. 2(a)**	**36**	**0.05**	**1.5**
	PC Fig. 2(c)	**50**	**0.07**	**1.5**

* Parity Generator (PG) and Parity Checker (PC).

4. Conclusion

In the present research work, we have proposed a new even parity generator and checker using QCA. A simple and an effective technique to detect errors in telecommunication network systems at the nano-scale. The proposed party generator and checker have been achieved significant improvements in terms of circuit parameters including area, clock delays and circuit complexity than conventional counterparts. The design and simulation results of the proposed work have been verified using QCADesigner tool ver. 2.0.3.

References

[1] C. S. Lent, P. D. Tougaw, W. Porod, G. H. Bernstein, “Quantum cellular automata,” Nanotechnology, 4 , 49-57, **1993.**

[2] P. D. Tougaw and C.S. Lent. “Logical devices implemented using quantum cellular automata,” J. Appl. Phys. 75, 1818, 1994.

[3] Firdous Ahmad, Ghulam Mohiuddin Bhat, Hossein Khademolhosseini, Saeid Azimi, Shaahin Angizi, Keivan Navi, “Towards single layer quantum-dot cellular automata adders based on explicit interaction of cells,” Journal of Computational Science, vol. 16, pp. 8–15, September 2016.

[4] Timler, C. S. Lent, “Power gain and dissipation in quantum dot cellular automata,” J. Appl. Phys., 91, 823–830, **2002.**

[5] S. Angizi, S. Sarmadi, S. Sayedsalehi, and K. Navi, “Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata,” Microelectronics Journal, vol. 46, pp. 43-51, **2015.**

[6] S. Hashemi, R. Farazkish, and K. Navi, “New quantum dot cellular automata cell arrangements,” Journal of Computational and Theoretical Nanoscience, vol. 10, no. 4, pp. 798–809, **2013.**

[7] B. Sen, A. Nag, A. De, and B. K. Sikdar, "Towards the hierarchical design of multilayer QCA logic circuit," *Journal of Computational Science*, **2015.**

[8] S. Angizi, F. Danehdaran, S. Sarmadi, S. Sheikhfaal, N. Bagherzadeh, and K. Navi, "An Ultra-High Speed and Low Complexity Quantum-Dot Cellular Automata Full Adder," *Journal of Low Power Electronics*, vol. 11, pp. 173-180, **2015.**

[9] S. Sheikhfaal, K. Navi, S. Angizi, and A. H. Navin, "Designing high speed sequential circuits by quantum-dot cellular automata: Memory cell and counter study," *Quantum Matter*, vol. 4, pp. 190-197, **2015.**

[10] S. Sayedsalehi, M. R. Azghadi, S. Angizi, and K. Navi, "Restoring and non-restoring array divider designs in quantum-dot cellular automata," *Information sciences*, vol. 311, pp. 86-101, 2015.

[11] F. Ahmad, P. Z. Ahmad, and G. M. din Bhat, Design and analysis of odd and even-parity generators and checkers using quantum-dot cellular automata (QCA), Computing for Sustainable Global Development, IEEE, 187 – 194, New Delhi, March **2015.**

[12] M R. Beigh, M. Mustafa, “Design and implementations of quantum-dot cellular automata base novel Parity generator and checker circuits with minimum cell complexity and cell count,” Indian Journal of Pure & Applied Physics, vol. 51, pp. 60- 66, **2013.**

[13] Santanu Santra, Utpal Roy, “Design and Optimization of Parity Generator and Parity Checker Based On Quantum-dot Cellular Automata,” World Academy of Science, Engineering and Technology International Journal of Computer, Information, Systems and Control Engineering, vol. 8, no. 3, **2014.**

[14] P.Ilanchezhian, Dr.R.M.S.Parvathi, “Analysis and Design of Modified Parity Generator and Parity Checker using Quantum Dot Cellular Automata,” International Journal of Latest Trends in Engineering and Technology (IJLTET), Vol. 2, Issue 4 July **2013.**

[15] J.C. Das, D. De, Quantum-dot cellular automata based reversible low power parity generator and parity checker design for nanocommunication, Frontiers Inf Technol Electronic Eng. 17 224–236. 2016.
[16] F. Lombardi, J. Huang, X. Ma, M. Momenzadeh, M. Ottavi, L. Schiano, and V. Vankamamidi, Design and Test of Digital Circuits by Quantum-Dot Cellular Automata, F. Lombardi and J. Huang, Eds., Norwood, MA, 2008.
[17] Landauer, R., "Irreversibility and heat generation in the computing process. IBM journal of research and development, 5(3), 183-191, 1961.
[18] C. H. Bennett, "Logical reversibility of computation," IBM journal of Research and Development, 17(6), 525-532,1973.