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Design of One Stage Operational Transconductance Amplifiers at 65nm and 90 nm for Low Power Applications

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Abstract: ***A novel design technique for one stage CMOS Operational Transconductance Amplifier (OTA) for nanometer application. The idea is to achieve improved gain-bandwidth product (GBW), DC gain, settling time, and slew rate. This is well known that, these parameters are important for high frequency, fast settling applications, such as switched capacitor filters, analog to digital converters, oscillator. They have vast application areas through analog design field, implemented in 32nm process parameters. We have designed OTAs for 65nm and 90 nm technologies. DC gain, Average Power, Bandwidth, Output resistance, Phase Margins and Unity Gain Frequency have been simulated for both 65nm and 90 nm OTAs. At 65nm technology node DC gain (24.6 dB), Average Power(24.17uW), Bandwidth(1.16 MHz), Output resistance(7.7K-Ohms), Phase Margin(86.760) and Unity Gain Frequency(18.6MHz). At 90nm technology node, DC gain (29.3 dB), Average Power(14.54uW), Bandwidth(0.43 MHz), Output resistance(12 K-Ohms), Phase Margin(88.200) and Unity Gain Frequency(11.32MHz) are simulated using Hspice.***

Keywords: OTA, CMOS analog integrated circuits, operational amplifier

1. Introduction

The OTA is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impendence differential input stage and that it may be used with negative feedback. Portable electronics with low- voltage operation finds big markets . However, the threshold voltage is not reduced proportionally with the supply voltage. Thus, the threshold voltage is becoming a restraint for many analog circuits. Some special techniques are used to overcome the size of the threshold voltage, e.g. Floating gate transistors , bulk-driven transistors , continuous-time filters and low threshold transistors. They suffer from several drawbacks or need special fabrication steps, which increases the cost. It is preferred to implement low- voltage circuits using a standard CMOS technology. Operational transconductance amplifier (OTA) is one of the important analog signal processing block and has almost replaced operational amplifier [1-2]. The advantages of an OTA include more controlled nature due to presence of an extra control input, large bandwidth, large dynamic range and no excess phase issues. The flexibility and the tunability are the biggest advantages which are responsible for the extended application domain of an OTA. Further, with OTA, the realization of high integration level integrated circuits is highly possible [3-4].Since the output of an OTA is derived as the current, the output impedance of the OTA is very high (ideally infinity). Since gm, of the OTA is dependent on the I_{bis} current, the output characteristics of the OTA may be controlled externally by the bias current (I_{bis}). It adds new dimension to design and applications of OTA circuit. A widely used approach in design of low voltage circuits is to reduce the number of transistors between the supply voltage and ground. This approach led to the design of an OTA topology depicted in [5] known as basic transconductor stage, which is not only very simple in design but also works at really low voltages. However, the problems with the conventional OTA are related to gain and speed degradations in submicron range [6-10].

The Operation of a Conventional One – Stage CMOS OTA

Fig. 1 shows a conventional one stage CMOS OTA. The dc open loop gain, gain bandwidth product, and high impedance pole are

$$A_{OL} = Kg_{m1,2}\,(r_{o4} \,//\, r_{o5}) \quad (1)$$

$$GBW = \frac{Kg_{m1,2}}{2\pi C_L} \quad (2)$$

And

$$f_{pout} = \frac{1}{2\pi C_L\,(r_{o4} \,//\, r_{o5})} \quad (3)$$

respectively, where $g_{m1,2}$ is the small-signal transconductance of M_1 and M_2, C_L , $r_{o6}//r_{08}$ are the equivalent capacitance and resistance at the output node, K is the mirror current factor between core stage and shell stage. The internal poles at node A and B are

$$f_{pA,B} = \frac{1}{2\pi C_{A,B} R_{A,B}} = \frac{g_{m31,41}}{2\pi C_{gs31,41}\,(K+1)} \quad (4)$$

where

$$C_{A,B} \approx C_{gs31,41} + C_{gs3,4}$$

are the parasitic capacitances at nodes A and B, respectively. Typically the condition 2GBW< $f_{pA,B}$ is used in practice to enforce enough phase margin.

The quiescent current flowing through transistors M_1, M_2, M_3, and M_4 and through M_5 and M_6 are $I_{bias}/2$ and $KI_{bias}/2$ respectively. Therefore the maximum current delivered to the load is KI_{bias} and slew rate is therefore, given

$$SR = \frac{KI_{bias}}{C_L} \quad (5)$$

Or

$$SR = \frac{I_{bias}\ (2\pi GBW\ )}{g_{m1,2}} \quad (6)$$

Hence, for a given $C_{L,}$ to avoid limitation of settling time by slew rate K and/or I_{Bias} should be large. An increase in I_{Bias} leads to the same increase in static power dissipation. Larger K values not only increase slew rate, but also GBW and current efficiency [8,9].

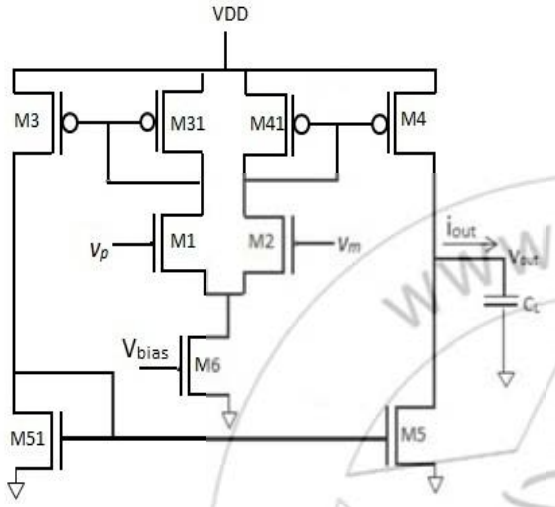

Figure 1: One Stage Operational Transconductance Amplifiers

Table 1: OTA Performance at 65nm and 90nm technology nodes

S. No.	Parameters	OTA *@ 65nm*	OTA *@ 90nm*
1	DC Gain in dB	24.6 dB	29.3 dB
2	Band width	1.16 MHz	0.43 MHz
3	Phase Margin	86.76^0	88.20^0
5	Average Power	24.17uW	14.54uW
6	Output Resistance	7.7K-Ohms	12 K-Ohms
7	Unity Gain Frequency	18.6MHz	11.32MHz

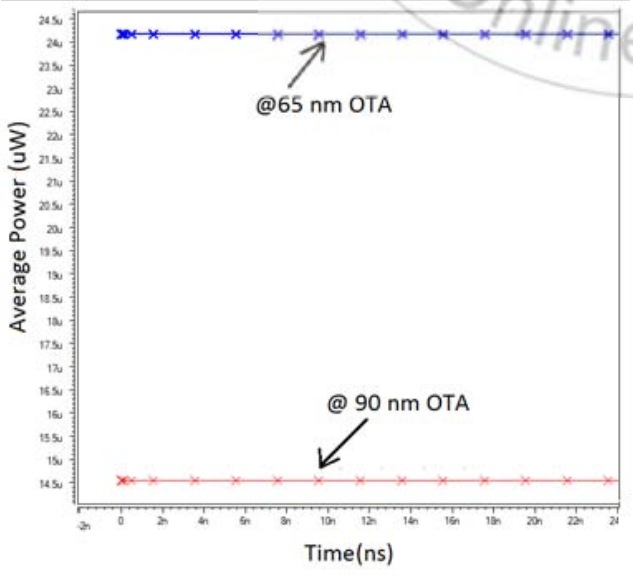

Figure 2: Average Power for 65nm and 90 nm OTAs

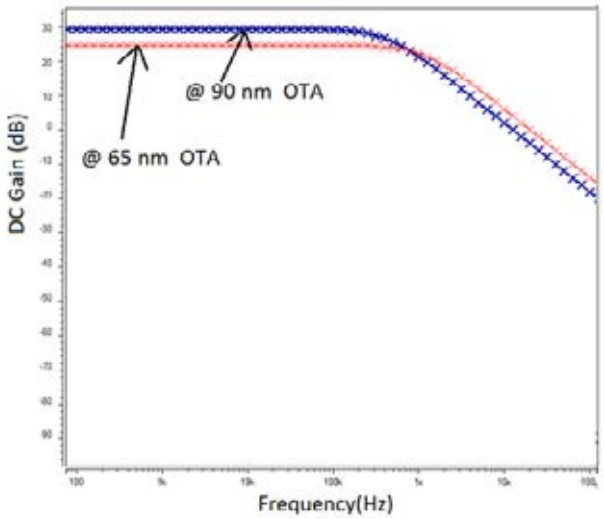

Figure 3: DC Gain for 65nm and 90 nm OTAs

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