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Novel Design of Low Power Nonvolatile 10T1R SRAM Cell

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Abstract: ***Power is a major issue in today's system on chip design at deep submicron. It is very important to control power dissipation in cache memories because 70 % of chip area is covered by memory in microprocessors. Various low power circuits are proposed in the past for volatile memories to alleviate the problem of power dissipation. However in today's era nonvolatile SRAMs (NVSRAMs) are being proposed to restore data along with faster access after power off operation. This paper proposes a nonvolatile Low power 10T1R SRAM cell. The proposed non volatile SRAM cell comprises a conventional 6T SRAM cell, memristor with 1 Transistor, USL technique comprising of 3 transistors, thus making a 10T-1R SRAM Cell. The proposed cell operates in three modes namely write, power off and restore. By simulating the proposed design, the power dissipation has reduced substantially. Experimental results shows that various parameters such as power, delay, power delay product and leakage current has also improved compared to the previous work. The work is done in cadence virtuoso tool at 45nm technology using GDPK045 library with supply voltage V_{dd}=1V***

Keywords: NVSRAM, Upper Switch level, leakage current, power, delay

1. Introduction

With technology getting scaled down, leakage current gets substantially increased. When the circuit is in idle mode, huge amount of power dissipates in the circuit. Since SRAMs are volatile, so in order to restore the stored data after power off operation nonvolatile memory is required with low power circuit. A nonvolatile SRAM is made up of Memristor comprising of two terms mem-memory, ristor-resistor is a two terminal device whose resistance is function of the voltage applied across its two terminals. A memristor remembers its most recent memresistance when voltage across terminals is removed till the time the voltage is applied. Memresistance is defined as rate of change of flux with respect to change in charge as follows:

$$M(q) = d(\Phi m/dq)$$

One of the major limitations of nonvolatile RAMs was the low density and speed as compared to volatile SRAM. But with the advancement in technology, density has increased to 64 Kbit and access time has also increased for NVSRAMs. Memristor presents another technology for the implementation of NVSRAMs. Memristor can operate at below 9 nm and offers faster access and lower space. This paper presents a new NVSRAM low power cell using a 6T SRAM cell; nonvolatile operation is performed using a memristor with 1 transistor. Previous work has been done using two Memristors in the SRAM cell. Power gating technique-upper switch level technique (USL) is proposed to minimize the leakage currents during the idle mode. With this technique the supply voltage is reduced to 0.65 V in standby mode.

2. Memristor (Memory-Resistor) Operation

Memristors are widely used as nonvolatile elements to restore the stored data during Power-off. A brief working principle of memristor is explained. Previous nonvolatile memory cells are also reviewed in this section. Invented the memristor and proposed its physical design .They realized its physical dimension by a resistor whose value varies linearly with respect to the charge q that passes across it. They made its design using two layers one a thin layer of TiO2 and other oxygen deficient layer TiO2-x (8 nm) surrounded by two Platinum wires. When positive voltage is applied at one end the ions start drifting from one end to resulting in change in concentration of oxygen vacancies which changes the resistance. As a result, the total resistance which is the sum total of both regions resistance is reduced. When no more ion scan pass between these two layers in that case the resistance is called memresistance .By applying negative voltage the process gets reverse and the ions goes back to the TiO2--x layer resulting in off state. This change in resistance is non-volatile. Fig. 1 shows both the regions of memristor where RON is the resistance of doped region and ROFF is the resistance of undoped region, w (t) is given by

$$dw(t)/dt = uv\ RON * i(t)/D \tag{1}$$

Where uv is the dopant mobility and D is the length of memristor. To minimize the nonlinearity effect which is one of the conditions when all the ions move from one layer to another, window functions are used in order to minimize these effects. The very logA model used in this work is non-linear dopant drift model with biolek window.

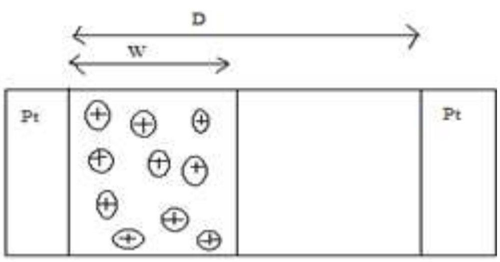

Figure 1: Memristor Physical Design

3. Conventional 6T Sram Cell Description

Basic Description: The conventional 6T SRAM Cell is shown in Fig 2. It consists of two cross coupled inverters with two access transistors.

a) **Hold Mode**: When word line is disconnected, both the access transistors disconnect the cell from the bit lines. The two cross-coupled inverters will continue to reinforce each other and the data remains in the hold mode as long as the power supply is on.
b) **Write Mode**: The write cycle begins by applying the value which needs to be written on the bit line and its complement on BLB.After that word line is activated and the data is stored at the nodes Q and Qb.
c) **Read Mode**: Assuming that logic '1' is stored in SRAM Cell. The read mode starts by pre-charging both the bit lines to a half of the supply voltage, then asserting the word line WL high. The values stored at Q and Qb gets transferred to the bit lines by leaving BL at its pre-charged value and discharging BLB through M5 and M1 to a logic '0' .

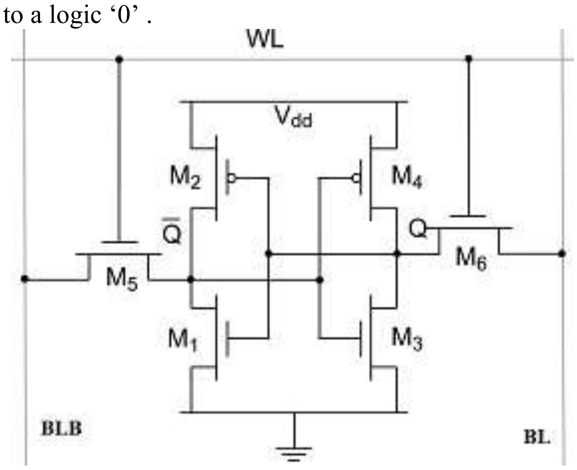

Figure 2: Conventional 6T SRAM Cell

4. Proposed NVSRAM Design

The proposed low power 10T1R NVSRAM circuit is shown in Figure 3. In this figure, conventional 6T SRAM cell is used with 1 memristor and 1 transistor controlling the memristor. The proposed power gating technique (USL) technique is applied on the pull up network. One of the terminals of Memristor is connected to the node Qa through the controlling transistor and the other end is connected to control voltage V2.The aspect ratio of each transistor is set as 3:1 for M5, M6 and M7; 4:1 for M1 and M2; 2:1 for M3 and M4; 6:1 for M9, M10; 5:1for M8. The operation of NVSRAM is controlled by the two control voltages namely V1 and V2 because of these two voltages the memresistance is varied from the low resistance state (LRS) to the high resistance state (HRS). Low resistance state corresponds to Ron that's 1kΩ and high resistance state corresponds to Roff which is 1MΩ.These values are Putting the properties of memristor operation during simulation.

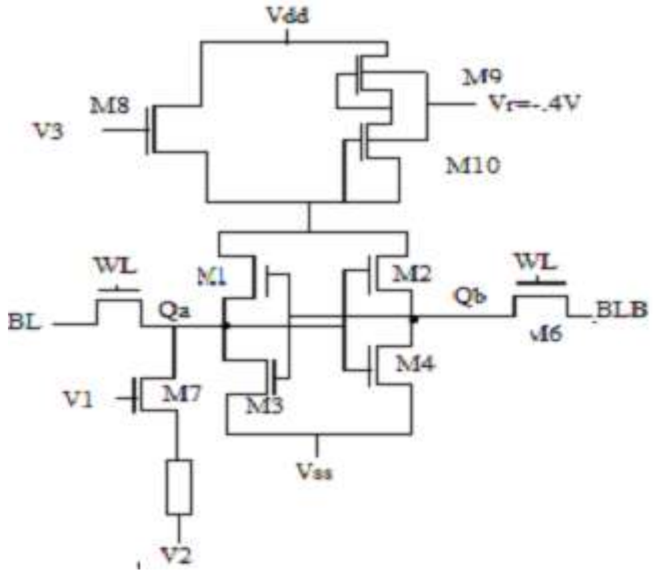

Figure 3: Proposed NVSRAM Cell

a) **Reset mode**: Firstly memristor has to be reset to high resistance state before writing in to the memory. In this operation if the memristor is not in HRS state, then, logic '1' is applied on both the control voltages V1 and V2. Power is held at logic '0' at this point of time. As a result the voltage from the V2 will pass through memristor and transistor M7 and thus the voltage at Qa will rise to logic '1'.
b) **Store mode**: In this phase, firstly the data is given at BL and the complement on BLB, then the access transistors are turned on by providing logic'1' at word line. In this operation the circuit is in active mode so implementing the USL technique transistor M8 is turned on while transistors M9 and M10 are reverse body biased by applying negative voltage of 0.4 V at the substrates of both the transistors. Due to this power supply (Vdd) is lowered to new low supply (Vdd1) .Meanwhile, transistor M7 is turned ON by applying voltage of 1 V at V1 and V2 is held at 0V so as to program the memristor accordingly to the voltage at node Qa. C. Power-Off mode: The non volatile characteristics of SRAM are achieved by turning off the supply. This is done so as to ensure that the stored data is retained during the Power-down mode. Logic '0' is given at V1, Vdd and Vss such that both the storage nodes are at logic'0'.

5. Simulation Results

The simulations of the above mentioned modes are explained in this section.

Firstly Store'1' operation is performed which is shown in Figure 4. Initially the NVSRAM is reset so as to set the Resistance of memristor to HRS; as shown in the timing waveform.

1) In the first phase(0 to 20ns), WL is on and the data to be written is provided at BL, correspondingly 6T SRAM is written, memristor is also programmed by turning on M7 by applying logic '1' at v1 and applying logic '0' at v2 respectively. In this case, when WL is at logic '1' state then only the data at node BL is written on Qa node. The

resistance change is from Qa to V2 and thus memresistance changes to LRS.

2) After the first phase, Vdd is lowered to 0Vand thus the data stored at node q discharges to '0' as shown in the waveform range from 20 to 40ns.In this stage memristor is in LRS state.
3) In the third phase, power supply turned ON; both the control voltages V1 and V2 are held at high value .If the memristor is in LRS ,then data at node charges back to logic '1' and if it is HRS state, then Qa discharges to'0' through M3 thus completing the Restore mode.

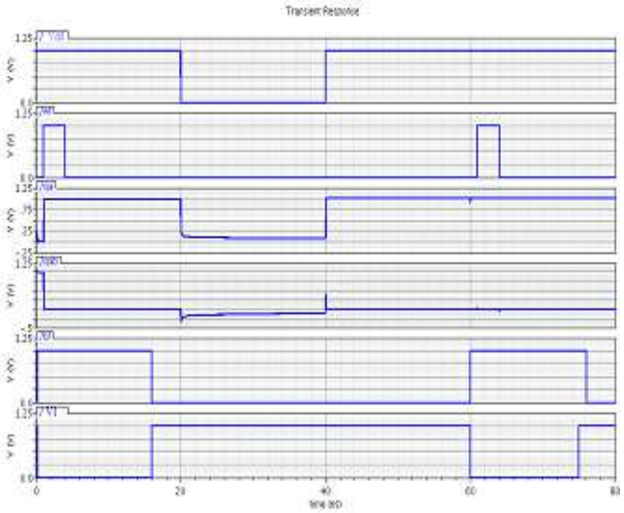

Figure 4: Output waveform of Store'1' power-down and restore operation

The Store '0' Power-down Restore '0' operation: In the first
Phase data is stored at node Qa as shown in Fig5. In the second phase Vdd is lowered. In the Restore cycle, when Vdd is turned on the stored data at node Qa is restored back ,in this phase both the voltages V1 and V2 are logic '1' that slowly charges the node Qa and Qab charges faster than q to '1'.

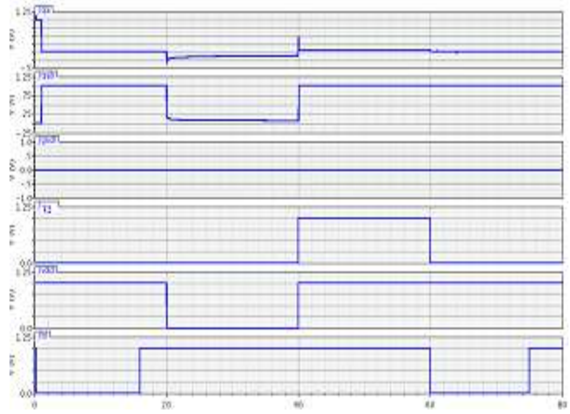

Figure 5: output waveform of Store '0', power down

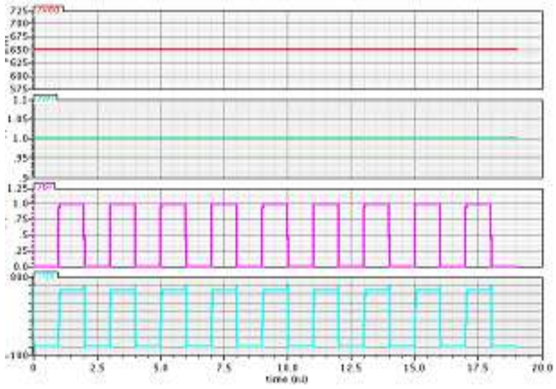

Figure 6: Write operation of proposed cell using USL technique

Fig.6 shows the write operation during idle mode of 10T1R SRAM Cell when power supply is lowered to 0.65V. n of proposed cell using USL technique

6. Results

Power is of two types namely static and dynamic. Nowadays static power dissipation is one of the most important area of concern since more power consumption by the circuit withdraws more current from the power supply thus leading to temperature rise of device as heat dissipated is directly proportional to the temperature. Static power dissipation due to standby leakage currents accounts for a huge percentage in total power dissipation. The proposed 10T1R memory cell achieves a significant reduction in both leakage currents and average power dissipation.

Figure 7 and Figure 8 shows the average power dissipation and static power dissipation in the conventional 6T SRAM Cell with proposed USL technique.

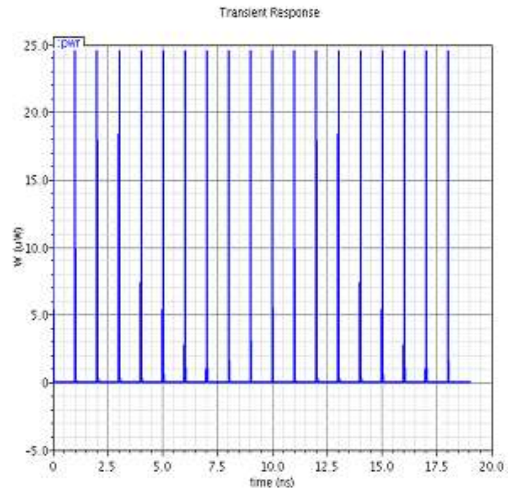

Figure 7: Average power dissipation in conventional SRAM cell with USL technique

Design Specifications	Conventional 16T SRAM cell	8T 2R[11]	9T 2R[12]	7T 1R[13]	Proposed NVSRAM
Technology NODE	45 nm	45 nm	45 nm	45 nm	45 nm
Supply Voltage	1 V	1 V	1 V	1 V	1 V
Power	1.164uW	0.134W	0.00612W	0.0119W	772.9Nw
Write delay	28.31 ps	48.88 ps	148.8 ps	32.67 ps	25.02 ps
PDP	0.03295e-15	658e-15	912e-15	390e-15	0.01932e-15
Leakage current	0.000996 nA	----	----	----	5.95Na

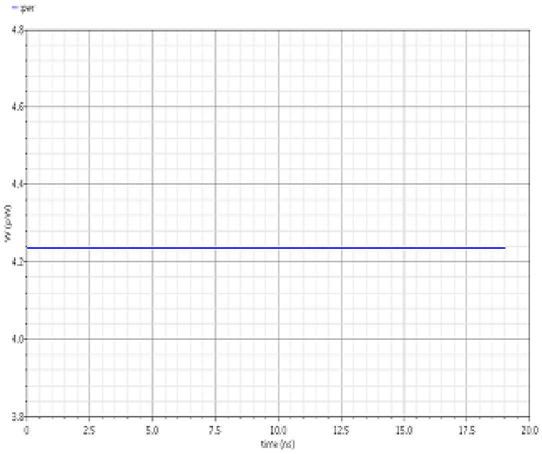

Figure 8: Static power dissipation in conventional SRAM cell with USL technique

7. Conclusion

This paper has proposed a low power design for a NVSRAM cell that makes the volatile SRAM cell into a non volatile SRAM cell which reduces the static power dissipation and PDP using the USL technique. In this work, supply voltage scales down by 35% which reduces the leakage power by 42% when compared to conventional 6T SRAM Cell. The leakage power is major concern in portable devices like smart phones, tablets etc because leakage power relates to battery backup of devices, and hence in our proposed work leakage power is reduced compared to previous work which leads to improved battery life of modern portable devices. With this proposed work larger non volatile memories can be designed in the future using the USL technique to reduce the power consumption of the circuit.

References

[1] C. Yakopcic, T. M. Taha, G. Subramanyam, E. Shin, P. T. Murray, and S. Rogers,"Memristor-Based Pattern Recognition for Image Processing: an Adaptive Coded Aperture Imaging and Sensing Opportunity," SPIE Adaptive Coded Aperture Imaging and Non-Imaging Sensors, 2010.
[2] Z. Biolek, D. Biolek, and V. Biolkov, ``A SPICE model of memristor with nonlinear dopant drift," Radio Eng. J., vol. 18, no. 2, p. 211, 2009.
[3] J. G. Lee, D. H. Kim,et al., "A compact HSPICE macro model of resistive RAM," IEICE Electron. Exp., vol. 4, no. 19, pp. 600–605, 2007.
[4] Strukov, D. B., and Likharev, K. K, "A reconfigurable architecture for hybrid CMOS/Nano device circuits". in Proc. ACM/SIGDA 14th international symposium on Field programmable gate arrays (2006), pp. 131–140.
[5] L. O. Chua, "Memristor – the Missing Circuit Element," IEEE Trans. on Circuit Theory, vol. 18, no. 5, pp. 507-519, September,1971.