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Fabrication and Evaluation of Thin Film Transistor with Improved Electrical Characteristics

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Abstract: ***Gallium Arsenide is a potential candidate for optoelectronic devices which can be used in Thin Film Technology with Alq_3 as gate insulator. The samples of field effect transistor are fabricated using thermal evaporation method. GaAs epilayers showed (00l) orientation with zinc blende structure and good optoelectronic quality with minimal thermoelastic/lattice mismatch strain. The device parameters have been evaluated from the characteristics. The TFTs exhibited good channel modulation and better stability Scanning electron microscopy (SEM), energy dispersive spectroscopy (EDS), X-ray powder diffraction (XRD) and the temperature dependence were used to characterize the layers.***

Keywords: Thin Film Transistors, channel modulation, thermal evaporation, SEM, EDS

1. Introduction

Medical field have experienced tremendous advances over the last century and continue to enjoy state-of-the-art cutting edge technology today. At the molecular level, to meet the need for diagnostics, FETs and semiconductor integrated circuit technology have provided a base to achieve miniaturized devices. Depending upon the application preferred for the medical field, the material chosen for fabricating FET varies. The semiconductor gallium arsenide (GaAs) is an important candidate in manufacturing a field effect transistor. GaAs is preferred than silicon for these applications due to its higher mobility and direct band gap structure. Recent progress in using ion implantation as a major means of controlled doping of semiconductors has led to significant advances in the fabrication of integrated circuits (ICs). Thin film technology is the basic of astounding development in solid state electronics. The usefulness of the optical properties of metal films, and scientific curiosity about the behavior of two-dimensional solids has been responsible for the immense interest in the study of science and technology of the thin films. Thin films are especially appropriate for applications in microelectronics and integrated optics. The processing of materials into thin films allows easy integration into various types of devices. The properties of material significantly differ when analyzed in the form of thin films. Most of the functional materials are rather applied in thin film form due to their specific electrical, magnetic, optical properties or wear resistance. Thin film technologies make use of the fact that the properties can particularly be controlled by the thickness parameter. Thin films are formed mostly by deposition, either physical or chemical methods. In the present work thermal evaporation method is used for the preparation of thin film field effect transistor. FET stands for field effect transistor is a three terminal unipolar solid state device in which current is controlled by an electric field. FET can be N-type or P-type. In this work a p-type GaAs fet is fabricated using thin film technology. The understanding of FET channel characteristics and its topological studies are important for improving the reliability of GaAs FET [1].

2. Thin Film Technology

Thin films are thin material layers ranging from fractions of a nanometer to several micrometers in thickness. Electronic semiconductor devices and optical coatings are the main applications benefiting from thin film construction. The engineering of thin films is complicated by the fact that their physics is in some cases not well understood. In particular, the problem of rewetting may be hard to solve, as there is ongoing debate and research into some processes by which this may occur. So a thin film is defined as a low dimensional material created by condensing, one by one, atomic/molecular/ionic species of matter. The thickness is typically less than several microns.

Thin film technology is a relatively young and ever growing field in the physical &chemical sciences which is confluence of materials science, surface science, applied physics, applied chemistry. Thin film technology has its objectives in the provision for scientific bases for the methods & materials used in thin film electronics. Additionally; it provides a sufficient data in the area of applications to permit for understanding of those aspects of the subject that might still be termed an ‘art’. Thin film of metals were probably first prepared in a systematic manner by Michael Faraday, using electrochemical methods. Thin films have a no. of applications in various fields. Few of them are A.R.coatings, solar energy converters, transistors, coating, technology, interference filters, polarisers, narrow band filters, solar cells, photoconductors, IR detectors, waveguide coatings etc[4].

2.1 Practical Application of Thin Film – FET

Although the study of thin film phenomena dates back well over a century, it is really only over the last four decades that they have been used to a significant extent in practical situations. The requirement of microminiaturisation made the use of thin and thick films virtually imperative. The development of computer technology led to a requirement for very high density storage techniques and it is this which has stimulated most of the research on the magnetic properties of

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thin films. Many thin film devices have been developed which have found themselves looking for an application or, perhaps more importantly market. In general these devices have resulted from research into the physical properties of thin films. FETs have source, drain, and gate terminals that correspond roughly to the emitter, collector, and base of BJTs. Most FETs have a fourth terminal called the body, base, bulk, or substrate. This fourth terminal serves to bias the transistor into operation; it is rare to make non-trivial use of the body terminal in circuit designs, but its presence is important when setting up the physical layout of an integrated circuit. The size of the gate, length L in the diagram, is the distance between source and drain. The width is the extension of the transistor, in the direction perpendicular to the cross section in the diagram (i.e., into/out of the screen). Typically the width is much larger than the length of the gate. A gate length of 1 µm limits the upper frequency to about 5 GHz, 0.2 µm to about 30 GHz. The names of the terminals refer to their functions. The gate terminal may be thought of as controlling the opening and closing of a physical gate. This gate permits electrons to flow through or blocks their passage by creating or eliminating a channel between the source and drain. Electron-flow from the source terminal towards the drain terminal is influenced by an applied voltage. The body simply refers to the bulk of the semiconductor in which the gate, source and drain lie. Usually the body terminal is connected to the highest or lowest voltage within the circuit, depending on the type of the FET. The body terminal and the source terminal are sometimes connected together since the source is often connected to the highest or lowest voltage within the circuit, although there are several uses of FETs which do not have such a configuration, such as transmission gates and cascade circuits[2],[3],[5].

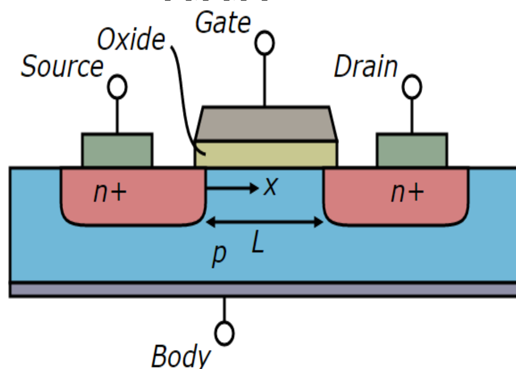

Figure 1: Cross sectional View of FET [4]

In the past two decades there have been extensive studies of the electrical and optical properties of GaAs. GaAs has a Zinc blende structure. The crystal structure of GaAs is shown in figure 2. It comprises of two interpenetrating face centered cubic lattices, one for Ga and another for As displaced from one another by (¼, ¼, ¼) a, where 'a' is the lattice constant, which is ~ 5.66A°.

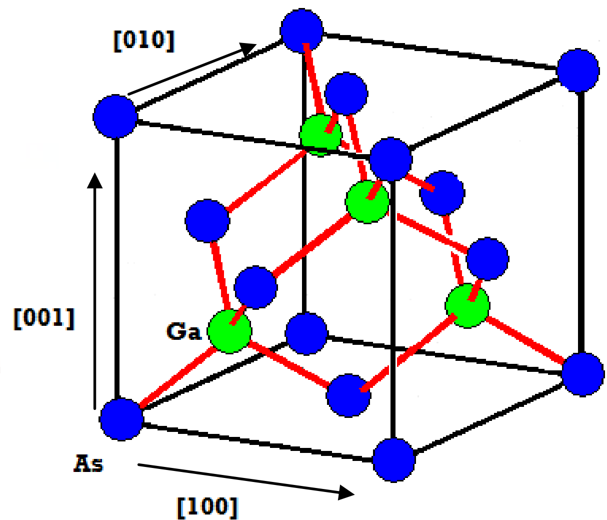

Figure 2: Crystal Structure of GaAs [8]

GaAs has direct band gap structure. The conduction band has three minima: one at k = 0 (the Γ point), another at the L on the Brillouin zone boundary along <111> direction and at X point on the Brillouin zone boundary along <100> direction. GaAs has tetrahedral bonding between Ga and As and the character is partially ionic with large covalent character. The band gap is 1.42eV at 300K [8].

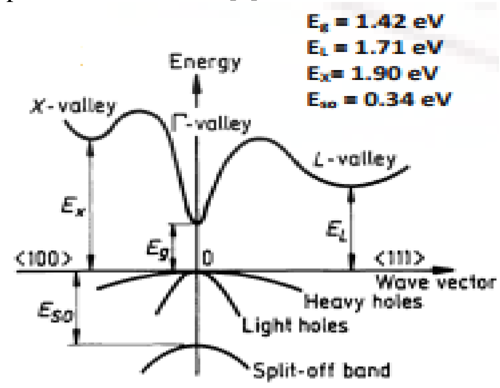

Figure 3: Band gap structure of GaAs [8]

Because of its high electron mobility (8500 cm^2/V-sec as compared to 1500 cm^2/V-sec for Si at room temperature), high speed devices have been produced. Large scale integrated circuits in GaAs are being developed in an effort to increase device speed, decrease power requirements and be more cost effective[6],[7].

3. Experimental Details

3.1 Deposition Technique

In the present work thermal evaporation method is used for the preparation of thin films. The films are deposited onto clean substrates. In thermal evaporation, the material is heated to vapour form by means of resistive heating. On heating the materials in vacuum, sublimation takes place and the atoms are transported and get deposited onto the cleaned substrates held at a suitable distance from the source and kept at desired temperatures. The material for deposition is supported onto a vapour source which is heated to produce

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required vapour pressure. The requirements for the vapour source are that it should have a low vapour pressure at the deposition temperature and should not react with the evaporant. We have used molybdenum boats and tungsten baskets as the vapour sources. The evaporant material in the powder form is kept in the molybdenum boat. The low tension (LT) supply for evaporation source is obtained from a 230 V input transformer by means of parallel connections in the secondary side of the transformer. The LT output from the transformer is fed through a current meter and a selector switch to LT feed-through and filament holders. The unit is connected to the 10 V/100A ratings of the transformer.

3.2 FET Fabrication

TFTs have been fabricated by thermal evaporation method and ultrasonically cleaned glass substrates by vacuum deposition of different layers in the given sequence: silver source drain electrode, GaAs film at elevated substrate temperature (200°C), Alq_3 layer as gate insulator and finally the tin as gate electrode as shown in figure 4. The channel was defined by a 50 nm wire grill fixed on the source drain mask. The technology of producing the thin films of conjugated polymer coatings based on tris-(8-hydroxyquinoline) aluminum (Alq3) by the thermal evaporation method on a solid substrate was developed and optimized. The optimal mode and conditions of the producing, in which the thickness of the coatings are in the range of 10 nm, was founded. All the depositions were made in vacuum of the order of 10^{-6} torr. The fabricated samples were then used for recording I-V data.

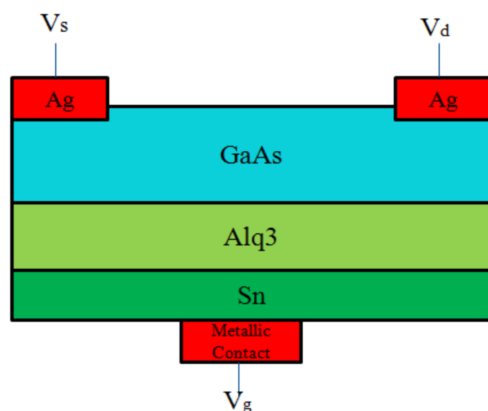

Figure 4: Schematic Representation of GaAs FET

4. Results & Discussions

The source-drain characteristics of a fresh sample of GaAs – Alq_3 TFT at different gate voltages (V_G) are shown in figure 5.

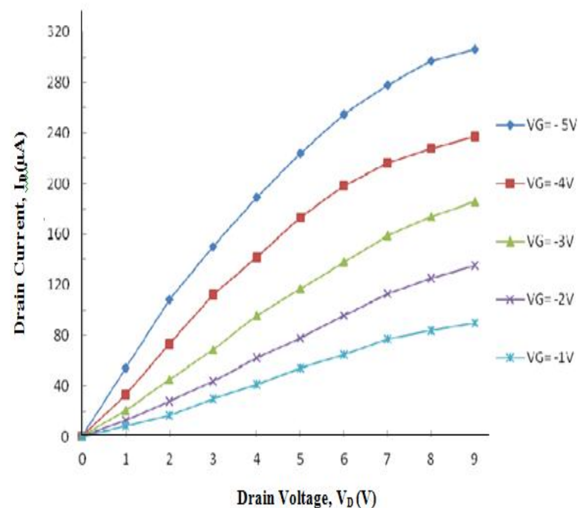

Figure 5: Source Drain Characteristics of a GaAs FET

The following transistor parameters are evaluated from the characteristics and LCR meter.

Trans conductance (gm) = 100 μmho.

Output resistance (rd) = 111 K ohm.

Amplification factor (μ) = 11.1

Gain band-width product = 8.85 KHz

Due to polycrystalline nature of GaAs film, existence of traps in the devices is most common. Presence of traps in the devices could be determined if the transition of the saturation region of the normalized drain current $I_D/I_{D\ (sat)}$ versus drain voltage plot is sharp the device contains traps. The transition is smoother and less abrupt for trap less TFTs. Relatively sharp transition of this plot at V_G = 5V (fig. 5) infers the presence of traps in the devices.

Figure 6: SEM micrograph of GaAs

Figure 6 presents a plan view SEM micrograph of the GaAs layer grown by the thermal evaporation setup with a spacer of 2 mm thickness. In this figure a kind of polycrystalline structure is observed, it corresponds to a three-dimensional growth. This structure is uniform in the central area of the grown layer while, in the periphery close to the delimiting o'ring spacer some density of pit defects (OPO) appears.

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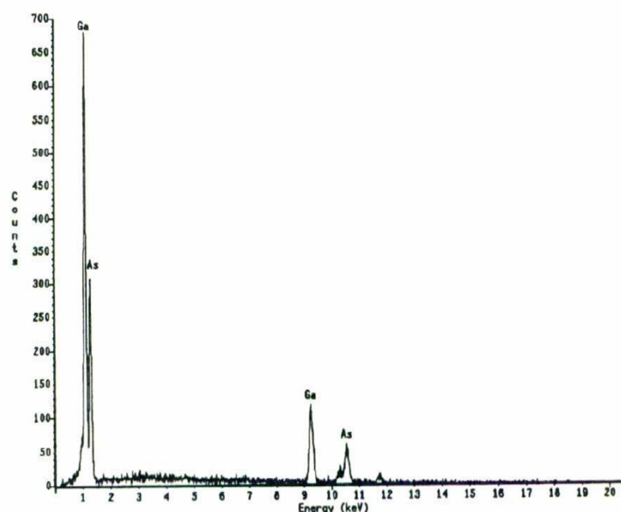

Figure 7: EDS spectrum corresponding to the GaAs layer

Figure 7 shows the EDS spectrum corresponding gallium arsenide layer. It shows the presence of the elements that is gallium and arsenide present in the gallium arsenide layer.

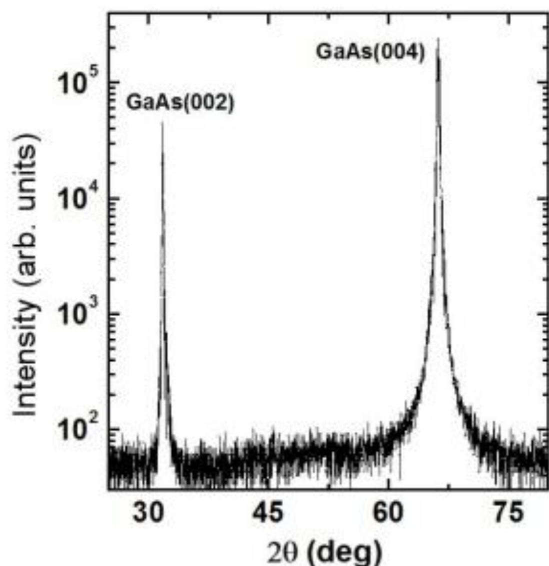

Figure 8: XRD pattern of GaAs layer

Figure 8 shows the XRD pattern of a p-type GaAs thin film on a GaAs (001) substrate. All peaks were indexed on the basis of the zinc-blende structure with a lattice constant of 5.655 ˚A. The film was oriented along the < 100 > direction.

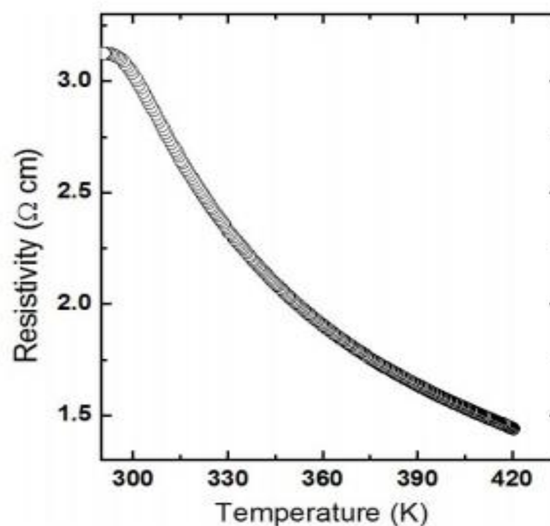

Figure 9: Temperature dependence of the resistivity for a p-type GaAs thin film

Figure 9 shows the temperature dependence of the resistivity of a GaAs thin film. The resistivity decreases with increasing temperature up to 420 K, which is a semiconducting behavior.

4. Conclusion

TFTs fabricated with the semiconductor insulator combination of GaAs and Alq_3 exhibits good channel modulation and with a good stability. The crystal structure ad band gap structure is also depicted in this paper. The drain current decreases with time and ambient exposure lead to faster deterioration. Presence of traps and absorption of atmospheric vapour contribute towards device degradation. Improved fabrication technique will be needed to ascertain the suitability of this semiconductor insulator combination. From the morphological analysis by SEM we conclude that the GaAs layers with the "best" morphologies were grown at the smaller source-substrate temperature gradients, since they are homogeneous throughout the growth area and present less defect densities. From the EDS analysis it is found the presence of gallium and arsenide in the thin film. XRD pattern were also noted. As for the semiconductor, the resistivity decreases with increase in temperature, the same is found for the gallium arsenide thin film.

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