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Design and Implementation of Efficient Combinational Logic Circuits with Minimum Area and Circuit Complexity Using Quantum- dot Cellular Automata (QCA)

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Abstract: ***Quantum dot cellular automata (QCA), is a rising innovation and a possible alternative for scaling-down trend of VLSI technology. It advantages diminutive size, low power consumption, better switching speed. QCA seems to be a good competitor for future digital systems and widely utilized as a part of advance frameworks. Therefore numerous implementations of QCA based logic functions have been proposed so far. In this paper, an efficient XOR gates is presented. The model proves designing capabilities of combinational logic circuits. The proposed XOR gate has been testified to design logic circuits for QCA. Adder circuit is the most fundamental component used in digital systems. An efficient Half-Adder and Half-Subtractor circuits are designed employing the proposed XOR gate. Performance evolutions of the proposed XOR circuits are compared to its conventional counter parts. The functionality and circuit operation of the proposed designs have been authenticate used QCA Designer simulation tool Ver. 2.0.3.***

Keywords: QCA, XOR Gate, Half-Adder, Half-Subtractor, Performance, QCA Designer

1. Introduction

The CMOS technology has been emerged over last four decades as predominant technology of microelectronics industry. It has improved device density, power consumption, and speed of integrated circuits during past several decades by means of reducing the feature size of various semiconducting components. However, CMOS technology has some growing concerns like ultra-thin gate oxides, Off-stage leakages and power consumption which cannot be ignored. Today‟s leading VLSI experts predicts a hard well for CMOS and other conventional fabrication technology in about a decade. This lithographic based technology is now facing serious challenges. Moreover researchers adore more speed and miniaturization has brought them to the verge of classical devices, forcing them to peek in an unknown and astonishing world of nanotechnology and quantum devices. A number of research efforts that have focused on new devices that might replace CMOS technology [1-2]. Utilizing the QCA technology for implementing digital logic circuits is one of the interesting approaches, which seems to be a best competitor and a possible replacement of CMOS technology. QCA nanotechnology is first introduced by Lent et al. [2]; an emerging nanotechnology at the nanotechnology scale by controlling the position of single electron. QCA has achieved significant interest to researchers due to its attractive characteristics such as high device density, low power consumption and small dimensions. It does not involve any voltage or current to encode the information. Position of single electron using Coulombic repellent force has been used to encode the information. Each QCA cells consists of four quantum dots. Two electrons are loaded, in antipodal sides which determine the logic, „0‟ and „1‟. QCA cells are used to implement combinational logic circuits.

Several studies have been reported about QCA circuits [3-15]. Exclusive-OR (XOR) is the most logical gate and is widely used in many combinational and sequential logic circuits. Several XOR gates have been reported in [3-8]. Therefore numerous studies have been reported about QCA Full Adder [9-14] and Programmable Logic Array [16].A new bit serial QCA adder has also been proposed in [17] that uses carry feedback and only requires three majority gates and two inverters.

In this paper a new QCA implementations have been proposed. In the initial step, an efficient two XOR gates with the proper arrangement of QCA cells and clock delays has been proposed. The proposed XOR gates consist of less area and reduced circuit complexity as compared to previous structures. Several conventional XOR designs have been compared to the proposed adder designs in which circuit parameters like area and circuit complexity are in comparison factors. In the next step, the proposed XOR gate has been testified to design a Half-Adder & Half-Subtractor circuit with minimum area and circuit complexity. We aimed to design QCA circuits that are minimal in its use of cell counts, area and clock delays.

Rest the paper is organized in five sections. The second section provides the necessary QCA Materials and Methods. The proposed QCA XOR is presented in third section and is compared with conventional XOR implementations. The proposed 1-bit full Adder (FA) and its simulation results

have been discussed in fourth section. Finally, conclude has been discussed in last section.

2. Materials and Methods

2.1 QCA cell

QCA circuits are composed of identical components which are referred to as QCA cells. A QCA cell, a square-shape structure, has four quantum-dots positioned at the four corners and two electrons which are allowed to move between the dots. Due to Coulombic repulsion, the electrons occupy the dots located at the diagonally opposed corners. Hence, two stable states occur which are assigned to logics "0" and "1" [2, 10]. Fig. 1 shows a QCA cell and the two possible polarizations. By placing QCA cells side-by-side, a QCA standard wire can be constructed.

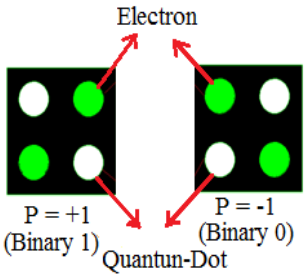


Figure 1: QCA cell and two possible polarizations

2.2 QCA Fundamental Structures

Two basic structures in QCA are Inverter and Majority gate (MG) [10]. Fig. 2 depicts one of the formerly presented Inverters. As illustrated, the input polarization is inversed when it reaches the output cell.

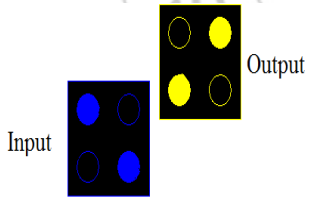


Figure 2: Simple QCA inverter.

In conventional QCA designs, three-input and five-input majority gates play a significant role in general circuit architecture. Therefore, circuit"s complexity and latency have been relatively associated to the cells configuration of QCA fundamental gates. Accordingly, various QCA structures for multi-input majority gates have been designed by researchers, so far. Fig. 3 shows layout of a three-input majority gate.

The logic function of MG gate is worked out as:
MG (A, B, C) = AB+AC+BC

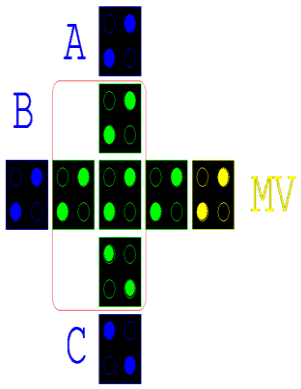


Figure 3: QCA 3-input Majority gate

In Fig. 4, two five-input majority gates are displayed which are provided in [18-19]. The output cell of the gate shown in Fig. 4 (a) is a middle cell which is a barrier to cascading gates, however this problem is solved in the design depicted in Fig 4 (b). The logical function of five-input majority gate is written as:

$$MG(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE$$

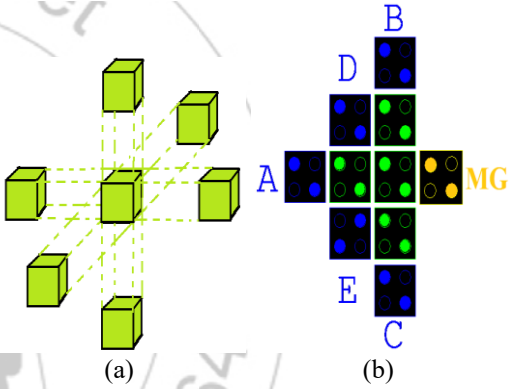


Figure 4: Layouts of two QCA 5-input majority gates (a) in [18] (b) in [19].

2.3. Wire Crossing in QCA

Wire crossing is a significant issue in QCA circuit design. Three different crossing methods have been proposed, so far [20]:

1) Single-layer crossing: this kind of QCA crossing is implemented in one layer using both 45-degree and 90-degree QCA cells, each one dedicated to one side of a crossing. These different cells can pass over the crossing without any significant effect on each other. Fig. 5(a) depicts a single-layer crossing.
2) Logical crossing: although this crossing is implemented on a single layer, only one type of QCA cell is required. The effects of wires of a crossing on each other are neutralized utilizing different phases in each wire. Cells with switch and hold phases are allowed to cross over the cells with release and relax phases, respectively. Fig. 5(b) illustrates a QCA logical crossing.
3) Multi-layer crossing: unlike the previous one, multi-layer method uses only 45-degree cells or 90-degree ones. One wire of the crossing is transferred to another layer and after passing through the crossing, the wire is returned to the original layer (Fig. 5(c)).

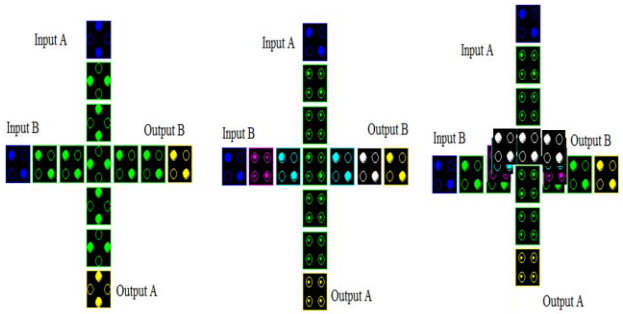


Figure 5: Wire crossing methods: (a) Single layer wire crossing (b) Logical crossing (c) Multi-layer wire crossing

3. QCA Implementations

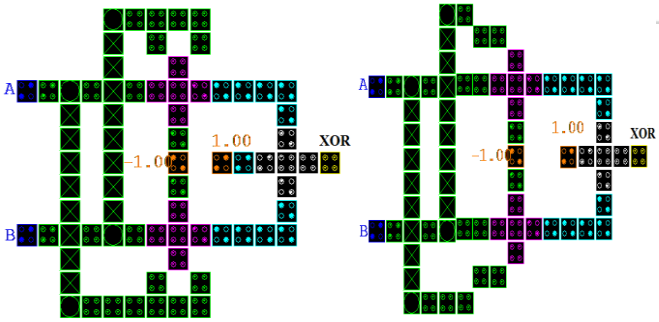
3.1 The Proposed Exclusive-OR (XOR) Gates

In addition to basic and universal logic gates in digital systems, Exclusive-OR (XOR) gate is also widely used for the design of digital circuits. These gates are mainly used in arithmetic operations as well as error detection and correction circuits. XOR gate is usually found as 2-input gates. No multiple-input XOR gates are available since they are complex to fabricate with hardware. Several QCA XOR implementations have been reported in [3-6, 10, 21].

Exclusive-OR (XOR) is a logical operation on two operands that results in a logical value of true if and only if one of the operands, but not both, has a value of true.

The logic expression for XOR gate is:
$A \oplus B = A'B + AB'$

Two such conventional QCA layouts are shown in Fig. 6(a) & (b) [6, 21]. The main drawback of these ciruits are circuit complexity and area. These circuits are constructed using Multi-layer and Wire crossover schemes which causes low robustness and fabrication difficulties in QCA circuits [21-23]. Numerious combinational circuits have been redesigned to reduce the circuit complexity and achieve significent efficiency.

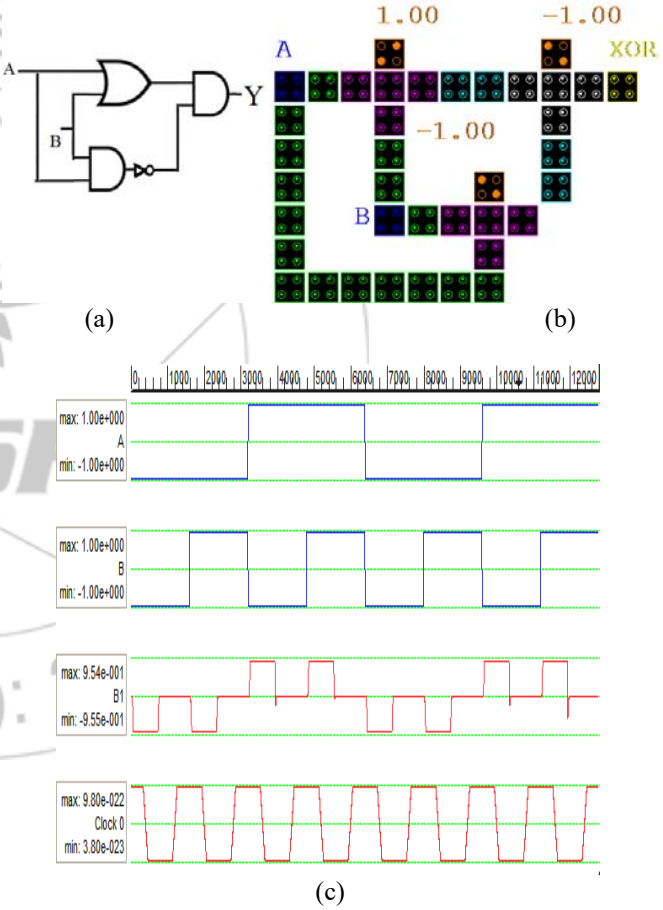


(a) (b)

Figure 6: (a) Conventional designs of XOR [21] (b) Conventional designs of XOR [6].

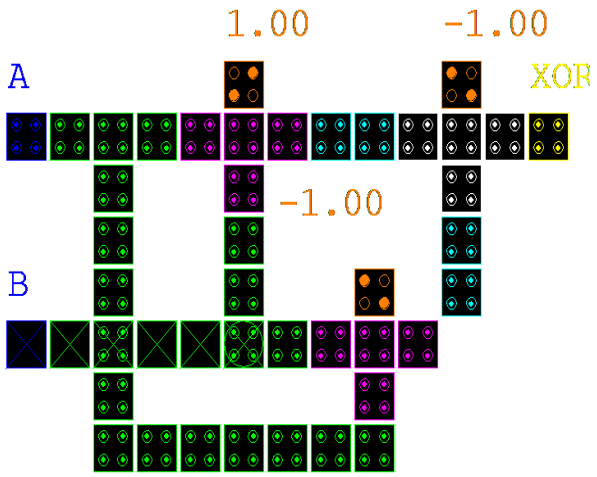
We have proposed an efficient two XOR gates. First one is implemented using Single layer and second layer is implemented using Multilayer. Fig. 7(a) shows the logic diagram of proposed XOR. Single layer is designed using with simple arrangement of standard cells and consist of very less area 0.03um^2, circuit complexity of 38-cells with proper arrangement of 1-clock delay. The new XOR gate is the modified version of XOR presented in [24]. The results of the comparison of all the existing XOR designs are presented in Table 1. The QCA layout of the modified single layer XOR gate is shown in Fig. 7(d) and simulations results are shown in Fig. 7(c). The second layer is composed of Multi-layer and consists of area 0.04um^2, circuit complexity of 47-cells with proper arrangement of 1-clock delay. The QCA layout of the Multilayer proposed XOR gate is shown in Fig. 7(d) and simulations results are shown in Fig. 7(e).The proposed layouts can be easily used to design complex circuits based on XOR operation like adder circuits, shift registers etc.

These results indicate that the proposed design consumes smaller area, has less or equal latency and also has less complexity compared to the previous designs except the proposed XOR design in

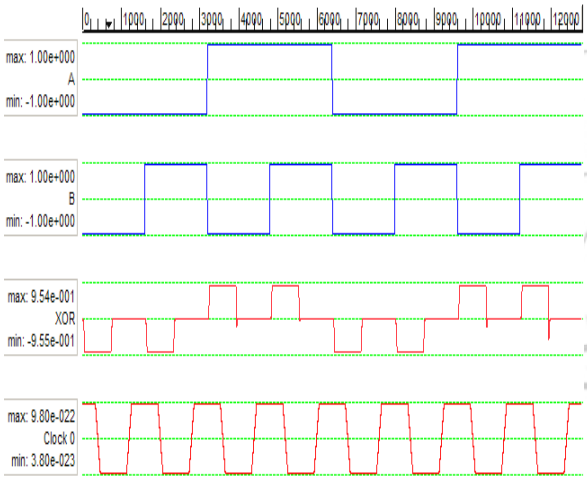


(a) (b) (c)

Figure 7: (a) Logic diagram (b) QCA layout XOR (c)Simulation results



(d)



(e)

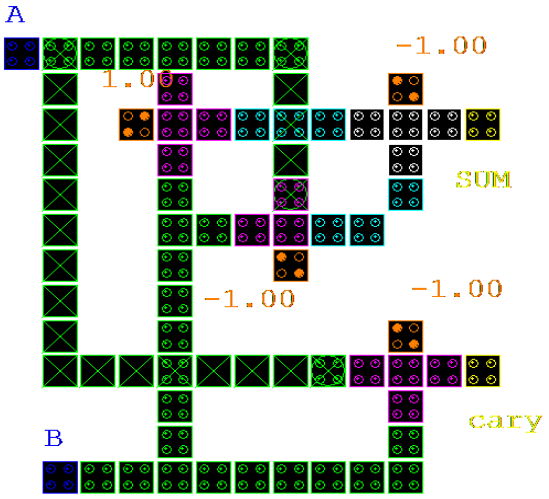
Figure 7: (d) QCA layout Multilayer XOR (c)Simulation results

3.2 QCA Layout of Half-Adder

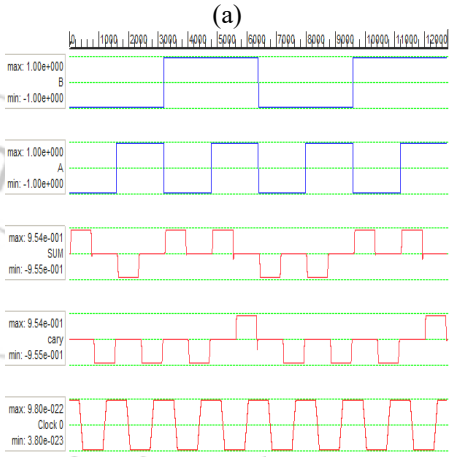
Adder circuits perform various arithmetic operations like addition, subtraction, division and multipulcation; Half-Adder is the main block to design Full Adder. The Half-adder is a performs addition of two bits. It is designed conventionally by XOR and AND gates, with two inputs A and B and output. Sum is produced using XOR gate and Carry is produced using AND gate.

The logic function for Half-adder is:
Sum = A'.B + A.B' which is Exclusive-OR (XOR) function
Carry = A.B, which is an (AND) function

Fig. 8(a) shows the logic diagram of proposed Half-Adder. It is constructed using Multilayer scheme. The proposed XOR gate present in Fig. 7(d) has been further modified and testified to design Half-Adder. The proposed Half-Adder consists of circuit area of 0.06um^2, circuit complexity of 82-cells with proper arrangement of 1-clock delay. The simulations results of proposed Half-Adder are shown in Fig. 8(b).



(a)



(b)

Figure 8: (a) QCA layout Half-Adder (b)Simulation results

3.3 QCA Layout of Half-Subtractor

The Half-Subtractor is a combinational circuit that performs subtraction of two bits. It is designed conventionally by XOR, AND and NOT gates. When two inputs A and B are subtracted, the Difference and Borrow outputs are produced. Difference is produced using XOR gate and Borrow is produced using AND gate.

The logic function for Half-Subtractor is:
Difference = A'.B + A.B', which is XOR function
Borrow = A.B', which is an AND function

Fig. 9(a) shows the logic diagram of proposed Half-Subtractor. The proposed Half-Subtractor consists of circuit area 0.06 um^2, circuit complexity of 81-cells with proper arrangement of 1-clock delay. The simulations results of proposed Half-Subtractor are shown in Fig. 9(b).

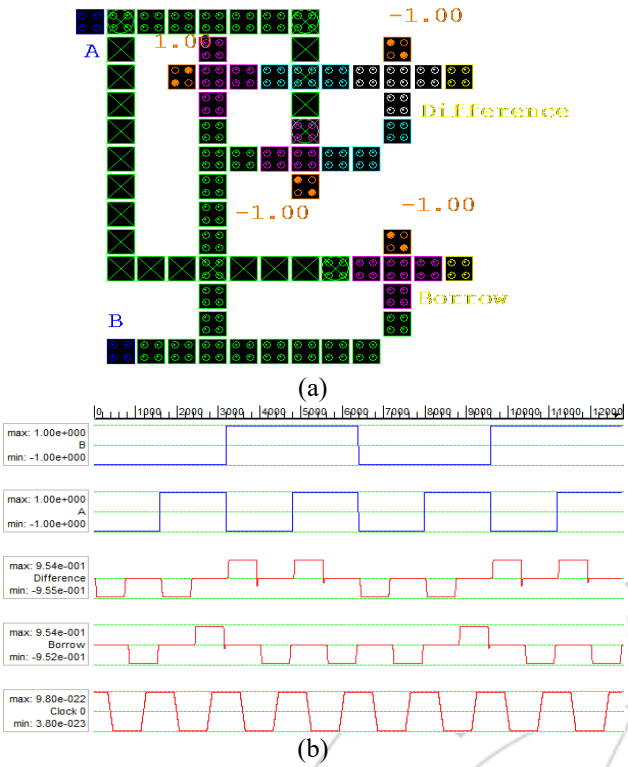


Figure 8: (a) QCA layout Half-Subtractor (b)Simulation results

4. Performance of XOR Gates

Table 1 shows the significant improvements of our proposed designs as compared to [4-5, 6, 10, 21, 24]. Here we have developed an extensive structural analysis in different aspects (Area, Circuit complexity& Clock delays) of full adder structures previously published in literatures. The proposed single layer design is the modified version of previous XOR present in [24]. To correct the circuit functionality we have reduce maximum number of circuit complexity (cell counts) and area in previous XOR presented in [24]. Area and circuit complexity is the major issue for any circuit designers at neno-scale. Therefore in general Table 1 depicts the significent improvements in terms of area and circuit complexity (cell counts) as compared to as compared to conventional counter parts [4-5, 6, 10, 21, 24]. Complexity, area and latency is the major issues for any circuit designers at nano-scale. The proposed XOR implementations are at advantage with the conventional designs and is evident from the said Table.

Table 1: Comparisons of XOR Gates

Feature	Complexity (No. of cells)	Area ($um^{2)}$	Latency (clock delay)
Ref.(4)	95	0.21	2.25
Ref.(5)	121	0.22	1
Ref.(6)	74	0.07	1
Ref.(10)	84	0.08	1
Ref.(21)	87	0.09	1
Ref.(24) Fig 14(b) Previous XOR parameters	54	0.07	1
Single Layer Modified XOR New parameters Fig. 7(b)	38	0.03	1
Multiayer Proposed XOR Fig. 7(d)	42	0.04	1

5. Conclusion

In this paper, two efficient XOR (Single layer & Multilayer) gates have been proposed with the reduced number of circuit complexity (cell counts) and area as compared to conventional counter parts. The comparison of proposed XOR gate has been listed in Table 1. The proposed XOR gates have achieved significant improvements in terms of circuit parameters like area and circuit complexity (cell counts). In addition, the proposed XOR gates have been testified to implement a new Half-Adder and Half-Subtractor circuits for QCA. Bistable approximation simulating engine of QCA Designer tool have been used to verify the operation and simulation results of the proposed circuits.

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