# Implementation of Bridgeless Cuk Power Factor Corrector with Positive Output Voltage

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Abstract: A single-phase bridgeless Cuk ac/dc power factor correction (PFC) rectifier with positive output voltage is designed. For low output voltage product applications, the rectifier is designed to convert high input voltage to low output voltage. Due to no bridge diodes required and thus decreased input conduction losses, the rectifier efficiency can be improved. The proposed rectifier operates in discontinuous conduction mode, and the current-loop circuit is hence not needed. In addition, only a single switch is used in the rectifier to simplify the control circuit design. A simple translation method to have the positive output voltage in the Cuk converter is presented in the rectifier to reduce the component counts and the cost. The operational principles, steady-state analysis, and design procedure of the rectifier are analysed in detail.

Keywords: DC-DC converter, Power factor correction, zcs turn on of switch, zcs turn off of diode

## 1. Introduction

The current flows through bridge diodes and the power switch  $S_1$  during the switch on-time and through bridge diodes and the output diodeD<sub>0</sub> during the switch off-time. Thus, during each switching cycle, the current flows through three power semiconductor devices. As a result, the significant conduction loss caused by the forward voltage drop across the bridge diodes degrades the converter's efficiency, particularly at low line input voltage. To reduce the conduction losses, the number of semiconductor devices should be reduced in the current path.

Some methods are introduced to reduce conduction losses in Cuk converter. Bridgeless PFC circuits where the current flows through a minimum number of switching devices compared with the conventional PFC rectifier. Accordingly, the converter conduction losses can be significantly reduced, and higher efficiency can be obtained and cost savings.

The Cuk and SEPIC converters have negative output voltages. Therefore, the extra requirement is an inverse amplifier circuit to translate the negative into the positive voltage The additional inverse amplifier circuit needed.thus increases the cost. obtain the positive output voltage in cuk converter without the inverting amplifier circuit, we transfer the polarity of all the components

## 2. Topology of the Converter

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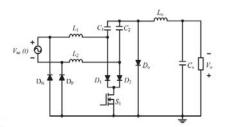


Figure 2.1: BridgelessCuk PFC Rectifier with Negative Output Voltage

Fig.2.1 shows the initial bridgeless Cuk PFC rectifier, which has a negative output voltage, like the existing Cuk PFC rectifier. As noted, for this circuit, an inverting circuit is needed to transfer the negative to the positive output voltage is still required for analog feedback control, as shown in Fig. 2.2 To obtain the positive output voltage without the inverting amplifier circuit, we have to transfer the polarity of all the components in Fig. 2.1 in the way as shown in Fig. 2.3.

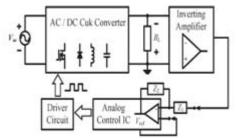


Figure 2.2: Blocking diagram of the conventional Cuk PFC circuit (with negative output voltage).

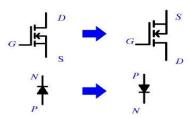


Figure 2.3: Transferring the polarity of all components (switch and diodes)

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By transfering the polarity of all the components we can obtain the bridgeless Cuk PFC rectifier with positive output voltage.

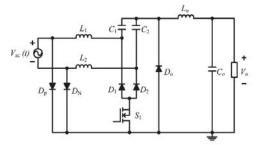


Figure 2.4: BridgelessCuk PFC Rectifier With Positive Output Voltage

Thus, the feedback control circuit is simpler, and the cost can be also reduced, as compared with the conventional feedback control circuit shown in Fig. 1.2 although the power switch employed in the circuit is floated with a highside gate driver needed.

#### Steady state analysis assumptions

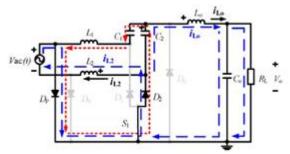
Before analyzing the rectifier, the analysis of the circuit supposes that the converter is operating at steady state with the following assumptions.

- 1) The ON-state resistance  $R_{DS}$  and parasitic capacitances of the main switch  $S_1$  and the forward voltage drops  $V_d$  of the diodes are neglected.
- 2) The input capacitances are large enough such that, during a switching period  $T_s$ , their voltages are considered to be constant.
- 3) The output capacitor  $C_o$  is sufficiently large that the output voltage is considered to be constant.
- 4) The proposed converter is operated in DCM.
- 5) Due to symmetry of the circuit, it is sufficient to analyze the circuit during the positive half-cycle of the input voltage

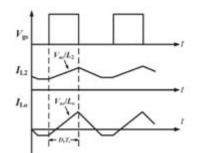
# 3. Operation of the Converter

The converter is operated in discontinous conduction mode.Operation of the converter can be explained through three modes.

*Mode 1*  $[t_0 - t_1]$  :



**Figure 3.1:** Equivalent circuit in mode I (switch  $S_1$  is turned on).



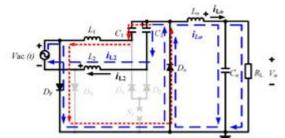
**Figure 3.2:** Theoretical DCM waveforms during one switching period  $T_S$  in mode I (switch  $S_1$  is turned on)

This mode starts when switch S1 is turned on, as shown in Figs.3.1and 3.2 Input inductor L<sub>2</sub> starts to charge linearly in slope of  $\frac{Vac(t)}{L_2}$  and diode D<sub>P</sub> is forward biased by the inductor current L<sub>2</sub>. The voltage acrossL<sub>0</sub> is equal to V<sub>ac</sub> (t) thus, L<sub>0</sub> increases linearly in slope of  $\frac{Vac(t)}{L_0}$ . The inductor currents of L<sub>0</sub> and L<sub>2</sub> during this mode are given by  $\frac{di_L}{dt} = \frac{V_{ac}(t)}{L_n}$  n=2, Accordingly, the peak current through the active switch is S<sub>1</sub> given by

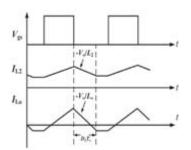
$$I_{(S_1),PK} = \frac{Vm}{L_e} * D_1 * T_S$$

where  $V_m$  is the amplitude of the input voltage Vac(t),  $D_1$  is the switch duty cycle, and  $L_e$  is the parallel combination of inductors  $L_1$ ,  $L_2$  and  $L_o$ 

*Mode 2*  $[t_1 - t_2]$ :



**Figure 3.3:** Equivalent circuit in mode II (switch  $S_1$  is turned off)



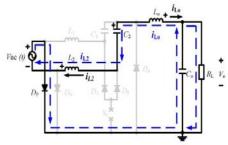
**Figure 3.4:** Theoretical DCM waveforms during one switching period  $T_S$  in mode II (switch  $S_1$  is turned off)

This mode starts when switch  $S_1$  is turned off,  $D_o$  is turned on, simultaneously, as shown in fig 3.3, fig 3.4 Input inductor  $L_2$  starts to discharge linearly in slope of  $\frac{Vac(t)}{L_2}$ . And diode D<sub>P</sub>is forward biased by the inductor current  $i_{L_2}$ . The voltage across  $L_o$  is equal to  $V_o$ ; thus,  $i_{L_2}$  decreases linearly in slope of  $\frac{V_o}{L_2}$ . Note that diode  $D_o$  is turned off at zero current.

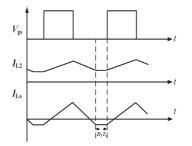
Volume 5 Issue 9, September 2016 <u>www.ijsr.net</u> Licensed Under Creative Commons Attribution CC BY The inductor currents of  $L_2$  and  $L_o$  during this mode are given by

$$\frac{li_{L2}}{dt} = -\frac{V_{ac}(t)}{L_n}$$
$$\frac{li_{L0}}{dt} = -\frac{V_0(t)}{L_n}$$

Mode 3  $[t_2 - t_3]$ :



**Figure 3.5:** Equivalent circuit in mode III (switch  $S_1$  is turned off)



**Figure 3.6:** Theoretical DCM waveforms during one switching period  $T_S$  in mode III (switch  $S_1$  is turned off)

During this interval, only diode  $D_p$  conducts to provide a path for  $L_2$ , as shown in Fig. 3.5. Accordingly, the inductors  $L_2$  and  $L_0$  in this interval behave as constant current source. Thus, the voltage of inductors  $L_2$  and  $L_0$  is zero. Capacitor  $C_2$ is being charged by the inductor current  $i_{L2}$  and the energy of capacitor  $C_0$  is released to load. This is a freewheeling mode. The theoretical waveforms in this mode are shown in Fig. 3.6 This mode lasts until the start of a new switching period. The turn off time of the switch and the output diode is given by

$$T_{off} = T_S - t_{on} - t_{don}$$

where  $t_{on}$  is the conducting interval of switch  $S_1$ , and  $t_{don}$  is that of the output diode  $D_0$ . The normalized length of mode II period can be obtained as follows:

$$D_2 = \frac{D_1}{M} sin\omega_t$$

where  $\omega$  is the line angular frequency, and M is the voltage conversion ratio (M =  $\frac{V_0}{V_c}$ ).

# 4. Simulation of Bridgeless Cuk PFC Rectifier with Negative Output Voltage

Design parameters and simulation circuit of Bridgeless Cuk PFC rectifier with positive output voltage

Parameters	Values
Input Voltage	(90-130) V <sub>rms</sub>
Switching Frequency, f <sub>s</sub>	50 KHz
Input Inductor, L <sub>1</sub> & L <sub>2</sub>	1mH
Output Inductor,L <sub>0</sub>	22µH
Capacitor, $C_1 \& C_2$	.luf
Output Capacitor	1000uf

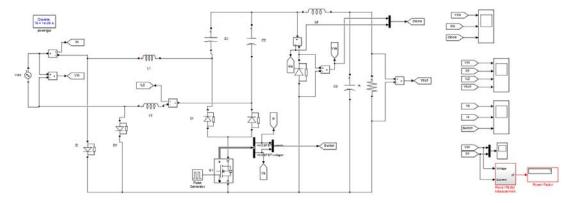


Figure 4.1: Simulation of Bridgeless Cuk PFC rectifier with positive output voltage

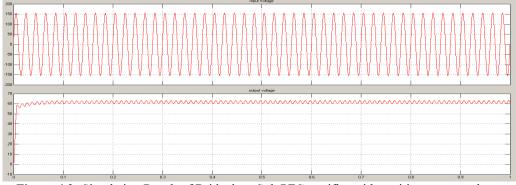
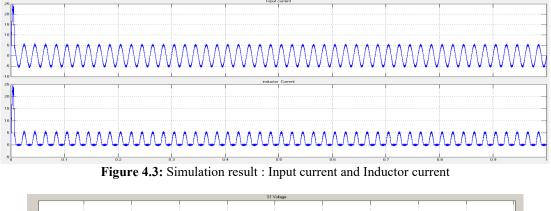


Figure 4.2: Simulation Result of Bridgeless Cuk PFC rectifier with positive output voltage

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International Journal of Science and Research (IJSR) ISSN (Online): 2319-7064 Index Copernicus Value (2013): 6.14 | Impact Factor (2015): 6.391



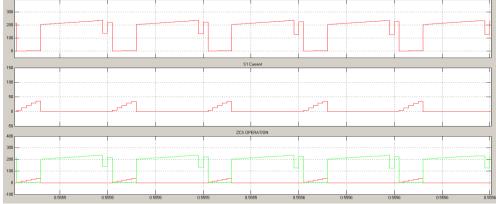


Figure 4.4: Simulation result :ZCS turn on of switch

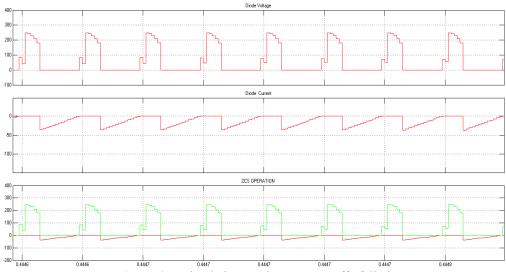
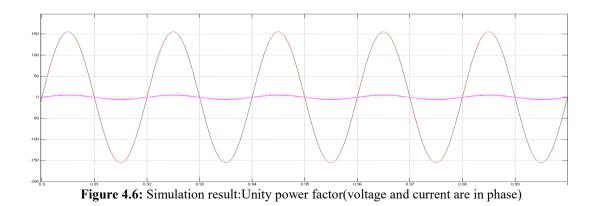


Figure 4.5: Simulation result :ZCS turn off of diode



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Figure 4.7: Hardware implementation of Bridgeless Cuk PFC rectifier with positive output voltaare made

## 6. Conclusion

The Cuk PFC rectifier with positive output voltage has been analyzed . The simulation results have shown good agreements with theBpredicted waveforms analyzed in the converter. The PF of the circuit has unity above at all the specified input and output conditions. Moreover, with higher efficiency and high PF, the Cuk PFC rectifier with positive output voltage is able to be applied to most of the consumer electronic products of 150-Wrating in the market. In addition, with only a single switch employed, the implemented system control circuit is simple to achieve high PF by applying any pulse width modulation control integrated circuit.

# References

- [1] Power Factor Correction (PFC) Handbook, ON Semiconductor, Denver, CO, USA, Rev."4, Feb. 2011
- [2] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC recti\_er with reduced components and conduction losses", IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 41534160, Sep. 2011.X. H. Yu, C. Cecati, T. Dillon, and M. G. Simoes, The new frontier of smartgrid, IEEE Trans. Ind. Electron. Mag., vol. 15, no. 3, pp. 4963, Sep. 2011.
- [3] T. Ching-Jung and C. Chern-Lin, "A novel ZVT PWM Cukpowerfactor corrector ", IEEE Trans. Ind. Electron., vol. 46, no. 4, pp. 780787, Aug. 1999.
- [4] Y. Jang and M. M. Jovanovic, "Bridgeless high-powerfactor buck converter", Trans. Power Electron, vol. 26, no. 2, pp. 602611, Feb. 2011
- [5] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode Sepic and Cuk power factor preregulators: Analysis and design", IEEE Trans. Ind. Electron., vol. 44, no. 5, pp. 630637, Oct. 1997.
- [6] M. Mahdavi and H. Faarzanehfard "Bridgeless CUK power factor correction rectifier with reduced conduction losses "IET Power Electron., vol. 5, no. 9,pp. 17331740, Nov. 2012.
- [7] M. Brkovic and S. Cuk, "Input current shaper using Cuk converter ", in Proc. 14thIEEE Telecommun. Energy Conf., Oct. 1992, pp. 53253
- [8] Y. S. Roh, Y. J. Moon, J. G. Gong, and C. Yoo, \Active power factorcorrection (PFC) circuit with resistor-free