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Comparative Analysis of a Low Power and High Speed Hybrid 1-Bit Full Adder for ULSI Circuits

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Abstract: ***Full adder circuit is a basic building block for designing any arithmetic circuits. Due to high demands and need for low and high speed digital circuits with small silicon area scaling trends have increased tremendously. In this paper a new high speed full adder circuit is proposed with very less static and dynamic power dissipation which occupies less silicon area when compared with existing techniques. For 1.8-V supply at 180µm technology the average power consumption (0.306mw) was found to be extremely low with a delay of 728.54ps. Correspondingly values of the same are found to be 0.034mw and 44.235ps with 1.2V supply at 130nm technology. The design was further extended for implementing 32-bit full adder and is found to be efficiently working with only 23.3088ns(1.41552ns) delay and 9.792mw(1.088mw) power at 180µm (130nm) technology for 1.8V(1.2V) supply voltage. In comparison with the existing full adder designs the proposed circuit offers significant improvement in terms of area, speed and power.***

Keywords: carry propagation, gate diffusion, high speed, low power, logic styles

1. Introduction

Battery operated electronic gadgets, like smart phones, Personal Digital Assistants (PDAs),and notebooks demand Ultra Large Scale Integrated circuits designs with an improved power-delay characteristics. For all the aforementioned applications, full adders is one of the basic building block and remains as a key focus domain fir the researchers. Even though many logic styles were proposed each have its own advantages and bottlenecks in implementing one bit full adder. These logic styles can be broadly classified into two categories, i.e. static style and dynamic style[1]. Static full adders even though are more reliable, but occupy more on-chip area with complex logic styles.

Standard static Complementary CMOS logic style[1] has 28 transistors. This full adder is based on regular CMOS structure with conventional pull-up and pull-down transistors providing full swing outputand good driving capabilities.

Other advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing and thus reliable operation at low voltage and arbitrary transistor sizes. The main drawback is the existence of the pMOS block, because of its low mobility compared to the nMOS devices. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a pMOS and anMOS device. Mirror adder is static complementary style full adder which is designed to improve speed of the carry block. The P logic tree allows output to be changed high, while the N allows to be discharged to ground.Static CPL[8] gate which consists of two nMOS logic networks and two small pull-up pMOS transistors used for swing restoration, and two output inverters having good driving capabilityused for the complementary output signals. The advantages of the CPL style are the small input loads, and the fast differential stage due to the cross coupled pMOS pull-up transistors. Other disadvantages are the substantial number of loads and high wiring overhead due to the dual-rail signals and the inefficient realization of simple gates.The TFA[8] design was improved with 16 transistors which is based on the transmission function theory and maintains full output voltage swing operation. The basic advantage of 10T[8] full adders is smaller area and low power utilization. It becomes not moreeasyand even obsolete to keep full output voltage swing operation as the design with fewer transistor count and lower power utilization are pursued. The Fourteen transistors fulladder, as the name implies uses 14Transistors[8] to realize the adder function. The 14Tfull adder cell, like the transmission function full adder cell, implements the complementary pass logic to drive the load.

Dynamic Full Adder24T[8] is based on bridge style. The body of the FA24T has 4 transistors less than static CMOS.The main disadvantage is sum generator should wait to receive the Cout generator which increases the delay. In DPL[8] style, both logic networkspMOS and nMOS are used in parallel. This provides full swing on the output signals(i.e., no level restoration circuitry is needed), the number of transistors especially large pMOS transistors and the number of nodes is quite high, leading to substantial capacitive loads. The combination of large PMOS transistors and inefficient dual-rail logic marks DPL not competitive compared to other pass-transistor logic styles and to complementary CMOS. Note that DPL can be regarded as a dual-rail pass-gate logic, while CMOS+ is a single-rail pass-gate logic.

2. Design Approach of the Existing Full Adder

The existing full adder circuit is represented by three blocks as shown in fig1(a).module1 and module2 are the XNOR modules that generate the sum signal (SUM) and module3 generates the output carry signal(c_{out}).each module is designed individually such that the entire adder circuit is optimized in terms of power, delay, and area. These modules are discussed below in detail.

A. XNOR Module

In the existing full adder circuit, XNOR module is responsible for most of the power consumption of the entire

adder circuit. therefore, this module is designed with avoiding the voltage degradation possibility .fig. 1(b) shows the modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors being small) formed by transistors Mp1 and Mpn [fig 1(b)].Full swing of the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3[fig1(b)].various XOR/XNOR topologies have already been reported .the XOR/XNOR reported uses four transistors but at the cost of low logic swing.to the contrary,the XOR/XNOR reported uses six transistors to get better logic swing compared with that of 4T XOR/XNOR .in this paper also the XNOR module employed 6T,but having different transistor arrangement than that of 6T XOR/XNOR .the modified XNOR presented in this paper offers low-power and high speed(with acceptable logic swing)compared with 6T XOR/XNOR.

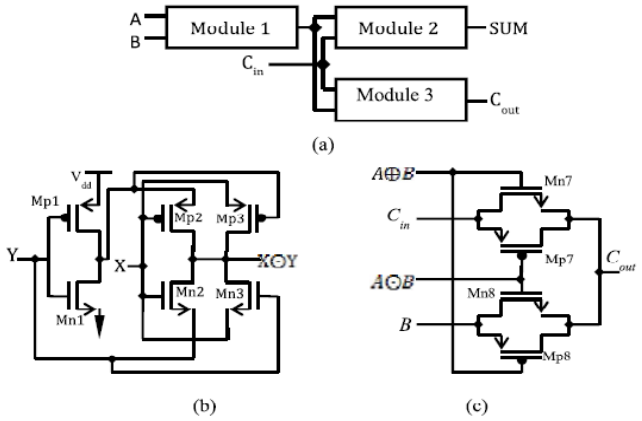

Figure 1: (a) Schematic structure of existing full adder (b)XNOR module(c) Carry generation module.

B. Carry Generation Module

The output carry signal is implemented by the transistors Mp7,Mp8,Mn7 and Mn8in the existing circuit asshownin fig 1(c). The input carry signal(c_{in}) propagates only through a single transmission gate (Mn7 andMp7),reducing the over all in carry propagation path significantly. The use of transmission gates(channel width of transistors Mn7,Mp7,Mn8 and Mp8 is made large) guarantee the further reduction in propagation delay of the carry signal.

C. Operation of Existing Technique

Fig. 2 shows the detail diagram of the proposed full adder. The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B', which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem, which has been removed using two pass transistors Mp3 and Mn3. pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6) realize the second stage XNOR module to implement the complete SUM function. Analyzing the truth table of a full adder, the condition for *C*out generation has been deducted as follows:

If A=B thenC_{out}=B

If A≠B then C_{out}=C_{in}

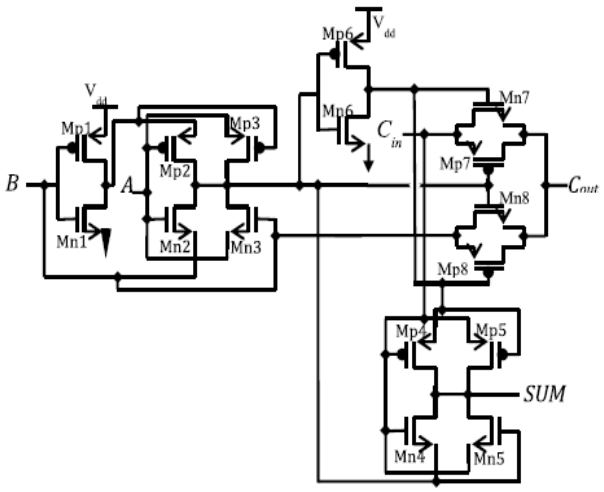

Figure 2: Existing Full Adder Circuit

The parity between inputs A and B is checked by *A*_ *B* function. If they are same, then *C*out is same as B, whichis implemented using the transmission gate realized bytransistors Mp8 and Mn8. Otherwise, the input carry signal(*C*in*)* is reflected as *C*out which is implemented by anothertransmission gate consisting of transistors Mp7 and Mn7.

3. Proposed Method

Proposed method is based on the use of a simple cell as shown in Figure 3. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: (1) proposed cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in proposed design method. As can be seen in [3], proposed cell structure is different from the existing PTL techniques and has some important features, which allows improvements in design complexity level, transistor counts, static power dissipation and logic level swing.

XOR and XNOR functions are the key variables in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. In this new cell, we have used the proposed technique for generating of XOR and XNOR functions. It uses only six transistors to generate the balanced XOR and XNOR functions, as shown in Figure 4.

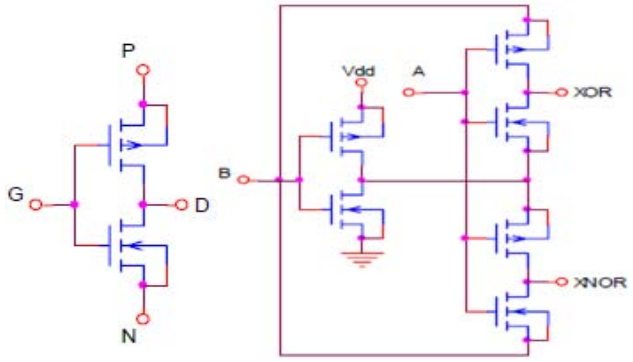

Figure 3: Proposed basic cellFig4: XOR/XNOR cell in proposed full adder

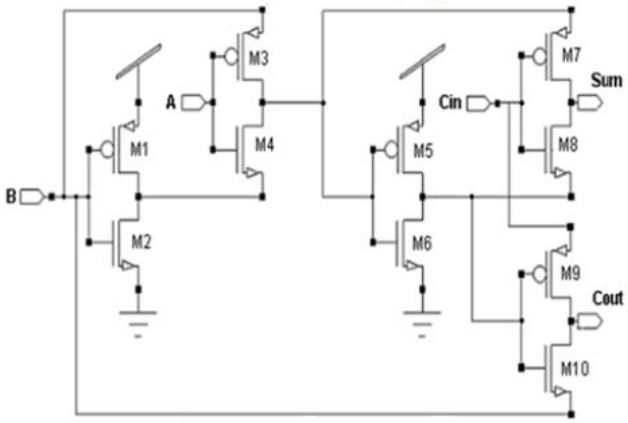

Figure 5: Proposed Full Adder Circuit

Fig5 is the proposed full adder circuit which is responsible for reduction of power consumption,delay, area to greater extent as compared with existing full adders.

4. Performance Analysis of Full Adders

Various full adder techniques are compared in terms of area delay and power with the existing and proposed full adders. All the above discussed techniques are simulated in mentor graphics and tanner EDA tools and the values are tabulated below. From the following tables we observe that the proposed fulladder occupies very less area, consumes less power and shows very less carry propagation delay.

Table 1: Simulation Results For Full Adder In 180um Technology With 1.2V Supply

Design	*Average Power(µW)*	*Delay (ns)*	*PDP*	*Transistors*	*References*
C-CMOS	11.21	1.09961	12.3266281	28	5,8
MIRROR	10.97	2.54	27.8638	28	7
CPL	13.08	3.13554	41.0128	32	1,8
TFA	4.73	1.96711	9.3044	16	8
TGA	2.62	2.04	5.3448	20	3
14T	1.08	1.707	1.8435	14	8
10T	1.1949	2.11	2.5212	10	8
HPSC	9.99	1.01997	10.1895	22	8
24T	8.71	1.51915	13.2317	24	8
FA_HYBRID	10.81	1.44464	15.6146	24	3
FA_DPL	11.39	3.1	35.3090	22	1,8
FA_SR_CPL	11.39	2.03711	23.2026	20	1,4
FA_TG_CMOS	0.86418	0.91068	0.78699	16	8
PROPOSED	0.3068	0.72854	0.223516	10	-

Table 2: Simulation Results for Full Adder in 130nm Technology with 1.8V Supply

Designs	*Average Power(µW)*	*Delay(ns)*	*PDP(ff)*	*Transistor*	*References*
CMOS	0.39	50.198	19.57722	28	5,8
MIRROR	0.33	50.1177	16.538841	28	7
CPL	2.3	50.2147	115.49381	32	1,8
TFA	0.36	100.0137	36.0049	16	8
TGA	0.36	49.985	17.9946	20	3
14T	0.72	2.19	1.5768	14	8
10T	0.316	2.55	0.8058	10	8
HPSC	0.379	10.782	4.096	22	8
24T	0.42	50.1345	21.05649	24	8
FA_HYBRID	0.36	50.1981	18.071316	24	3
FA_DPL	0.79	2.04	1.6116	22	1,8
FA_SR_CPL	0.21	50.1851	10.538871	20	1,4
FA_TG_CMOS	0.042	0.06476	0.00271992	16	8
Proposed	0.034	0.0442351	0.0015039934	10	-

5. Calculation of Power Consumption

In hybrid full adder's Power consumption is classified into two categories.they are 1) static power and 2) dynamic and short-circuit powerStatic power is due to biasing and leakage currents[2]. This static power is low when compared to the dynamic part in CCMOS implementations. When compared with the over alldynamic power, the over all static power is very low and is 519pw for 1.8v supply in 130nm technology which is less than the dynamic power but in this, the ratio of static and dynamic power[2] is increased which is due to increase in subthreshold conduction current and gate leakage. The increase in dynamic power is due to charging anddischarging of load capacitances.[12] The summation of fixed capacitance and variable capacitance is load capacitance as shown in below equation(1):

$$C_{load}=C_{fix}+C_{var} \quad (1)$$

Load capacitance is equal to sum of fix and variable capacitances, where as 1)C_{fix} is technology dependent and interconnect dependent capacitance. Interconnect dependent capacitance is minimized by efficient layout design. 2)C_{var} is of input capacitance and part diffusion capacitance dependent and can be minimized by proper sizing of transistors

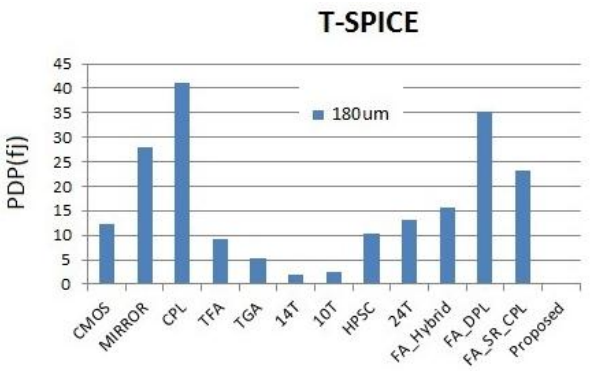

Figure 6: Comparison of PDP of various full adder designs

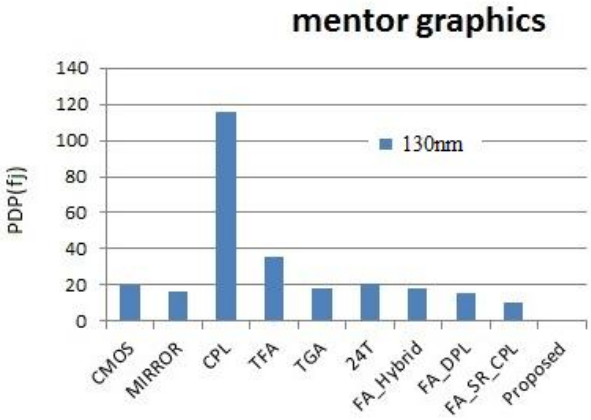

Figure 7: Comparison of PDP of various full adder designs

The effective parameter for reducing dynamic power consumption is to reduce the transistor size. Transistor sizes are enclosed according to the design. They were varied according to thepreviously set values to get the best performance in terms of power and delay.

6. Calculation of Propagation Delay

In most of the systems, adder is the fundamental computational unit and hence its delay governs the overall speed performance of the entire systems. The speed of response of an adder depends upon the propagation delay of carry signal which is minimized by reducing path length of carry signal. The carry signal propagates only through single transmission gate. The carry propagation path is minimized which substantially reduces the propagation delay. The delay is further reduced by efficient transistor sizing and by incorporating strong transmission gates.

The transmission gate between signals *C*in and *C*out as shown in figure (2) will be in the ON state[12]. The simulation results incorporating the gradual increase in the number of stages of full adders also validated this second order rise in delay with increase in the number of stages.

Figure 10: Total propagation delay for different stages

The simulation resultswere measured for no load capacitance (130-nm technology) and the worst case carry propagation delay is represented here. Incorporation of the load capacitance increased the delay but the nature of the graph remained the same. The buffers were included at appropriate stages of full adder chain, to minimize the overall delay. For efficient incorporation of buffers at appropriate stages, analytical evaluation was performed by extracting capacitance and resistance values from the postlayout simulation results.The delay of the buffers is independent of the number of stages, *m*, and its value is obtained by intermediate delay calculation. For achieving the minimum carry propagation delay, the appropriate number of stages, *m*, is further authenticated by the practical simulation results as in fig(10).

7. Performance of 32-Bit Full Adder

A 32-bit carry propagation adder is implemented as an extension of the proposed 1-bit full adder. It is a noncarry look-ahead adder structure where the carry propagation takes place all the way to the last adder block. The performance evaluation of this 32-bit adder was also carried out in 130nm and 180µm technologies with and without using intermediate buffers at appropriate stages. Both power consumption and carry propagation delay was improved after using buffer; however, the delay improvement was more significant. The performance of this 32-bit full adder at supply voltage of 1.8 V (130-nm technology) and 1.2 V

(180µm technology) is shown Fig(11). The difference in static and dynamicpower consumption is large in 130-nm technology. But, this difference was somewhat reduced in 180µm technology because of increase in the sub-threshold conduction current and gate leakage. Fig.(12) shows the behavior of the carry propagation delay when extended from 1 to 32 bits. It is observed that the carry propagation delay increased almost linearly with respect to the proposed 1-bit full adder.

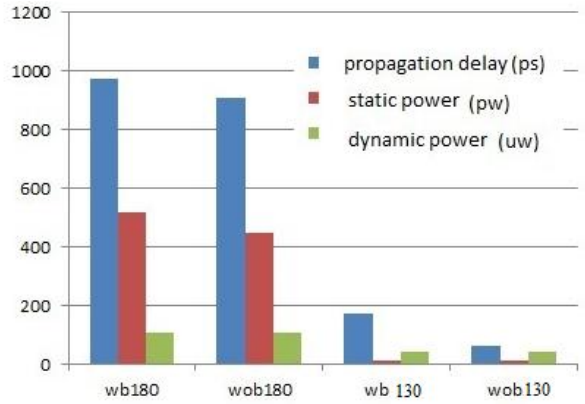

Figure 11: Performance of 32-bit carry propagation adder with and without buffer with supply voltage of 1.8V/1.2V

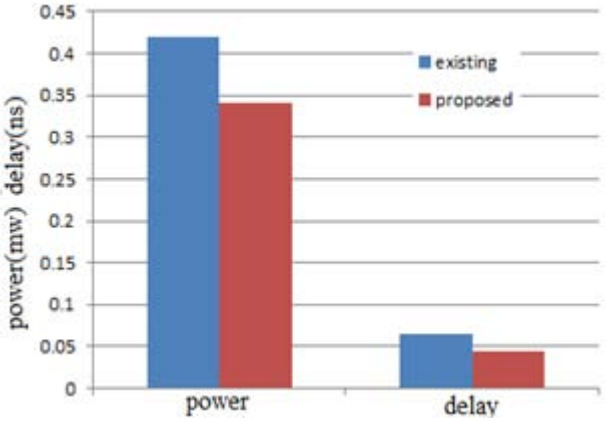

Figure 12: Comparison of existing and proposed technique in 130 nm technology

8. Conclusion

In this paper, a low power hybrid one bit full adder has been proposed and the design is extended for 32-bit. The simulation was carried out using tanner EDA and mentor graphics tools with 180µm and 130nm technology and compared with other standard design approaches like mirror, 14T, 10T, majority based, FA_DPL, FA_SR_CPL and hybrid CMOS full adder. The power delay product of the proposed adder was greatly improved when compared with earlier techniques. The efficient usage of CMOS inverters in the proposed technique lead to fast switching speed with very less count of 10 transistors. The implementation of different kinds of mixed and digital integrated circuits and we carried out using this superior gate induced 10T based full adders circuit.

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