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A PV Powered High Gain Input-Parallel Output-Series DC/DC Converter with Dual Coupled Inductors

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Abstract: ***High voltage gain dc-dc converters are required in many industrial applications. Here a novel input-parallel output-series boost converter with dual coupled inductors and a voltage multiplier module for solar source is going to be designed. The primary windings of two coupled inductors are connected in parallel to share the input current and reduce the current ripple at the input. The secondary sides of two coupled inductors are connected in series to a regenerative capacitor by adiode for extending the voltage gain and balancing the primary currents. In addition, the active switches are turned on at zero current and the reverse recoveryproblem of diodes is alleviated by reasonable leakage inductances of the coupled inductors. Besides the converter has low voltage stress across the switches andenergy of leakage inductances of the coupled inductors can be recycled.***

Keywords: DC–DC converter, dual coupled inductors, high gain, input-parallel output-series, leakage inductance

1. Introduction

We know that energy consumption is increasing day by day. But limited availability of energy sources has become an inevitable global problem. Hence efficient use of energy and its conservation is of great importance. Currently, environmental protection is a primary concern, in which available energy from natural resources is developed for ease of use. Such developments are also designed to generate inexpensive and effective energy sources while highlighting the importance of minimizing environmental destruction and pollution. Solar energy is one of the most extensively exploited sources of effective natural energy. An increasing number of countries and research institutions infuse substantial manpower and monetary investments in solar energy based projects. Solar energy is advantageous compared to any other renewable energy sources available. The efficient and fast growth in the field of solar energy result in Photovoltaic (PV) system design for various application with reliable operation. Given global attention, photovoltaic (PV) power systems have been increasingly explored. PV module represents the fundamental power conversion unit of a PV generator system.

2. Topology of the Converter

The converter consists of two parts. These two parts are named a modifed interleaved boost converter and a voltage doubler module using capacitor-diodeand coupled inductor technologies. The topology of the converter is shown in Figure 2.1.The basic boost converter topology is shown in Figure 2.1(a) and Figure 2.1(b) is another boost versionwith the same function in which the output diode is placed on the negative dc-link rail. Figure 2.1(c) is called a modified inter-leaved boost converter, which is an input-parallel and output-series configuration derived from two basic boost types. Therefore, this part based on interleavedcontrol has several main functions:

1) It can obtain double voltage gain of the conventional interleaved boost converter.
2) Low output voltage ripple due to the interleaved series connected capacitors.
3) Low switch voltage stresses.

Then, the double independent inductors in the modified interleaved boost converter are separately replaced by the primary windings of coupled inductors that are employed as energy storage and filtering as shown in Figure 2.1(d).The secondary windings of two coupled inductors are connected in series for a voltage multiplier module, which is stacked on the output of the modifed converter to get higher voltage gain. This connection is also helpful to balance thecurrents of two primary sides. The coupling references of the inductors are denoted by the marks "*" and ".". Equivalent circuit of the converter is as shown in Figure 2.2 where

L_{m1}, L_{m2} : magnetizing inductances
L_{K1}, L_{K2} : leakage inductances
C_1, C_2, C_3 : output and clamp capacitors
S_1, S_2: main switches
D_1, D_2: clamp diodes
D_r, C_r : regenerative diode and capacitor
D_3 : output diode
N :turns ratio of $\frac{N_S}{N_P}$
V_{N1}, V_{N2} : the voltage on the primary sides of coupled inductors.

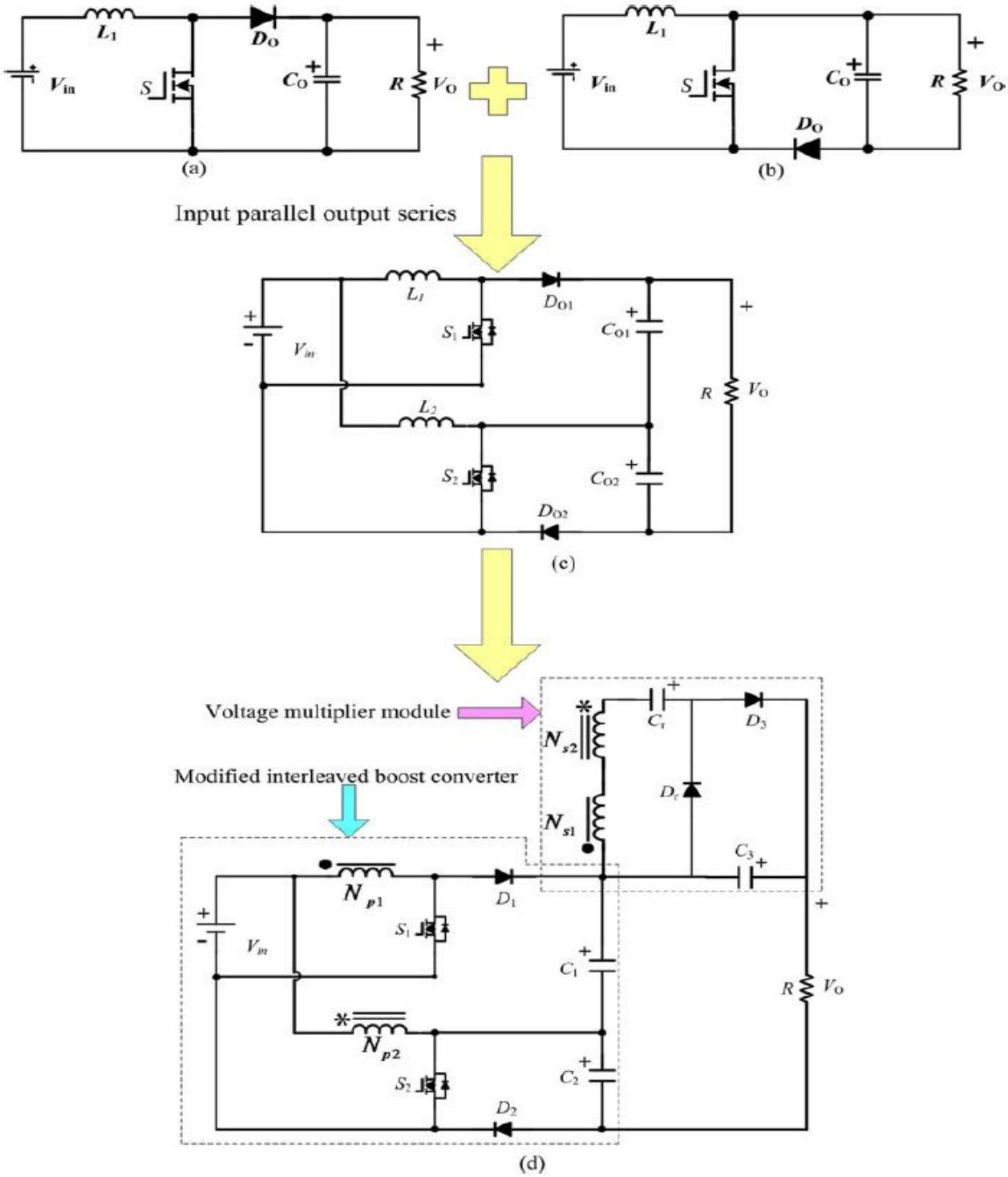

Figure 2.1: Topology of the converter with high voltage gain.(a) Conventional boost converter. (b) Other structure of boost converter. (c) The modified interleaved boost. (d) A high gain input-parallel output-series DC/DC converter with dual coupled-inductors.

The converter is operated in continuous conduction mode (CCM).The duty cycles of the power switches are interleaved with 1800 phase shift, and the duty cycles are greater than 0.5.Therefore the two switches can only be in one of three states as S_1: ON, S_2: ON; S_1: ON, S_2: OFF; S_1: OFF, S_2 : ON. This ensures normal transmission of energy from the coupled inductor's primary side to the secondary one.

3. Operation of the Converter

The converter is operated in continuous conduction mode. Operation of the converter can be explained through eight modes.

Mode 1 [$t_0 - t_1$]:
At time $t = t_0$, the power switch S_1 is turned on with zero-current switching (ZCS) due to the leakage inductance L_{K1},while S_2remains turned ON, as shown in Figure 3.1.Diodes D_1,D_2 , and D_r are turned OFF, and only output

diode $D_3$is conducting. The current falling rate through the output diode $D_3$is controlled by the leakage inductances L_{K1} and L_{K2},which alleviates the diode's reverse recovery problem. This stage ends when the current through the diode D_3decreases to zero.

Mode 2 [$t_1 – t_2$]:
During this interval, both the power switches S_1 and $S_2$are maintained turned ON, as shown in Figure 3.2. All of the diodes are reversed-biased. The magnetizing inductances L_{m1} and L_{m2} as well as leakage inductances L_{K1} and $L_{K2}$are linearly charged by the input voltage source V_{in}. This period ends at the instant t_2 , when the switch S_2 is turned OFF.

Mode 3 [$t_2 – t_3$]:
At time $t = t_2$, the switch S_2 is turned OFF, which makes the diodes $D_2$and D_r turned ON. The current flow path is shown in Figure 3.3. The energy that magnetizing inductance L_{m2} has stored is transferred to the secondary sidecharging the capacitor C_r by the diode D_r , and the current through the diodeD_r and the capacitor C_r is determined by the leakage inductances L_{K1} and L_{K2}.The input voltage source, magnetizing inductance L_{m2} and leakage inductance L_{K2} release energy to the capacitor C_2 via diode D_2.

Mode 4 [$t_3 – t_4$]:
At time $t = t_3$, diode D_2 automatically switches OFF because the total energy of leakage inductance L_{K2} has been completely released to the capacitor C_2. There is no reverse recovery problem for the diode D_2. The current flow path of this stage is shown in Figure 3.4. Magnetizing inductance L_{m2}still transfers energy to the secondary side charging

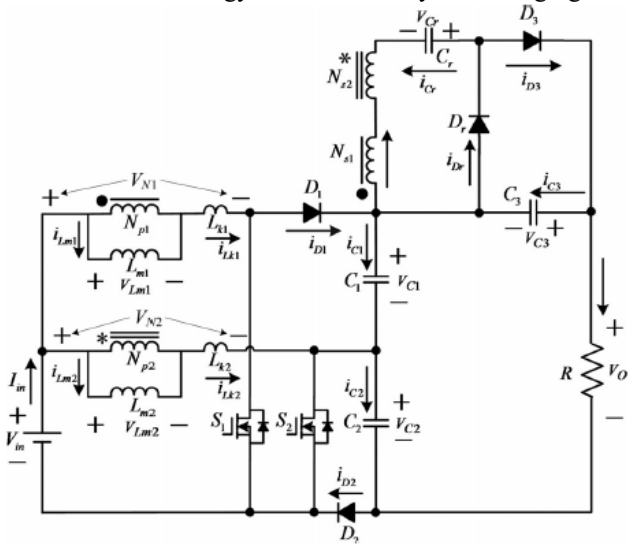

Figure 2.2: The equivalent circuit of the converter

the capacitor C_r via diode D_r. The current of the switch S_1 is equal to the summation of the currents of the magnetizing inductances L_{m1} and L_{m2}.

Mode 5 [$t_4 – t_5$]:
At time $t = t_4$, the switch S_2 is turned ON with ZCS soft-switching condition.Due to the leakage inductance L_{K2} and the switch S_1remains in ON state. The current flow path of this stage is shown in Figure 3.5. The current fallingrate through the diode D_r is controlled by the leakage inductances L_{K1} and L_{K2},which alleviates the diode reverse recovery problem. This stage ends when the current through the diode D_r decreases to zero at $t = t_5$.

Mode 6 [$t_5 – t_6$]:
The operating states of stages 6 and 2 are similar as shown in Figure 3.6. During this interval, all diodes are turned OFF. The magnetizing inductances $L_{m1}$and L_{m2} , and the leakage inductances L_{K1} and L_{K2} are charged linearly by the input voltage. The voltage stress of D1 is the voltage on C1, and the voltage stress of D2 is the voltage on C2. The voltage stress of $D_r$is equivalent to the voltage on C_r, and the voltage stress of D_3 is the output voltage minus the voltages on C_1 and C_2 and C_r .

Mode 7 [$t_6 – t_7$]:
The power switch S_1 is turned OFF at $t = t_6$, which turns ON D_1 and D_3 , andthe switch S_2 remains in conducting state. The current flow path of this stage is shown in Figure 3.7. The input voltage source V_{in} , magnetizing inductance L_{m1} and leakage inductance L_{K1} release their energy to the capacitor C_1via the switch S_2 . Simultaneously, the energy stored in magnetizing inductor $L_{m1}$is transferred to the secondary side. The current through the secondary sides in series flows to the capacitor C_3 and load through the diode D3.

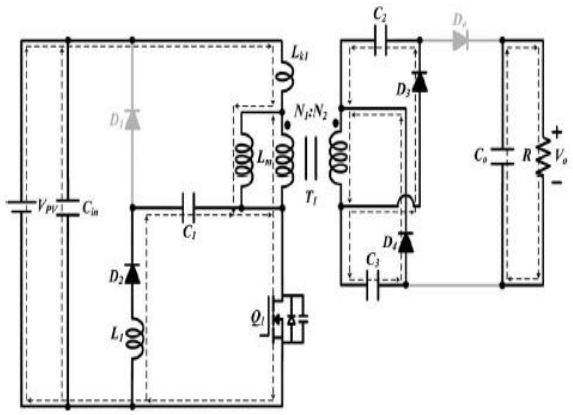

Figure 3.1: mode 1

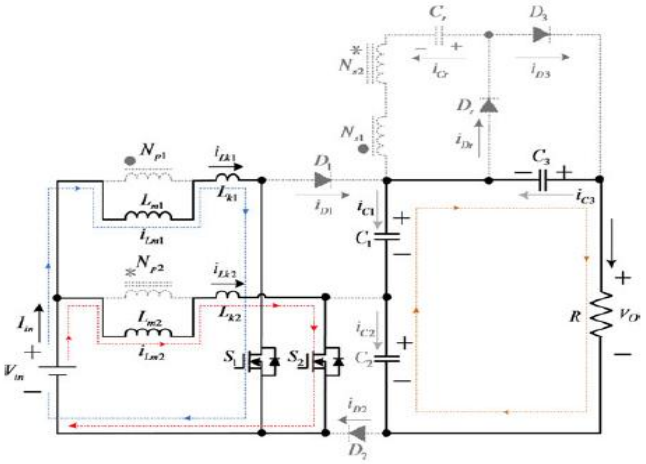

Figure 3.2: mode 2

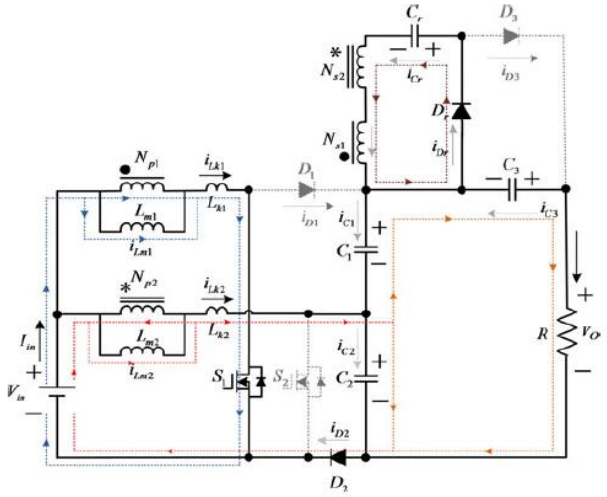

Figure 3.3: mode 3

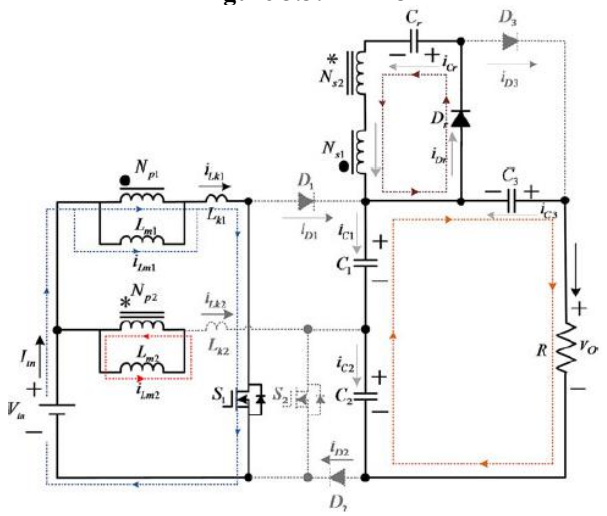

Figure 3.4: mode 4

Mode 8 [$t_7 - t_8$] :

At time t = t_7 , since the total energy of leakage inductance L_{K1}has been completely released to the capacitor C_1 , diode D_1automatically switches OFF as shown in Figure 3.8. The current of the magnetizing inductance $L_{m1}$is directly transferred to the output through the secondary side of coupled inductor.

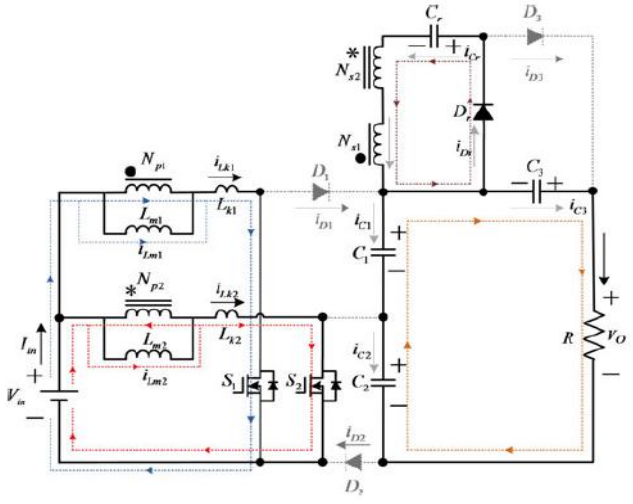

Figure 3.5: mode 5

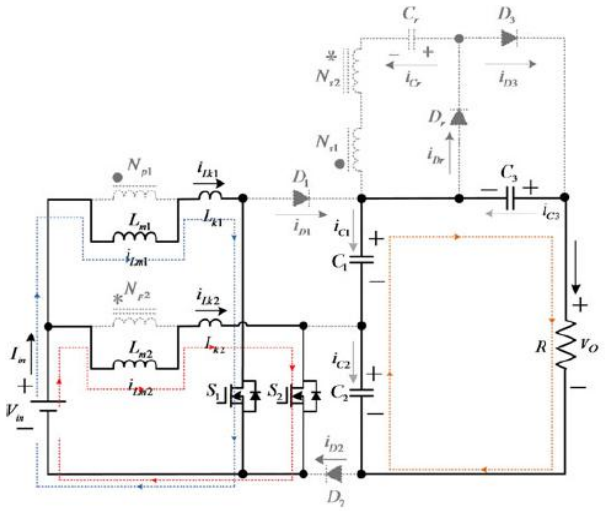

Figure 3.6: mode 6

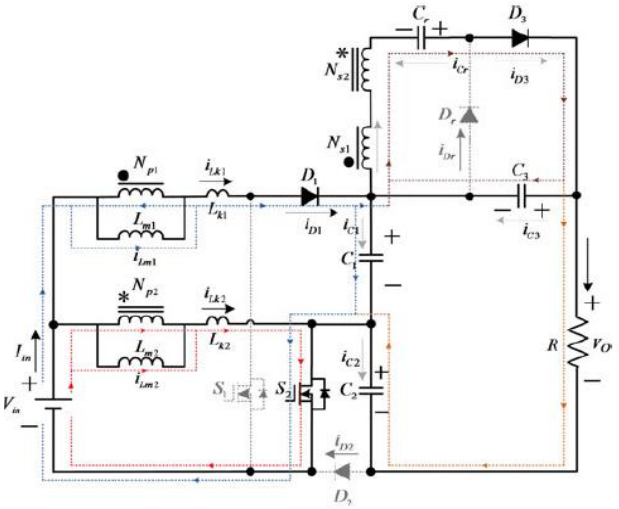

Figure 3.7: mode 7

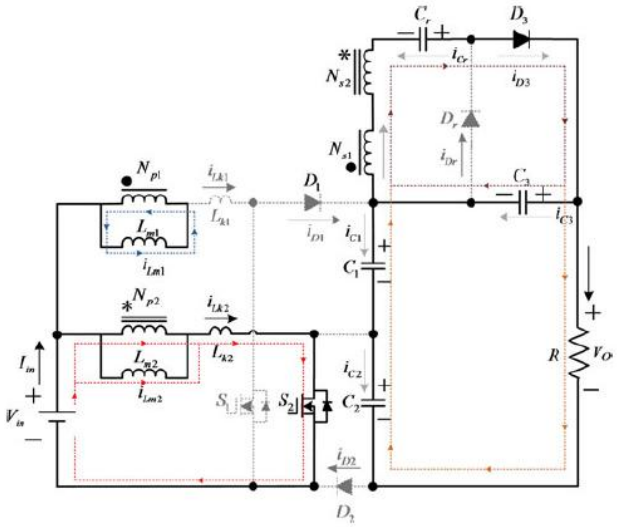

Figure 3.8: mode 8

4. Steady State Analysis of the Converter

To simplify the circuit performance analysis of the converter in continous conduction mode, the following assumptions are made.

1) All of the power devices are ideal. That is to say, the on-state resistance $R_{DS(ON)}$ and all parasitic capacitors of the

main switches are neglected, and the forward voltage drop of the diodes is ignored.
2) The coupling-coefficient k of each coupled inductor is defined as $L_m/(L_m+L_K)$. The turn ratio N of each coupled inductor is equal to N_S/N_P.
3) The parameters of two coupled inductors are considered to be the same, namely $L_{m1} = L_{m2} = L_m$, $L_{K1} = L_{K2} = L_K$, $N_{S1}/N_{P1} = N_{S2}/N_{P2} = N$, and $k_1 = L_{m1}/(L_{m1} + L_{K1}) = k_2 = L_{m2}/(L_{m2} + L_{K2}) = k$.
4) Capacitors C_1, C_2, C_3, and C_r are large enough. Thus, the voltages across these capacitors are considered as constant in one switching period. The time durations of modes I, IV, V, and VIII are significantly short, hence only stages II, III, VI, and VII are considered for the steady-state analysis.

A Voltage gain

If the transient characteristics of circuit are disregarded, each magnetizing inductance has two main states in one switching period. In one state, the magnetizing inductance is charged by the input source. In the other state, the magnetizing inductance is discharged by the output capacitor voltage V_{C1} or V_{C2}minus the input voltage.

At stages II and VI, following equations can be written

$$V_{Lm1}^{II} = V_{Lm1}^{VI} = kV_{in} \quad (1)$$
$$V_{Lm2}^{II} = V_{Lm2}^{VI} = kV_{in} \quad (2)$$
$$V_0 = V_{C1} + V_{C2} + V_{C3} \quad (3)$$

At mode III, the following equations are written.

$$V_{Lm1}^{III} = kV_{in} \quad (4)$$
$$V_{Lm2}^{III} = k(V_{in} - V_{C2}) \quad (5)$$
$$V_{Cr} = V_{S1} - V_{S2} = kNV_{C2} \quad (6)$$

During the time duration of mode VII, the following voltage equations can beexpressed.

$$V_{Lm1}^{VII} = k(V_{in} - V_{C1}) \quad (7)$$
$$V_{Lm2}^{VII} = kV_{in} \quad (8)$$
$$V_{C3} = V_{Cr} + V_{S2} - V_{S1} = kN(V_{C1} + V_{C2}) \quad (9)$$

Using the volt-second balance principle on L_{m1} and L_{m2} respectively, voltage across capacitors are obtained as

$$V_{C1} = V_{C2} = \frac{V_{in}}{(1-D)} \quad (10)$$
$$V_{Cr} = \frac{kNV_{in}}{(1-D)} \quad (11)$$
$$V_{C3} = \frac{2kNV_{in}}{(1-D)} \quad (12)$$

Hence voltage gain can be written as

$$M_{CCM} = \frac{V_0 2(kN+1)}{V_{in}(1-D)} \quad (13)$$

Neglecting the impact of leakage inductances of the coupled inductor,coupling coefficient k is equal to one.Thus ideal voltage gain is rewritten as

$$M_{CCM} = \frac{V_0 2(N+1)}{V_{in}(1-D)} \quad (14)$$

B. Voltage and current stress analysis

To simplify the voltage stress analyses of the components, the leakage inductance of coupled inductor and the voltage ripples on the capacitors are ignored. The voltage stresses on power switches S_1 and $S_2$are derived as

$$V_{S1-stress} = V_{S2-stress} = \frac{V_{in}}{(1-D)} = \frac{V_0}{2(1+N)} \quad (15)$$

This confirms that low-voltage-rated metal-oxide-semiconductor field-effect transistors with low $R_{DS(ON)}$can be adopted for the proposed converter to reduce conduction losses and costs.The voltage stresses on the diodes D_1,D_2,D_3 , and D_r related to the turns ratioand the output voltage can be derived as

$$V_{D1-stress} = \frac{2V_{in}}{(1-D)} = \frac{V_0}{(1+N)} \quad (16)$$
$$V_{D2-stress} = \frac{V_{in}}{(1-D)} = \frac{V_0}{2(1+N)} \quad (17)$$
$$V_{D3-stress} = V_{Dr-stress} = \frac{2NV_{in}}{(1-D)} = \frac{NV_0}{(1+N)} \quad (18)$$

The average currents that pass through output capacitors C_1, C_2, C_3 , and C_r are equal to the output current at modes II and VI, which are given by

$$I_{C1} = I_{C2} = I_{C3} = -\frac{V_0}{R} \quad (19)$$

At mode III, the currents owing through each capacitor are written by

$$I_{C1} = I_{C3} = -\frac{V_0}{R} \quad (20)$$
$$I_{C1} = I_{D2} = I_{C3} = -\frac{V_0}{R} \quad (21)$$
$$I_{C1} = I_{Dr} \quad (22)$$

At mode VII, the average currents that pass through output capacitors are

$$I_{C1} = I_{D1} + I_{C3} + I_{Cr} \quad (23)$$
$$I_{C2} = -\frac{V_0}{R} \quad (24)$$
$$I_{C3} = I_{D3} - \frac{V_0}{R} \quad (25)$$
$$I_{C1} = -I_{Dr}$$

Using the amp-second principle on capacitors, the average currents of the diodes D_1,D_2,D_3 , and D_r can be derived

$$I_{D1} = I_{D2} = I_{D3} = \frac{V_0}{(1-D)R} \quad (26)$$

Similarly, according to the steady operating principle, the average currents of the power switches are given by

$$I_{S1} = \frac{D}{(1-D)} I_{D1} = \frac{DV_0}{(1-D)^2 R} \quad (27)$$
$$I_{S2} = \frac{D}{(1-D)} I_{D2} + \frac{1}{(1-D)} I_{D1} = \frac{(D^2-D+1)V_0}{(1-D)^2 R} \quad (28)$$

5. PV Modelling

Modelling of PV is done on the basis of single diode model as shown in Fig 5.1.Itconsists of a current source in anti parallel with a diode, a series resistance indicating internal resistance to the current ow, and a parallel resistance indicatingleakage current.

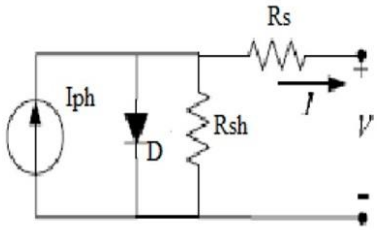

Figure 5.1: Solar cell model

The voltage-current characteristics equation of a solar cell is given as

$$I = N_P I_{ph} - N_P I_s \left(\exp\left(\frac{q(V+IR_{SM})}{KT_C A}\right) - 1\right) \quad (29)$$
$$R_{SM} = \frac{N_S R_S}{N_P} \quad (30)$$

where $I_{ph}$is a light generated current or photo-current,$I_s$is the cell saturation of dark current,q is the electron charge,k is Boltzmann's constant,T_c is the cell's working temperature,A is an ideal factor,$R_{sh}$is shunt resistance, and $R_s$is the series resistance of the solar cell. The photocurrent

mainly depends on the solar insolation and cell's working temperature, whichis described as

$$I_{ph} = [I_{SC} + K_I(T_C - T_{ref})]H \quad (31)$$

where I_{sc} is the cell's short-circuit current at a 25^0C and 1kW/m^2 KI is the cell's short circuit current temperature coefficient, T_{ref} is the cell's reference temperature and H is the solar insolation in kW/m^2 On the other hand, the cell's saturation current varies with the cell temperature,which is described as

$$I_{S=}I_{RS}\left(\frac{T_C}{T_{ref}}\right)^3 \exp\frac{qE_G(T_C - T_{ref})}{T_{ref}T_C KA} \quad (32)$$

Where I_{RS} is the cell's reverse saturation current at a reference temperature andstandard solar radiation, E_G is the band-gap energy of the semiconductor usedin the cell and A is the ideal factor,dependent on PV technology.

6. MPPT Perturb and Observe Algorithm

A typical solar cell converts only 30 to 40 percent of the incident solar radiation into electrical energy. Maximum power point tracking is done to improve the efficiency of the solar panel. MPPT is used to maximize the PV array output power irrespective of the temperature and in solation conditions. For any given set of operating conditions, cells have a single operating point where the values of current and voltage of the cell result in maximum power output. In order to continuously harvest maximum power from the solar panels, they have to operate at their maximum power point despite of inevitable changes in the environment. There are different types of MPPT techniques. They include pertub and observe incremental conductance, constant voltage, short circuit pulse etc...Choice of algorithm depends on the time complexity the algorithm takes to track the maximum power point, implementation cost and the ease of implementation. Hereperturb and observe algorithm is used.

Perturb and observe algorithm uses hill climbing technique in which operating point of a solar cell moves in the direction of increasing direction of power. In this method operating voltage and current of PV panel is sensed and new power is compared with the previous power. Figure 6.1 shows the perturb and observe algorithm.

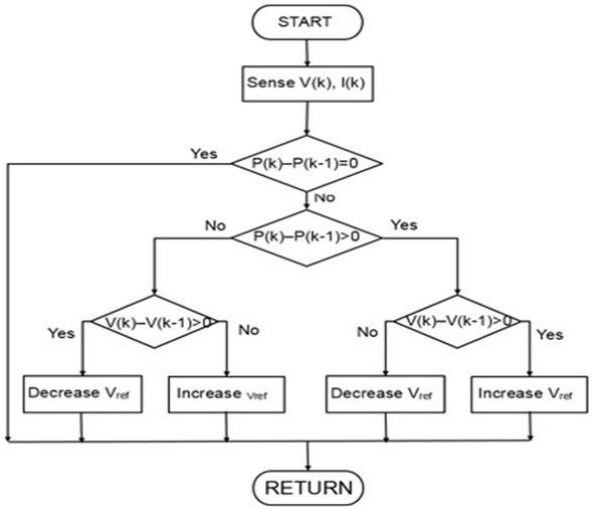

Figure 6.1: Flowchart of perturb and observe algorithm

7. Simulation and Results

Simulations were done to test the performance of the converter by using simulink/MATLAB software. Circuit used for simulation is as shown in Figure 7.1.PV subsystem is shown in Figure 7.2.

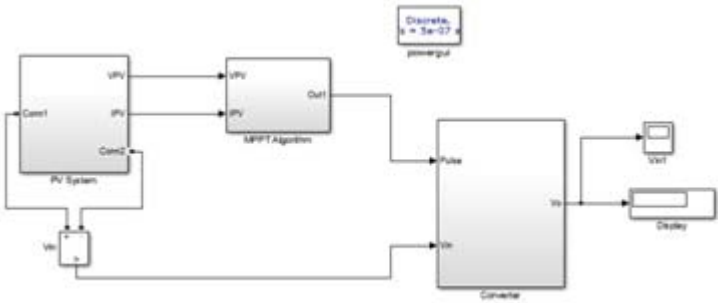

Figure 7.1: Simulation circuit of converter

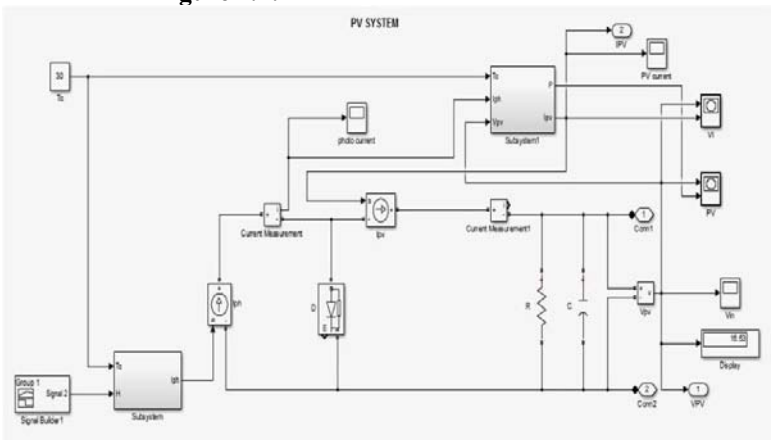

Figure 7.2: PV subsystem

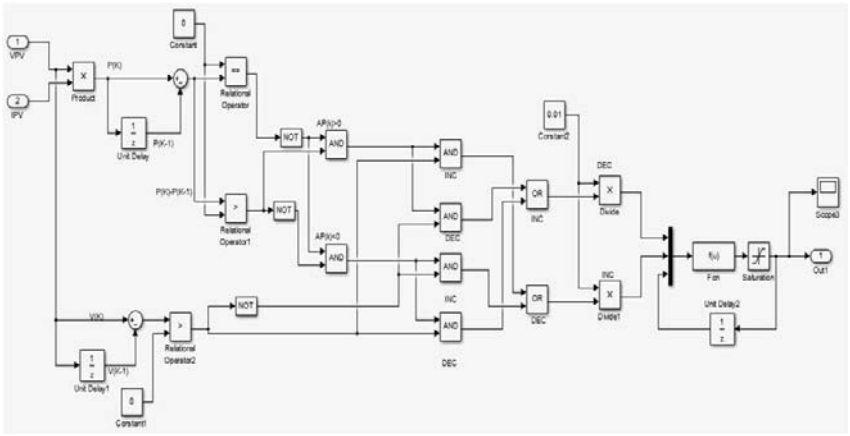

Figure 7.3: P& O MPPT algorithm

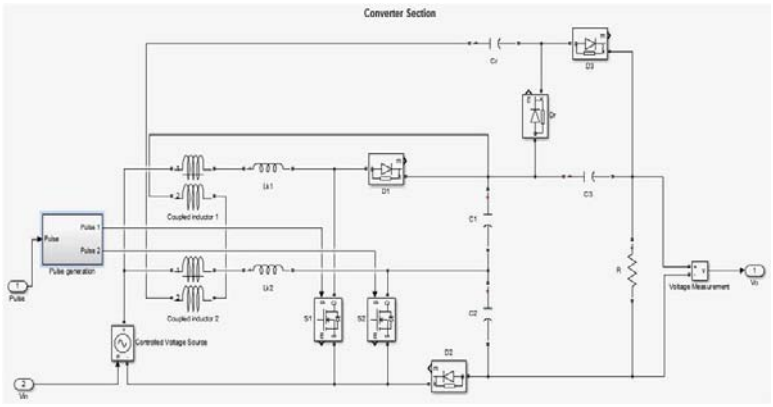

Figure 7.4: Converter section

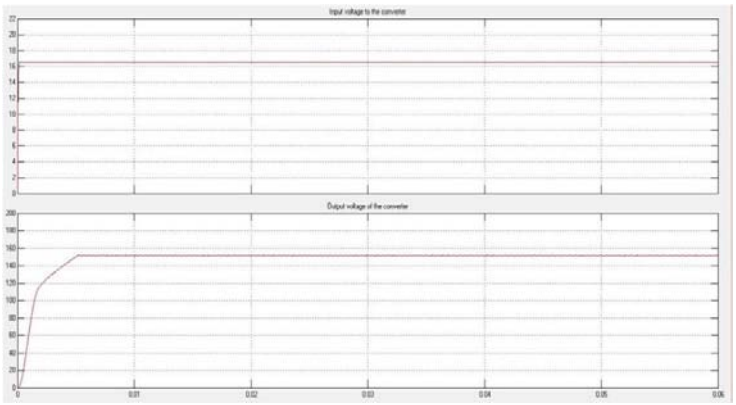

Figure 7.5: Input & Output voltage waveforms

8. Conclusion

For low input-voltage and high step up power conversion, this paper has successfully developed a high-voltage gain dc–dc converter by input-parallel output-series and inductor techniques. The key theoretical waveforms, steady-state operational principle, and the main circuit performance are discussed to explore the advantages of the proposed converter. Performance of the converter is simulated using MATLAB/SIMULINK software. From simulation circuit, we can see that the converter can achieve a much higher voltage gain and avoid operating at extreme duty cycle and numerous turn ratios. The main switches can be turned ON at ZCS so that the main switching losses are reduced. The current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated.

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