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Direct Digital Synthesizer using Numerically Controlled Oscillator for Signal Generation

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Abstract: ***The Direct Digital Synthesizer is implemented with the numerically Controlled Oscillator. The Direct Digital Synthesis is an advanced method of producing analogue waveforms where the generation is done completely in the digital sphere. This paper presents a design for a Direct Digital Synthesizer (DDS) which generates multiple waveforms. The proposed NCO is based on a 32 bit phase accumulator and a 12 bit addressed look-up table (LUT) as phase to amplitude converter. This design will be simulated in Xilinx12.3. This DDS will offer qualities like fast switching, good frequency resolution and good stability. This DDS can become highly convenient if it is designed on a Field Programmable Gate Array (FPGA). A FPGA-based system requires less development cycle and reduced space for design also increase the performance.***

Keywords: NCO, DDS, LUT, Xilinx, Phase accumulator

1. Introduction

Waveform generation is highly important in high speed wireless applications such as radar, telecommunication systems, instrumentation and many other fields. The common waveform generators were used the Direct analog synthesizers (DAS). They generated frequency by adding frequencies from distinct crystal and harmonics. The most common used analog waveform synthesizer uses the phase detector and a VCO called as analog Phase locked loop (PLL). These analog waveform synthesizers had slow switching time with poor frequency resolution, less flexibility and bulky.

Direct digital synthesis (DDS) based on numerically controlled oscillators (NCO) is an predictable method for generating quasi-periodic sinusoid signals at any time with high frequency resolution, fast changes in frequency and phase with high spectral purity of the output signal are required. The performance of NCO in signal quality and stability as compared to other methods (e.g., voltage-controlled oscillators, VCO), by considerable hardware complexity and a frequency limit by Nyquist theorem.

Now days FPGAs are very popular for implementing digital circuits due to less time to market, easy for programming at the consumer level compared to ASIC. So implementation of the DDS on FPGA makes our device highly efficient.

Also till now the main focus was on the generation of sine wave only but multiple waveform generation will increase the region of application. VHDL a Hardware Description language is generally used for design and simulation.

2. Literature Review

IreneuszJaniszewski, Bernhard Hoppe, and Hermann Meuth [1] proposed an hybrid function generation for sine wave generation with high-precision NCOs, which combines traditional LUTs with the iterative procedures of the CORDIC algorithm. This paper results with SNR(dB)=92 with word length of 16 bit.

Gopal D. Ghiwala, Pinakin P. Thaker, GireejaD.Amin [5] proposed the simulation and synthesis of NCO. The Design and Realization of NCO includes Phase Accumulator and Look-Up Table. In this paper proposed system is design for output frequency 2.5MHz with 24bits word length.

Snehal Gaikwad, Kunal Dekate [6] proposed Direct Digital Synthesizer is done at clock frequency which is specified as normalize value relative to clock rate given. as it is dual Oscillator, hence it support variable Width, Phase modulation and user defined frequency resolution with 5MHz output frequency.

Matt Bergeron and Alan N. Willson [15] proposed an architecture that used an angle rotation algorithm. This algorithm is used for phase to amplitude conversion. The architecture used phase accumulator of 32 bit and the clock frequency fclk is 1GHz which gives an output frequency of 400 MHz on Xilinx Virtex version 7 FPGA dissipate only 54.9mW.

3. Overview of NCO

A. Concept of NCO

Numerically Controlled Oscillator is constructed using ROM with samples of a sine wave saved in it (sine LUT) [5]. Fig.2 represents the block diagram of a NCO system. The NCO produces continues signals at a certain frequency selective word (FSW) which determines the phase. Once set, this FSW determines the signal frequency to be produced. Phase accumulator output continuously produces proper binary words representing the instant phase to the look-up table function.

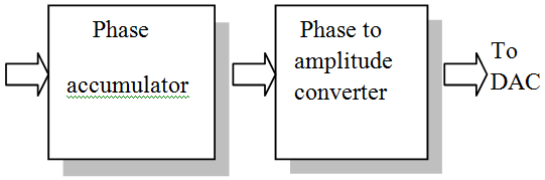

Figure 2: Block Diagram of NCO

Block Diagram of NCO is as shown in fig.2. The NCO will made up of phase accumulator and phase to amplitude converter. This phase to amplitude converter is nothing but Look up Table to convert phase to amplitude [15].

The frequency of the output signal for 32-bit system is determined by following equation

$$Fout = \frac{W \ Fclk}{2^{32}} \quad (1)$$

Where W is the FSW,
N=32 is the number of bits that the phase accumulator can handle
Fclk is system clock.

4. Direct Digital Synthesizer

The proposed DDS system is to overcome the problem of adjusting the output frequency. It gives us to produce wide range of output frequency. The block diagram of Direct Digital Synthesizer is as shown in Fig. 3. It will be composed on reference clock, a frequency control register with 32 bit binary word, a Numerical Control Oscillator (NCO) and a Digital to analog converter (DAC). NCO generates digital sine wave and it will convert into analog by DAC.

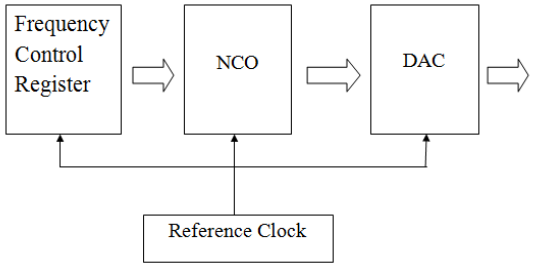

Figure 3: Block Diagram of DDS

The design will be simulated by Xilinx ISE tool and MODELSIM software which would be used to see the analog waveforms.

A. Performance detail of DDS

The frequency of the DDS can be controlled using the FSW (Frequency Selective Word).The output frequency will be determined by the FSW [6].

$$Fdds = FSW * \frac{Fclk}{2^N} \quad (2)$$

Where Fclk = Clock Frequency
The output frequency can be increased by changing the FSW.

B. Frequency Resolution

The frequency resolution of the direct digital synthesizer is a function of the applied referenced clock frequency and number of bits (N) employed in phase accumulator. The frequency resolution can be calculated using the formula given below [7]:

$$\Delta f = \frac{Fref}{2^N} \quad (3)$$

Where Δf = frequency resolution in Hz
In order to obtained improved frequency resolution, numbers of bits entered in the phase accumulators are increased.

C. Signal-to-Noise Ratio

Signal-to-noise ratio traditionally used to characterize spectral quality of a signal and it will determine by the formula [1]:

$$SNR(dB) = 6.02\ AW + 1.8. \quad (4)$$

By considering errors in 1- LSB amplitude so replacing AW by aw − 1, the SNR for aw = 32 is 188 dB.

5. Design of Submodules of DDS

A. Design of phase to amplitude converter

This section of DDS contains a Look up table in a Read only memory (ROM). This LUT is used to convert the phase accumulator's output value which is linear amplitude information of waveforms [14]. It is basically a memory which stores sampled 12 bit binary values which are stored in hexadecimal format. These values act as amplitudes which are taken into account as integer values. The phase accumulator gives output in 32 bit binary value. If we use all the 32 bits as address, we would require 4.29GB space for the look up table. Hence it gives phase truncation [15]. So we use only the top 12 bits of phase accumulator to address the LUT. Therefore the total required memory locations to store the amplitude values are only $2^{12} = 4096$.

B. Design of phase accumulator

The block diagram of phase accumulator as shown in Fig.4 which is consists of a divider, a multiplier and an adder. The accumulator structure will be 32 bit word. Here the phase incrementer stores a binary value which is the key factor in deciding the resultant frequency. The phase increment (W) is achieved by the divider and the multiplier which is shown by the formula [14]:

$$Phase\_inc(W) = \left(\frac{fout}{Fclk}\right) * 2\text{^}32 \quad (5)$$

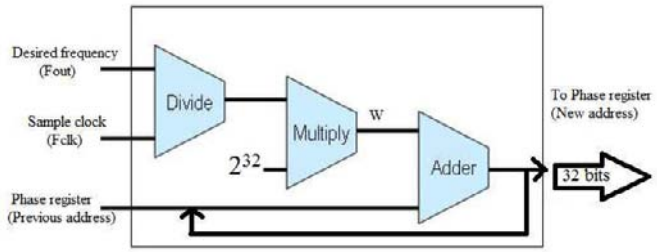

Figure 4: Block Diagram of phase accumulator

On each tick of the clock pulse, the adder will add the phase increment value (W) with the output of adder which is the result of previous clock pulse because of the feedback connection. This process gives help for some slope to the waveform.

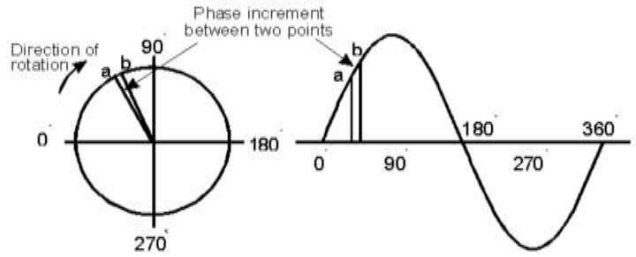

Figure 5: Digital Phase wheel

As shown in Fig. 5 the phase accumulator function is represented as a digital phase wheel representing 360º. The complete sine wave oscillation can be supposed as a point moving around the circle. Each designated point like a, b as shown in Fig. 5 corresponds to equivalent point on the cycle of the sine wave. One complete rotation gives one complete oscillation of the wave. If cycle is complete the rotation starts over again [15]. The number of points on the cycle is generally determined by N which is 32 here i.e 2^{32} points. But due to phase truncation the number of points equals to 2^{12}. So the address "000000000000" corresponds to 0º and the address "111111111111" is equal to 359.98º. The distance between two points a and b can determined by the value of W which is the phase increment. Hence the output frequency can be changed by changing the value of W. For higher frequency, W should be large and vice versa.

6. Simulation Results

The above discussed modules are simulated and synthesized by Xilinx ISE Design Suite 12.3_1.

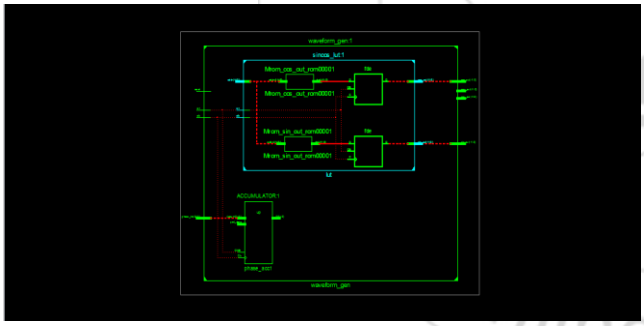

Figure 6: RTL view of NCO

The Fig. 6 shows RTL view of NCO. Consist of four inputs like clk, en, reset and phase_inc as FSW with four waveforms as output.

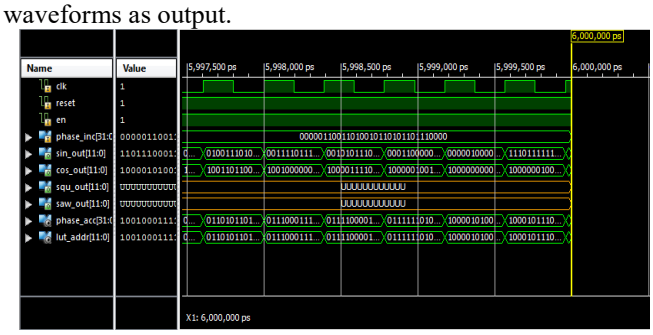

Figure 7: Simulation Result of NCO

The above Fig. 7 shows simulation result of NCO. Which receives Phase_inc value as Frequency Selective Word is "06696B70" with 2.55GHz clock frequency to generate 063.77MHz output frequency.

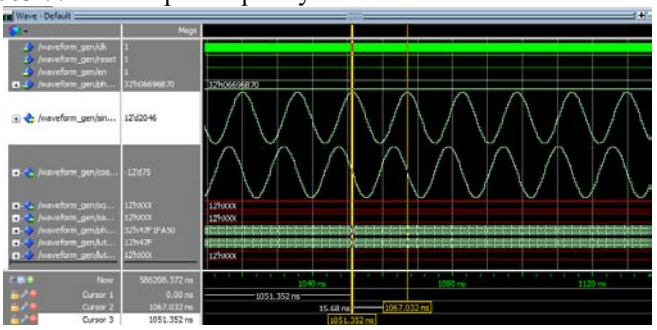

Figure 8: Simulation Result of DDS using ModelSim Simulator

The Fig.8 shows Simulation result of Direct Digital Synthesizer using ModelSim Simulator. This simulation represents sine and cosine wave with frequency 63.77MHz.

By using this technique we can calculate following parameters:

Below Table shows signal parameter that are calculated by generated signal and formulae.

Table 1: Calculated Signal Parameters

Parameter	Value
Reference Clock	2.55 GHz
Frequency Selective Word	06696B70
Desired Frequency	63.86 MHz
Actual Output Frequency	63.7755 MHz
Frequency Resolution	0.5937 Hz
Signal-to-Noise Ratio	188 dB

7. Conclusions

In this paper, we have presented different work done on FPGA based NCO. We have designed a 32 bit adder and a look up table for amplitude conversion. Multiple waveforms that are sine, cosine, square and saw tooth are generated increasing the area of application. Since these waveforms are of 12 bit each, the result will also have greater accuracy. We also have a phase resolution of 2Pi/4096 = 0.088 degrees. This complete design has the capability to produce waveforms in the MHz range.

8. Acknowledgment

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