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High Speed, Low Power Vedic Multiplier Using Reversible Logic Gate

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Abstract: ***Multipliers are very significant part of any processor or computing device. More often than not, performance of microcontrollers and DSP processors are calculated on the basis of number of multiplications completed in unit time. Therefore better multiplier architectures are assured to increase the capability of the device. Vedic multiplier is one such auspicious solution. Its easy architecture joined with raised speed forms an unparalleled combination for serving any composite multiplication computations. Attached with these best parts, realizing this with reversible logic further decreases power dissipation. Power dissipation is alternative significant constraint in an embedded system that cannot be ignored. In this paper we introduce a Vedic multiplier known as "UrdhvaTiryakbhayam", realized by reversible logic that is the first of its kind. This multiplier may find applications in Fast Fourier Transforms, and additional applications of DSP like software defined radios, imaging,wireless communications.***

Keywords: Vedic multiplier; Urdhva Triyagbhyam; Reversible logic; power; delay

1. Introduction

Vedic mathematics is the earliest Indian method of mathematics which in particular offers with Vedic mathematical formulae and their application to numerous branches of mathematics. Vedic mathematics was reconstructed from the earliest Indian scriptures (Vedas) by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja after his study on Vedas. He made 16 sutras and 16 upa sutras after huge study in Atharva Veda. It has been found that UrdhvaTiryakbhayam is the extreme efficient among those. The splendor of Vedic mathematics lies in the fact that it reduces otherwise clumsy looking calculations in traditional mathematics to quite simple ones. This is so because the Vedic sutras are claimed to be mostly based on the natural ethics on which the human thought works. As a result multiplications in DSP blocks can be executed at faster rate. This is a totallyexciting subject and affords a small number of powerful algorithms which can be applied to various branches of engineering [2].

Reversible logic has received too muchconsideration in the recent years due to their capability to decrease the power dissipation which is the fundamentalnecessity in low power very large scale integration design. It has wide usages in low power complementary metal-oxide semiconductor and polymer computing,optical science,nanotechnology andquantum computation. Irreversible hardware working out results in energy dissipation due to data loss. [5]

Reversible logic is one of the encouraging fields for upcoming low power design technologies. Since one of the necessities of all digital signal processors and other handheld devices is to reduce power dissipation multipliers with lower dissipation and extreme speed are necessary. [6]

This paper is divided into six sections, section II gives the literature survey, section III gives details about the Vedic multiplication using Urdhva-Triyagbhyam algorithm, and section IV explains Reversible logic, section V gives the implementation details of design and section VI gives the result and its discussion.

2. Literarute Survey

As the scale of integration keeps increasing, more and more sophisticated signal processing systems are being realized on a VLSI chip. These signal processing uses not only demand excessive computation capability but also consume huge amounts of energy. While performance and space remain to be two major design areas, power consumption has become a critical concern in today's VLSI system design. Conventional (irreversible) hardware computation results in energy dissipation because ofdata loss. As per Landauer's study, the amount of energy dissipated for each irreversible bit operation is at least kTln 2 Joules, where k=1.3806505×10-23m2kg-2K-1 (Joule/Kelvin-1) is that the Boltzmann's constant and T is the temperature at which process is executed . The heat produced due to the loss of one bit of data is very minor at room temperature but when the amount of bits is large as in the case of high speed computational works the heat dissipated by them will be huge so that it affects the performance and effects in the reduction of lifetime of the components. [5]

Multiplication is a significant process in most signal processing systems. Multipliers have working frequency and processing capacity per chip, more current has to be carried and the heat because ofgreat power consumption must be removed by suitable cooling methods. Second, battery life in movable electronic devices is limited. Little power design directly leads to lengthyprocess time in these movable devices. Therefore designing multipliers having low-power consumption, smallest area is asignificant part in low-power VLSI system design. In [1] Shamim Akhter explained the new method of digit multiplication based on Vedic process of multiplication. This gives us technique for hierarchical multiplier design. [2] Honey DurgaTiwari, et.al. studied the Vedic multiplication formulae, Urdhva-Tiryakbhyam and Nikhilam, in detail.[3] Anvesh Kumar et. al. described that

the Vedic mathematics are going to decrease the quantity of adder and multiplier as compare to the conventional techniquesince as the number of adder reduces the size is also going to reduced. [4] PrabirSaha, et.al reported on a novel complex number multiplier design based on the methods of the ancient Indian Vedic Mathematics, highly suitable for high speed complex arithmetic circuits. [5] Rakshith T.R., et.al. proposed the Vedic multiplier using reversible logicwith reduced TRLIC and reduced delay. [8] R. Anitha, et.al design a 32 bit MAC unit using vedic multiplierand reversible logic gate.

3. Vedic Multiplication Using Urdhva-Triyagbhyam Algorithm

Operation of Vedic multiplier depends upon the Vedic sutras which were reconstructed by Shree Bharati Krishna. Urdhva-tiryakbhyam is the multiplication sutra (algorithm) in Vedic mathematics.Urdhva means vertical. Triyakbhyam means Crosswise. The multiplier is based on an algorithm Urdhva-tiryakbhyam (Vertical and Crosswise) of Vedic Mathematics. Urdhva-tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It accurately means vertically and crosswise. It is based on a novel concept through which the generation of all partial products can be done with the simultaneous addition of these partial products. The algorithm can be generalized for n × n bit number. [1][3]

Unlike other multipliers with theincrease in the number of bits of multiplicand and/ormultiplier the time delay in calculation of the product doesnot increase proportionally. Because of this fact the time ofcalculation is independent of clock frequency of theprocessor. Hence one can limit the clock frequency to a lowervalue. Figure 1 shows UrdhvaTiryagbhyam algorithm for binary multiplication

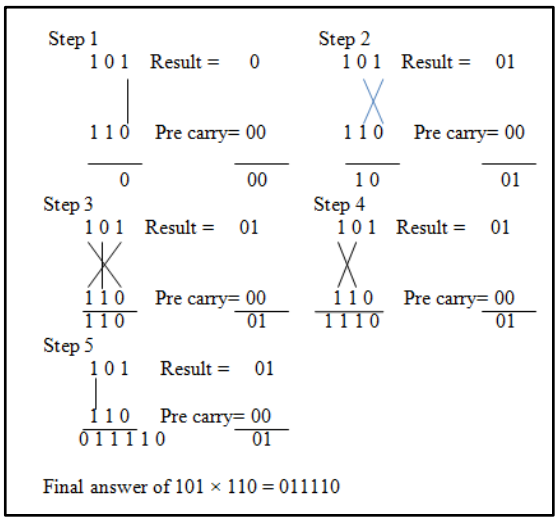

Figure 1: UrdhvaTiryagbhyam algorithm for binary multiplication

4. Reversible Logic

Conventional hardware computation results in energy dissipation due to data loss. The heat generated due to the loss of one bit of data is very minor at room temperature but when the amount of bits is more as in the case of high speed computational works the heat dissipated by them will be so huge that it affects the performance and effects in the decrease of lifespan of the components. Reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to decide the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. The reversible gates used for implementation of multiplier are as follows-

A. Basic Reversible Logic Gates[7]

1) *Feynman gate*: Fig 2 shows a 2×2Feynman gate. The input vector is I (P, Q) and the output vector is O (L, M). The outputs are defined by L=P, M=P xor Q. Quantum cost of a Feynman gate is 1.

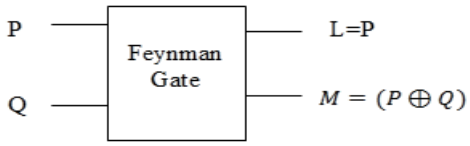

Figure 2: Feynman gate

2) *Peres gate:*The followingfigure 3 shows a 3×3Peres gate. The input vector is I (P, Q, R) and the output vector is O (L, M, N). The output is defined by L = P, M = P xor Q and N=PQ xor R. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowermost quantum cost.

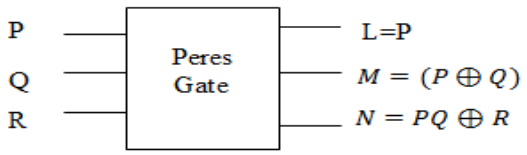

Figure 3: Peres gate

*3) HNG gate:*Fig 4 shows a HNG Gate. The input vector is I (P, Q, R, S) and the output vector is O (L, M, N, O).The full adder using HNG is obtained with R= Cin and S=0.

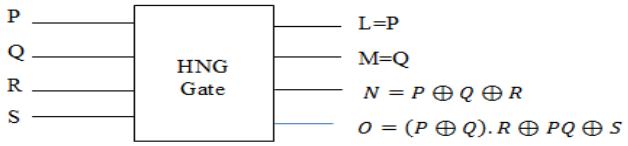

Figure 4: HNG gate

B. Features of reversible logic gates

A reversible logic circuit should have the following features-
1) Use minimum number of reversible gates.
2) Use minimum number of garbage outputs.
3) Use minimum constant inputs. [5]

5. Implementation of Vedic Multiplier Using Reversible Logic

An implementation of 4×4 bit Vedic multiplier which uses the 2×2 bit multiplier as a basic building block. So, here the sub modules are 2×2 bit Vedic multipliers, 4 bit Ripple carry adders which are also designed using reversible logic gates.[5]

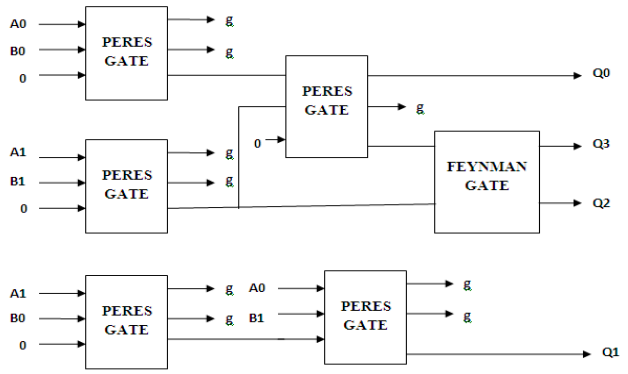

Figure 5: 2 X 2 UrdhvaTiryagbhyam Multiplier using reversible logic gate

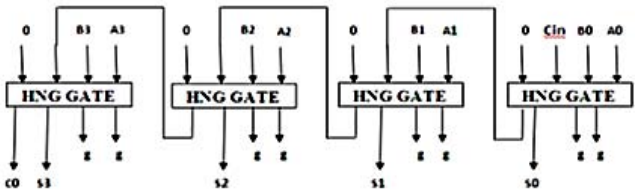

Figure 6: Four bit ripple carry adder using HN gate

The Ripple carry adder is the simple adder used for addition of the 4 bits and reversible RCA adder is implemented with the help of HN gate. There are three RCA adders used for 4 bit multiplication. Fig. 7 below shows the block diagram of the 4 bit Vedic multiplier.[6]

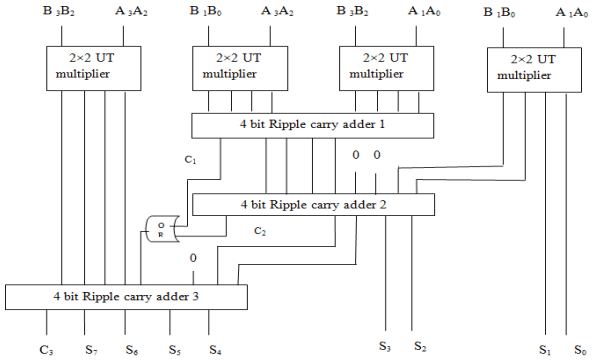

Figure 7: Block diagram of 4×4 Bit Vedic multiplier

6. Result

A. Simulation Result

Fig. 8 below shows the simulation result of the 4×4 bit reversible Vedic multiplier which uses the 2×2 bit Reversible Vedic multiplier and RCA adders in VHDL.

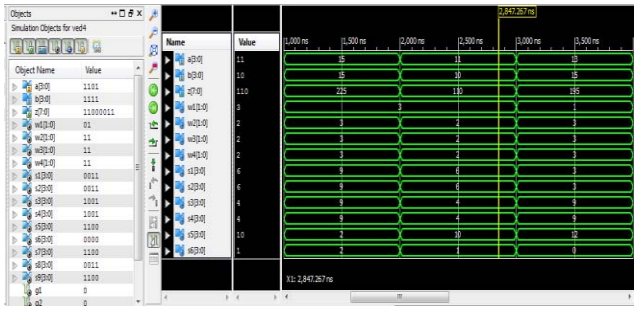

Figure 8: Simulation result of 4×4 bit reversible Vedic multiplier

B. Result

Synthesis of the designed multiplier is done using Xilinx ISE 12.1. In this the delay, Memory requirement is calculated and power consumption measured using the Xpower analyzer tool in Xilinx ISE 12.1. Table below represents the results after synthesis was done.

Table 1: Time delay of array and vedic multiplier

Multiplier	*Time delay in ns*		*Memory requirement in kilobytes*	
	Array multiplier	*Vedic Multiplier*	*Array multiplier*	*Vedic Multiplier*
4×4 bit	18.222	16.482	244556	244876
8×8 bit	35.048	29.535	250308	249228
16×16 bit	70.184	56.667	300876	264972

Table 2: Power consumption of vedic multiplier using conventional logic and reversible logic

Multiplier	*Time delay in ns*	
	Vedic Multiplier using conventional logic	*Vedic Multiplier using reversible logic*
4×4 bit	66.61	65.84
8×8 bit	84.01	79.52
16×16 bit	392.22	322.15

7. Conclusion

From the results, we can say that Vedic Multiplier is efficient than Conventional Multiplier. As the number of bit increases from 8 x 8 bit to 16 x 16 bit, the timing delay significantlydecreases for Vedic multiplier as compared to conventional multiplier. The time delay in Vedic multiplier for 16 x 16 bit number is 56.667 ns while the time delay for Conventional multiplier is 70.184 ns respectively. The memory required for 16 x 16 bit Vedic multiplier is 264972 kilobytes and Conventional multiplier required 300876 kilobytes. Thus Vedic multiplier shows the enhanced speed among the conventional multiplier and it also decreases the memory of the system.

The power consumption of vedic multiplier using reversible logic for 16 x 16 bit number is 322.15mW and using conventional logic is 392.22mW. Thus vedic multiplier using reversible logic shows reduced power consumption compare to vedic multiplier using conventional logic.

8. Acknowledgement

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