High Speed, Low Power Vedic Multiplier Using Reversible Logic Gate

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Abstract: Multipliers are very significant part of any processor or computing device. More often than not, performance of microcontrollers and DSP processors are calculated on the basis of number of multiplications completed in unit time. Therefore better multiplier architectures are assured to increase the capability of the device. Vedic multiplier is one such auspicious solution. Its easy architecture joined with raised speed forms an unparalleled combination for serving any composite multiplication computations. Attached with these best parts, realizing this with reversible logic further decreases power dissipation. Power dissipation is alternative architecture joined with raised speed forms an unparalleled combination for serving any composite multiplication computations. Therefore better multiplier architectures are assured to increase the capability of the device. Vedic multiplier is one such auspicious solution. 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the Vedic mathematics are going to decrease the quantity of adder and multiplier as compare to the conventional techniques since the number of adder reduces the size is also going to reduced. [4] PrabirSaha, et.al reported on a novel complex number multiplier design based on the methods of the ancient Indian Vedic Mathematics, highly suitable for high speed complex arithmetic circuits. [5] Rakshit T.R., et.al proposed the Vedic multiplier using reversible logic with reduced TRLIC and reduced delay. [8] R. Anitha, et.al design a 32 bit MAC unit using vedic multiplier and reversible logic gate.

3. Vedic Multiplication Using Urdhva-Triyagbhyam Algorithm

Operation of Vedic multiplier depends upon the Vedic sutras which were reconstructed by Shree Bharati Krishna. Urdhvatiryakbhyam is the multiplication sutra (algorithm) in Vedic mathematics. Urdhva means vertical. Triyakbhyam means Crosswise. The multiplier is based on an algorithm Urdhva-Tiryakbhyam (Vertical and Crosswise) of Vedic Mathematics. Urdhva-Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It accurately means vertically and crosswise. It is based on a novel concept through which the generation of all partial products can be done with the simultaneous addition of these partial products. The algorithm can be generalized for \( n \times n \) bit number. [1][3]

Unlike other multipliers with the increase in the number of bits of multiplicand and multiplier the time delay in calculation of the product does not increase proportionally. Because of this fact the time of calculation is independent of clock frequency of the processor. Hence one can limit the clock frequency to a lower value. Figure 1 shows Urdhva-Tiryagbhyam algorithm for binary multiplication.

4. Reversible Logic

Conventional hardware computation results in energy dissipation due to data loss. The heat generated due to the loss of one bit of data is very minor at room temperature but when the amount of bits is more as in the case of high speed computational works the heat dissipated by them will be so huge that it affects the performance and effects in the decrease of lifespan of the components. Reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to decide the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. The reversible gates used for implementation of multiplier are as follows-

A. Basic Reversible Logic Gates[7]

1) Feynman gate: Fig 2 shows a 2×2 Feynman gate. The input vector is I (P, Q) and the output vector is O (L, M). The outputs are defined by \( L = P \) and \( M = P \oplus Q \). Quantum cost of a Feynman gate is 1.

2) Peres gate: The following figure 3 shows a 3×3 Peres gate. The input vector is I (P, Q, R) and the output vector is O (L, M, N). The output is defined by \( L = P, M = P \oplus Q \) and \( N = PQ \oplus R \). Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowermost quantum cost.

3) HNG gate: Fig 4 shows a HNG Gate. The input vector is I (P, Q, R, S) and the output vector is O (L, M, N, O). The full adder using HNG is obtained with \( R = \text{Cin} \) and \( S = 0 \).

5. Implementation of Vedic Multiplier Using Reversible Logic

An implementation of 4×4 bit Vedic multiplier which uses the 2×2 bit multiplier as a basic building block. So, here the sub modules are 2×2 bit Vedic multipliers, 4 bit Ripple carry adders which are also designed using reversible logic gates[5]
The Ripple carry adder is the simple adder used for addition of the 4 bits and reversible RCA adder is implemented with the help of HN gate. There are three RCA adders used for 4 bit multiplication. Fig. 7 below shows the block diagram of the 4 bit Vedic multiplier.\[6\]

6. Result

A. Simulation Result
Fig. 8 below shows the simulation result of the 4×4 bit reversible Vedic multiplier which uses the 2×2 bit Reversible Vedic multiplier and RCA adders in VHDL.

Figure 5: 2 X 2 UrdhvaTiryagbhyam Multiplier using reversible logic gate

Figure 6: Four bit ripple carry adder using HN gate

Figure 7: Block diagram of 4×4 Bit Vedic multiplier

B. Result

Synthesis of the designed multiplier is done using Xilinx ISE 12.1. In this the delay, Memory requirement is calculated and power consumption measured using the Xpower analyzer tool in Xilinx ISE 12.1. Table below represents the results after synthesis was done.

Table 1: Time delay of array and vedic multiplier

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>Time delay in ns</th>
<th>Memory requirement in kilobytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array multiplier</td>
<td>Vedic multiplier</td>
<td>Array multiplier</td>
</tr>
<tr>
<td>4×4 bit</td>
<td>18.222</td>
<td>16.482</td>
</tr>
<tr>
<td>8×8 bit</td>
<td>35.048</td>
<td>29.535</td>
</tr>
<tr>
<td>16×16 bit</td>
<td>70.184</td>
<td>56.667</td>
</tr>
</tbody>
</table>

Table 2: Power consumption of vedic multiplier using conventional logic and reversible logic

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>Time delay in ns</th>
<th>Vedic Multiplier using conventional logic</th>
<th>Vedic Multiplier using reversible logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>4×4 bit</td>
<td>66.61</td>
<td>65.84</td>
<td></td>
</tr>
<tr>
<td>8×8 bit</td>
<td>84.01</td>
<td>79.52</td>
<td></td>
</tr>
<tr>
<td>16×16 bit</td>
<td>392.22</td>
<td>322.15</td>
<td></td>
</tr>
</tbody>
</table>

7. Conclusion

From the results, we can say that Vedic Multiplier is efficient than Conventional Multiplier. As the number of bit increases from 8 x 8 bit to 16 x 16 bit, the timing delay significantly decreases for Vedic multiplier as compared to conventional multiplier. The time delay in Vedic multiplier for 16 x 16 bit number is 56.667 ns while the time delay for Conventional multiplier is 70.184 ns respectively. The memory required for 16 x 16 bit Vedic multiplier is 264972 kilobytes and Conventional multiplier required 300876 kilobytes. Thus Vedic multiplier shows the enhanced speed among the conventional multiplier and it also decreases the memory of the system.

The power consumption of vedic multiplier using reversible logic for 16 x 16 bit number is 322.15mW and using conventional logic is 392.22mW. Thus vedic multiplier using reversible logic shows reduced power consumption compare to vedic multiplier using conventional logic.

8. Acknowledgement

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References


