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Ultra Low Power Design of Combinational Logic Circuits

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Abstract: ***The dynamic power utilization of CMOS circuits is constantly turning into a noteworthy worry in Very Large Scale Integration design. This issue can be fathomed with the assistance of adiabatic method that diminishes the dynamic power utilization in the pull up network and the energy stored on the load capacitance can be recycled. A multiplexer is the essential part of the any digital circuit and a standout amongst the most used circuits. An assortment of uses a multiplexer has, where a multiplexer can be actualized for e.g. in Full Adder, Arithmetic Logic Unit (ALU), Digital Compressor and so on. This paper displays the semi adiabatic Modified Positive Feedback Adiabatic Logic (MPFAL) for low power operation through energy recovery procedure. The circuit of positive Feedback adiabatic (PFAL) inverter has been modified. Correlation with static CMOS and PFAL circuits are made to demonstrate the designs. In post-layout simulation, energy saving funds of 27% is accomplished against the Modified PFAL Inverter, NAND, NOR gates and multiplexer circuits. The different change results are analyzed in mentor graphics.***

Keywords: Adiabatic logic, PFAL, MPFAL, MUX, Universal gates

1. Introduction

The power utilization is turning into a very enormous issue in the VLSI design. The explanation for is that as it were restricted power is supplied by the batteries, so the circuitry ought to be designed in a manner that it should consume less power. The large power dissipation requires costly and commotion cooling devices, batteries and power protection circuits[1]. Multiplexer is one of the vital segments in the digital design[2]. It is generally utilized inside information path intensive designs. The lessening of power dissipation of the multiplexer is one of the real issues in low power design. The vast majority of the power sparing procedures included scaling of the power supply, which results, considerable expansion in sub limit spillage current likewise it causes instability in the process variety. In this manner some other strategy is required that should autonomous of voltage scaling. It has been found that there is crucial association between calculation and power dissipation. That is if by one means or another calculation could be executed without any loss of the information, then the energy required by it could be potentially decreased to zero. This can be accomplished by playing out all the calculation in a reversible way. Along these lines least power utilization amid charge transfer phase known as adiabatic switching has been considered from the literary works. Traditional CMOS based designs consume a great deal of energy amid switching process. Adiabatic switching procedure diminishes the energy dissipation through PMOS amid charging process what's more, reuses a portion of the energy which is stored on load capacitor amid the discharging phase[1]. The term adiabatic originates from thermodynamics, used to depict a procedure in which there is no trade of heat with the environment. The adiabatic logic structure significantly lessens the power dissipation. The Adiabatic switching system can accomplish very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.[1][3]

2. Introduction to PFAL

PFAL is new adaibatic technique which uses positive feedback. This logic structure comprise of cross-coupled inverters, with NMOS devices are associated between the outputs and the power-clock[3]. In PFAL, sinusoidal power supply is utilized, known as power clock which is separated into four phases.In evaluate interval , the outputs are evaluated from stable input signal. Amid hold interval, output are kept stable , next is the recover interval, which recover the energy and the latter is wait interval , embedded for the symmetry. PFAL is a dual-rail circuit which acknowledge complementary inputs concerning each other and give outputs complemented each other with halfway energy recovery. The general schematic of the PFAL gate is appeared in Fig. comprise of an adiabatic amplifier, a latch made by the two PMOS and two NMOS , output hubs out and outB with no debasement in logic level . The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and structure a transmission gate. The two n-trees understand the logic functions.

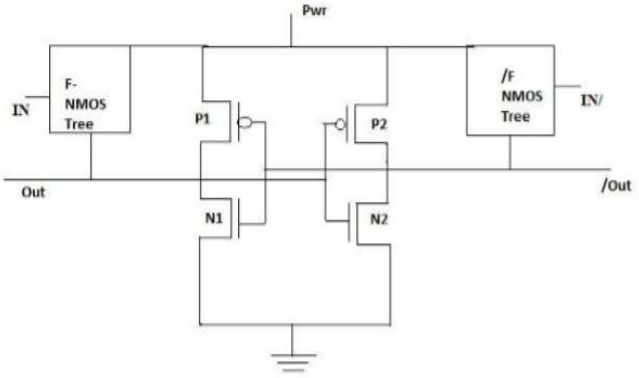

Figure 1: PFAL logic

The Positive adiabatic logic family shows low power dissipation and robustness against the technology parameter variation. The general schematic of the circuit is shown in Fig.. As in figure shows that two latches made by the PMOS P1 & P2 and NMOS N1 & N2. The input logic function that

is to be implemented, realize using the NMOS functional box. The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETS, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The advantage of the PFAL over the ECRL is, PFAL doesn't have the coupling effect and better power efficiency at higher frequency.[4]

3. Modified PFAL

The circuit diagram for modified PFAL adiabatic circuit is shown in Figure2 . It implements basic Inverter functionality. It uses an additional drain gate connected NMOS transistor, in between the source and ground terminal of PFAL cross coupled inverters to reduce the power dissipation more than PFAL inverter design.[5]

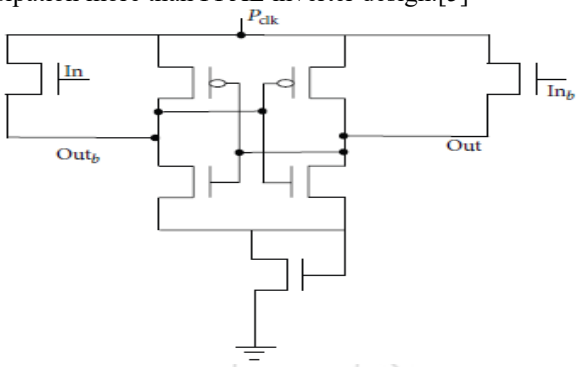

Figure 2: MPFAL Inverter

Modified PFAL NAND Gate

The partially adiabatic PFAL with two-input NAND gate can be implemented as shown below in the Figure3 using standard Mentor graphics technology and simulated waveforms is shown in Figure9 , respectively.

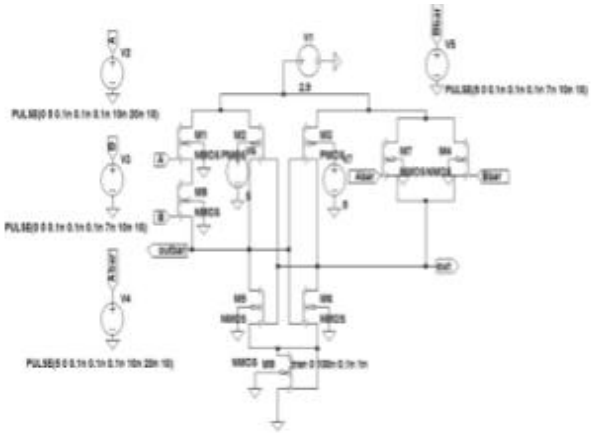

Figure 3: Basic Structure of MPFAL NAND Logic Gate

Modified PFAL NOR Gate

The partially adiabatic PFAL with two-input NOR gate can be implemented as shown below in the Figure4 using standard Mentor graphics technology and simulated waveforms is shown in Figure10 , respectively.

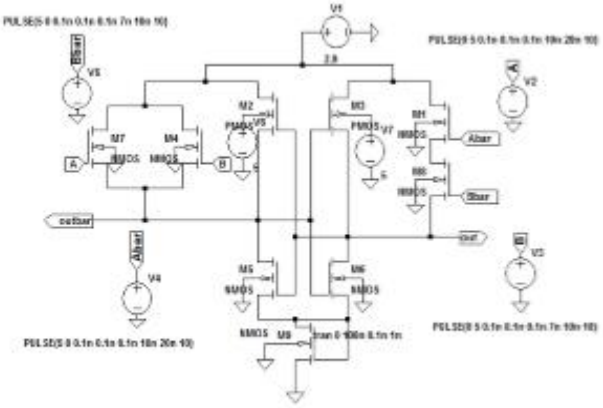

Figure 4: Basic Structure of MPFAL NOR Logic Gate

MULTIPLEXER

Multiplexer is a digital switch. It permits digital information from a few sources to be routed onto a single output line. The essential multiplexer has a few data input lines and a single output line. The selection of a specific input line is controlled by an arrangement of selection lines. Ordinarily, there are 2n input lines and n selection lines whose bit blends figure out which input is chosen. Accordingly, multiplexer is 'many into one' and it gives what might as well be called an analog selector switch. The 8x1 multiplexer has eight inputs and one output. What's more, it has three selection lines. Contingent upon the three selection lines, one output is chosen at once from among the eight input lines.[3]

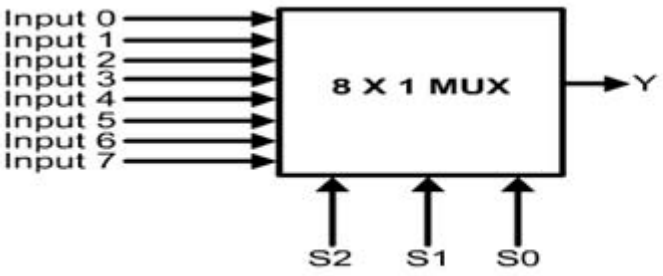

Figure 5: a) 8x1 MUX

Selection lines			Inputs								Output
S2	S1	S0	A	B	C	D	E	F	G	H	
0	0	0	1	0	0	0	0	0	0	0	A
0	0	1	0	1	0	0	0	0	0	0	B
0	1	0	0	0	1	0	0	0	0	0	C
0	1	1	0	0	0	1	0	0	0	0	D
1	0	0	0	0	0	0	1	0	0	0	E
1	0	1	0	0	0	0	0	1	0	0	F
1	1	0	0	0	0	0	0	0	1	0	G
1	1	1	0	0	0	0	0	0	0	1	H

b) Truth Table of 8x1 MUX

4. Simulation Results and Discussion

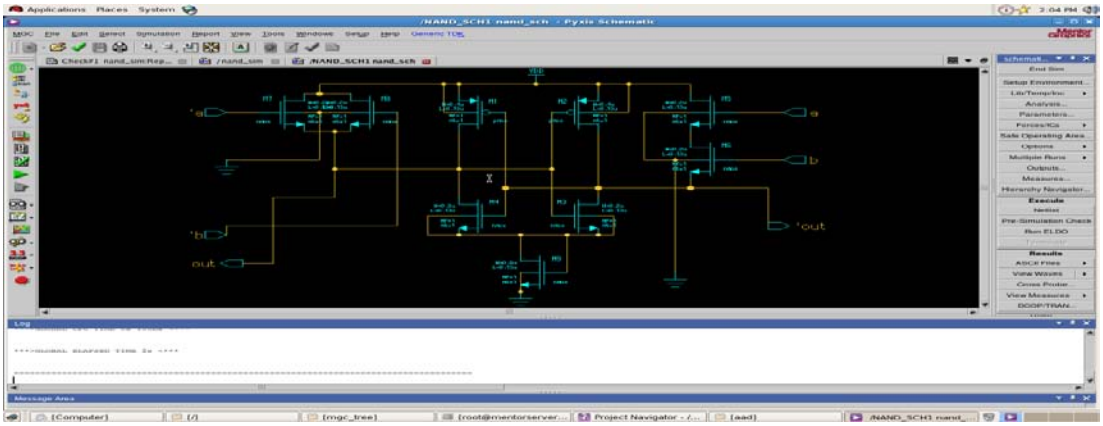

Figure 6: NAND schematic diagram

Above figure shows the schematic diagram of the MPFAL NAND. The inputs are denoted as a,b and output as out because it is having dual rail we can observe out'.

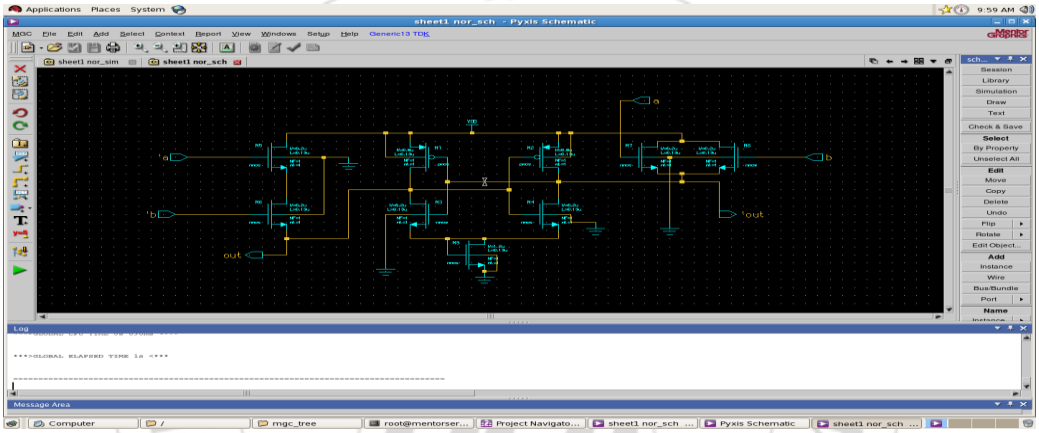

Figure 7: NOR Schematic diagram

Above figure shows the schematic diagram of the MPFAL NOR. The inputs are denoted as a,b and output as out because it is having dual rail we can observe out'.

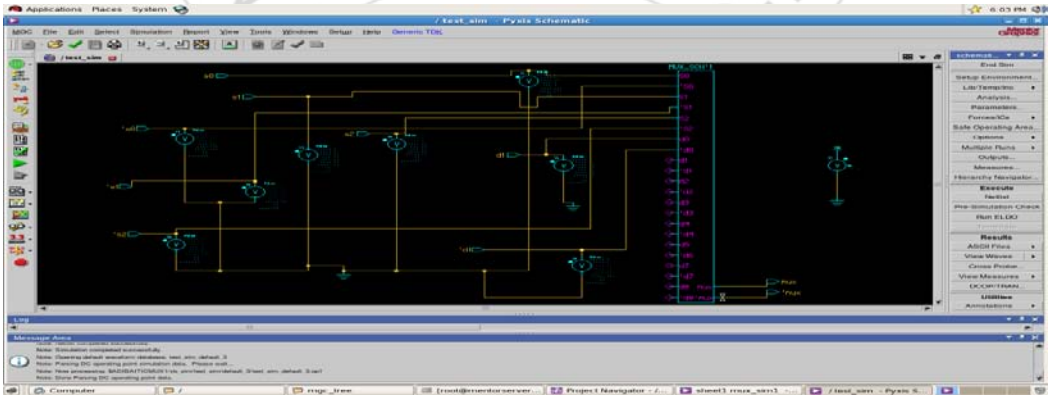

Figure 8: 8x1 MUX Schematic

Above figure shows the schematic diagram of the 8x1 MUX it is having 8 input lines,3 select lines and one output line.

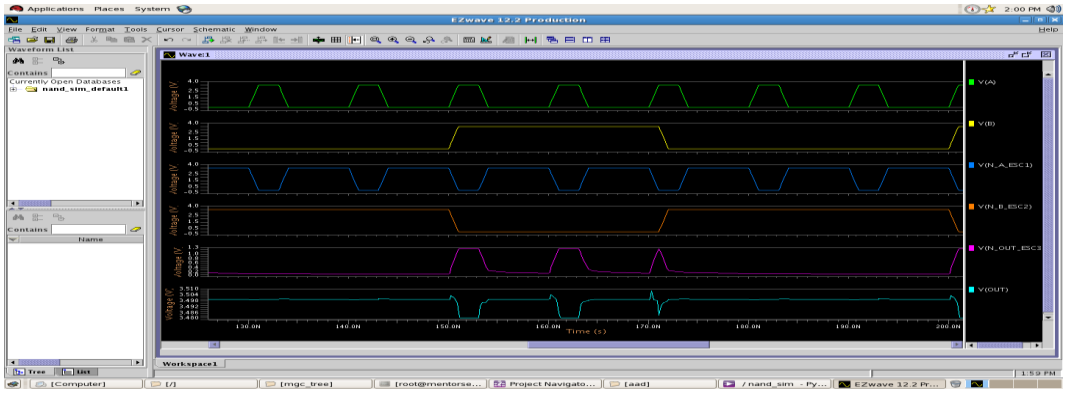

Figure 9: NAND simulation

Above figure shows the simulation of NAND circuit.

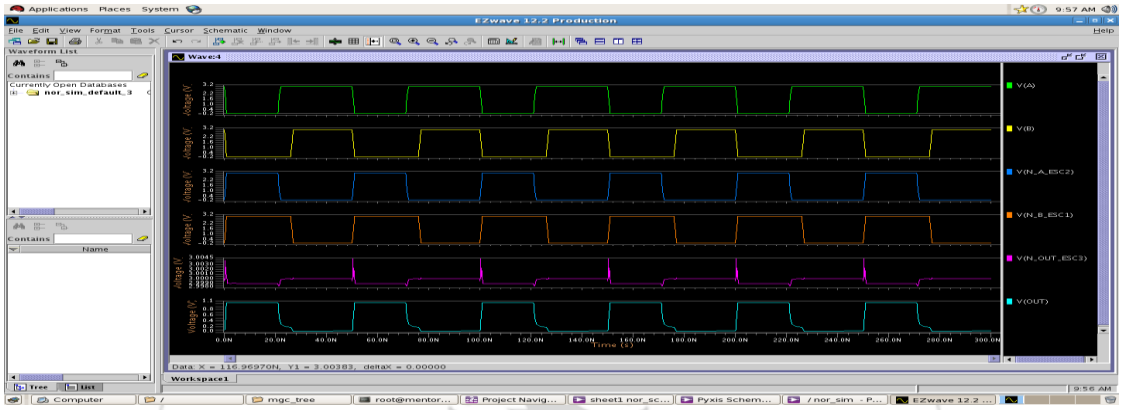

Figure 10: NOR simulation

Above figure shows the simulation of NOR circuit

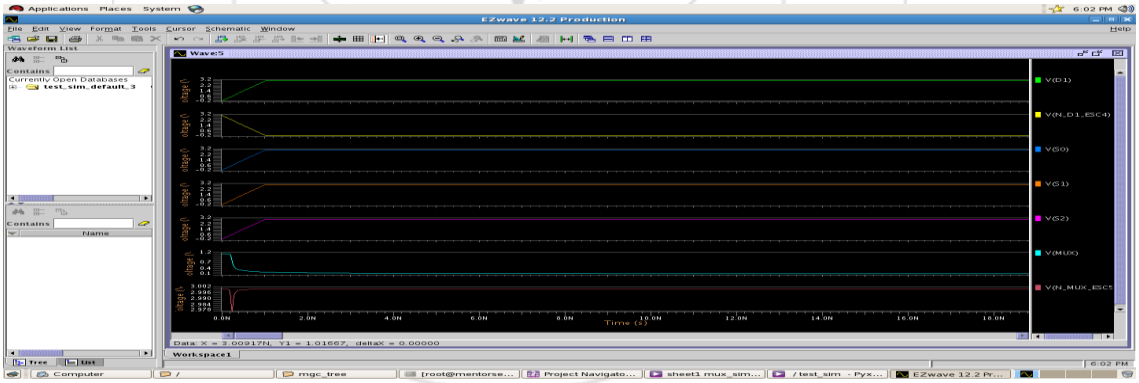

Figure 11: 8x1 MUX simulation

Above figure shows the simulation of MUX with 8 i/p lines

5. Results

This section showed the comparison of the conventional CMOS logic style with the low power adiabatic logic style. Table I, II& III indicate the power comparison made for the proposed inverter, NAND, NOR and MUX gates constructed using PFAL and MPFAL adiabatic structures. The analysis is made for various voltages across a range of 4V to 5V, to validate the design.

Table 1: Power Comparison at Different Voltages

Inverter type	*Power consumption in watts*		
	4v	*4.5v*	*5v*
CMOS Inverter	895.14m	1.074m	1.223m
PFAL Inverter	180.30u	245.52u	324.63u
MPFAL Inverter	7737u	107.31u	132.52u

Table 2: Power Comparison at Different Voltages

Inverter type	*Power consumption in Micro watts*		
	4v	*4.5v*	*5v*
CMOS NAND Gate	225.28	267.17	341.43
PFAL NAND Gate	208.96	260.06	321.19
MPFAL NAND Gate	75.73	102.14	122.52

Table 3: Power Comparison at Different Voltages

Inverter type	Power consumption in Micro watts		
	4v	4.5v	5v
CMOS NOR Gate	158.42	196.14	235.63
PFAL NOR Gate	115.51	160.60	212.84
MPFAL NOR Gate	47.95	80.39	103.24

6. Conclusion

From the simulation results we broke down the power consumption of different circuits appeared in above Table 1, 2, 3. Results cleared up that modified PFAL inverter has preferred execution over the normal PFAL inverter. The modified PFAL inverter has 70% less power dissipation over PFAL inverter. The modified PFAL universal gate (NOR) has 30% less power dissipation over normal PFAL circuits. The investigation demonstrates that designs in light of adiabatic standard gives better execution when thought about than customary CMOS as far as power despite the fact that their transistor include is high a few circuits.

7. Future Scope

Study of modified positive adiabatic logic connected with multiplexers, multipliers and different types of adders in different parameters will be measure. Area efficient layout design analysis of shifter and rotator will be formed using MPFAL logic. Also measure dissipated energy at higher frequencies.

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Author Profile

M. Shyam Sundar is a research Scholor in OPJS university Churu, Rajasthan, his research area is low power vlsi, he has more than ten papers in international journals and two international conference papers.