International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2015): 6.391

Multifunctional DVR With Seven Level Inverter Scheme Using Voltage and Current Control

Dony John[1], Surumi Hassainar[2]

[1]PG Student [PEPS], Department of EEE, FISAT Engineering College, Angamaly, Kerala, India

[2]Assistant Professor, Department of EEE, FISAT Engineering College, Angamaly, Kerala, India

Abstract: ***Voltage sag is a very crucial issue faced by the modern electrical industry which has resulted in increased attention..Voltage sag is defined as a decrease in voltage from 0.1 to 0.9 per unit (pu) in rms voltage at the power frequency for durations from 0.5 cycle to 1 min. It is mainly due to the energization of heavy loads or starting of large induction motors changeover of large loads etc. Other major issue that our utility mainly deals is short circuit faults like single phase to ground, two phase to ground or three phase faults. It cause to flow a large current through the unfaulted phase and decrease in voltage in the affected phase. So inorder to eliminate those two problems we use multifunctional DVR. It is a power electronic converter based custom power device used to compensate for voltage variations and to limit the fault current. This study proposes a new scheme for multifunctional DVR based on a seven level multilevel inverter and a different control scheme. This results in better quality of output voltage in voltage sags. It is important to emphasis that the existing inverter-based DVR topologies do not have the capability of third harmonic elimination, Consistency in DC link voltage, Better output for inverter section, efficient modulation scheme incorporation etc. The system model is carried out in MATLAB/SIMULINK environment. With the aids of the proportional-integral controllers, dq0-abc transformation Level shifted pulse-width modulation control technique, the inverter control system is managed.***

Keywords: Dynamic voltage Restorer, Fault current limiter, Multilevel Inverter

1. Introduction

There are two major challenges that the modern power system mainly deals with, voltage fluctuations and short circuit faults. With wide usage of nonlinear loads voltage unbalance and other power quality problems are arise. At the same time, many power loads become more sensitive to these disturbances. The rapid growth of renewable power generation sources in the grid has more prone to these power quality problems. With the rapid development of modern electrical power industry and the great changes of electrical load in system, more users use the new equipments with good performance and high efficiency, but these equipments are sensitive to the changes of system voltage. Voltage sag is such a crucial problem that the modern power system mainly deals with which introduce enormous loss in the system. The dynamic voltage restorer (DVR) which has appeared in recent years is another important member of the flexible ac transmission systems (FACTS).furthermore, short-circuit faults remain one of the most common faults in the grid and causes great concern for grid security and stability. In order to avoid the such instability and to avoid voltage issues multifunctional DVR is introduced. Here we are proposing a multifunctional DVR which using voltage and current in stationary frame to achieve the best result.abc to dq0 transition yields better output at the output side of rectifier unit, and the introduction of multilevel inverter scheme minimizes the THD of the output voltage which is injecting into the grid.

2. Proposed FCL-DVR Concept

It would be tremendously advantageous to provide both voltage compensation and fault current limiting functions by a single power electronic apparatus. Fault current interrupting feature is incorporating with the control strategy of a conventional DVR voltage compensation function. Due to the increased system cost and high power rating those are not that economical now days. So here a new concept of fault current limiting dynamic voltage restorer (FCL-DVR) with a new control scheme is proposed. As the conventional FCL-DVR it also has the two modes of operation.

- Compensation mode for voltage fluctuation and unbalance
- Fault current limiting mode.

The block diagram representation of the system is as shown below. 11kv source is feeding a load of 1MW through the series transformer which is used as compensation transformer or injection transformer. Input of the series injection transformer is feeding through a back to back converter topology. Supply to the rectifier is feeding through a delta connected shunt transformer inorder to eliminate the 3rd order harmonics. Output of the rectifier is stored across a capacitor. Then it is feeding a inverter. For the clean and minimized THD output seven level inverter is used. It has low THD and gives output very similar to the sine wave. Bidirectional switches are connected at each output terminals in every phase which are turned on and off depending on the requirement.

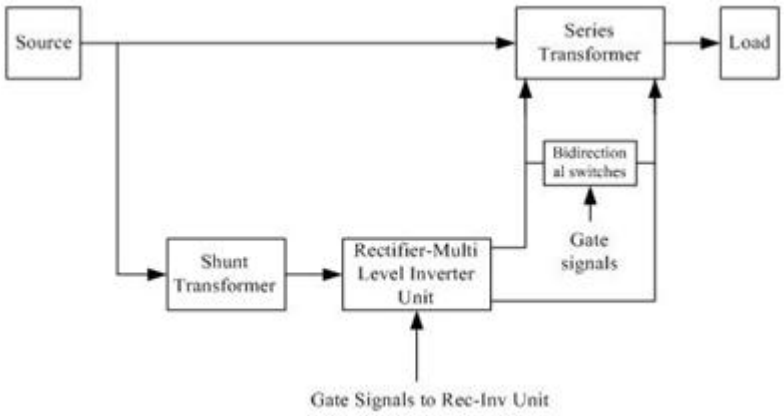


Figure 1: Block Diagram representation of system model

3. Voltage Compensation and Fault Current Limiting Mode

FCL-DVR has three main switching strategy as the conventional mode. But the generation of the control pulses are different and it uses stationary frame parameters. Three modes are

1) Grid is in Normal mode (No compensation required)
2) PCC voltage unbalance is their but no fault – FCL DVR operates in voltage compensation mode and the bidirectional switch is not activated.
3) Any fault occur – The healthy phase of FCL-DVR operate in voltage compensation mode and bidirectional switches corresponding to the faulted phase is activated. Thus the fault current is limited through the faulted path. Then it will return to the voltage compensation mode after the fault condition is removed.

4. Circuit Diagram Representation

The circuit diagram representation of the FCL-DVR is as shown in figure(2). It is composed of three single phase bridges. Each single phase topology mainly comprises of a shunt transformer, a back to back power converter, a series transformer, and a bidirectional switch. The input rectifier module of the back to back converter is connected to the grid through a shunt transformer with Lz to eliminate the high frequency ripples, and rectifies the power from the grid to the dc link capacitor. The output inverter module converts the power from the dc link capacitor to compensate voltage fluctuation, and is connected to the grid through a series transformer T4 and a LC output filter. The input rectifier module and output inverter module are connected through the dc link capacitor Cd. The bidirectional switch in each phase is across the output terminals of the output inverter module to provide short circuit fault current limiting function.

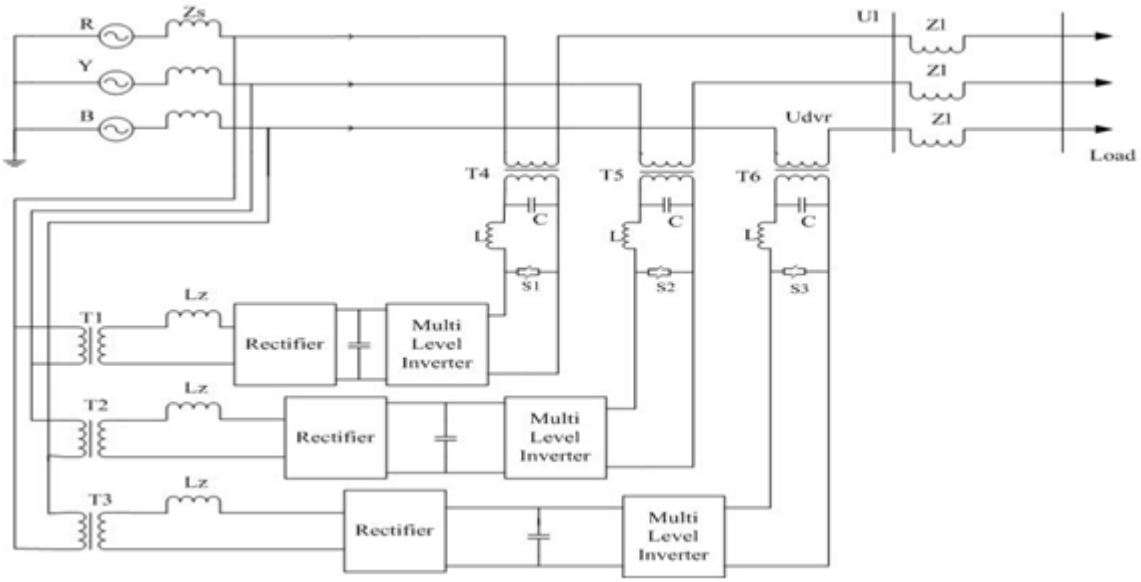
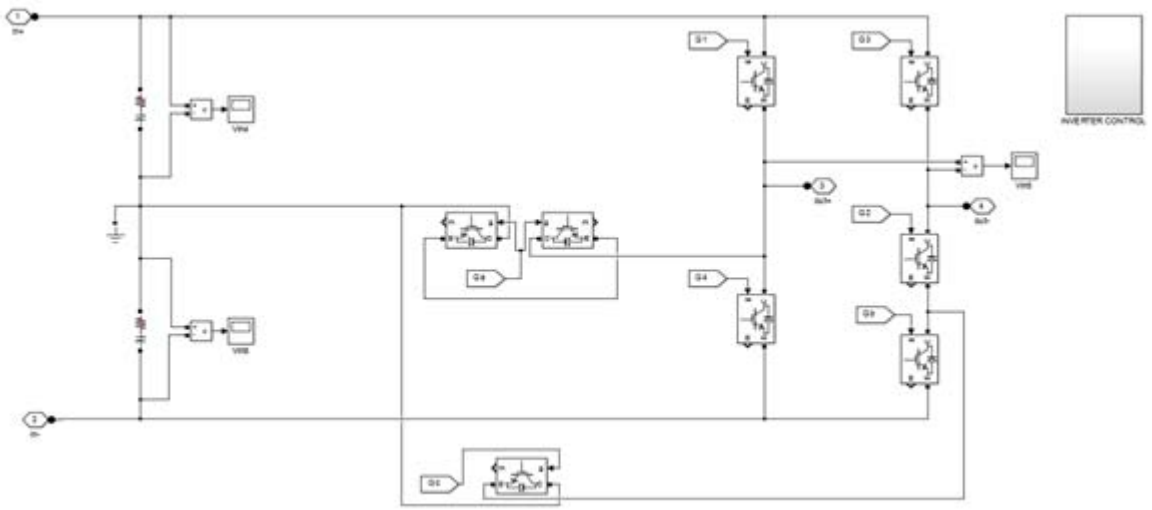


Figure 2: FCL-DVR system model.

5. Multilevel Scheme

Multilevel inverter scheme that going to implement is as shown below. The seven level inverter topology require less number of components compared to other well known symmetrical topologies like neutral point clamped, flying capacitor and cascaded H-bridge topology.

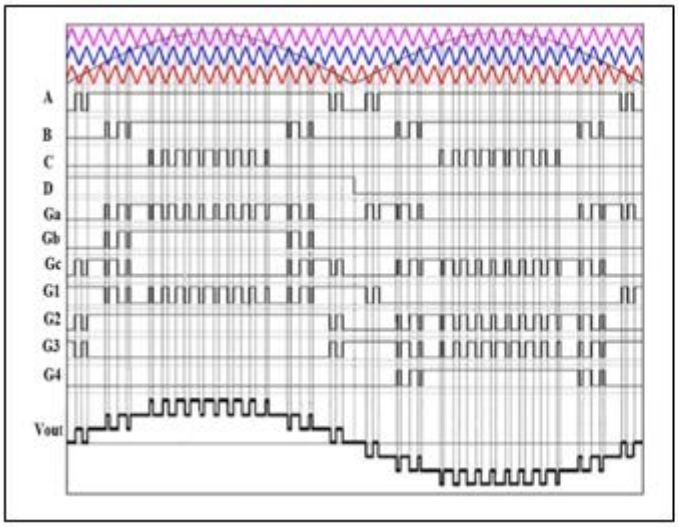


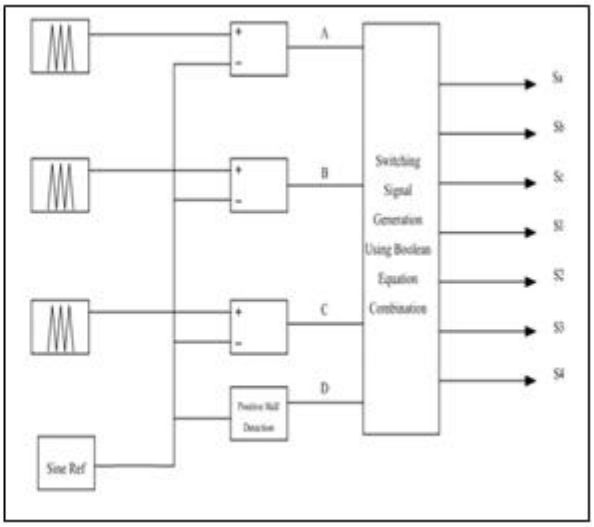
Multilevel inverter scheme used has only eight numbers of switches which is lesser compared to conventional H-bridge systems. So switching losses can be minimized. Proper switching will produce voltage levels of 0, E, 2E, 3E, -E, -2E and -3E at the inverter output. Switching pattern for the multilevel inveter is as below.

Output Voltage	S1	S2	S3	S4	Sa	Sb	Sc
E	1	1	0	0	0	0	1
2E	0	1	0	0	1	1	0
3E	1	1	0	0	0	1	0
0	1	0	1	0	0	0	0
-E	0	0	1	0	1	0	0
-2E	0	1	0	1	0	0	1
-3E	0	0	1	1	0	0	0

6. Modulation Scheme

PWM modulation techniques like staircase modulation technique alternate phase opposition disposition modulation technique, level shifted or phase shifted can be used for the generation of the control pulse generation for the inverter. Sine reference wave for the modulation is obtained using voltage and current control method which uses the load voltage sensor and current sensor. By the proper conversion in to stationary frame we are obtaining the quadrature axis and stationary axis actual and reference parameters. Using this we obtain the reference signal for the modulation. same will be repeated in each phases. Then using the proper combination of the A,B,C,D gate pulses to the each switches of multilevel inverter.

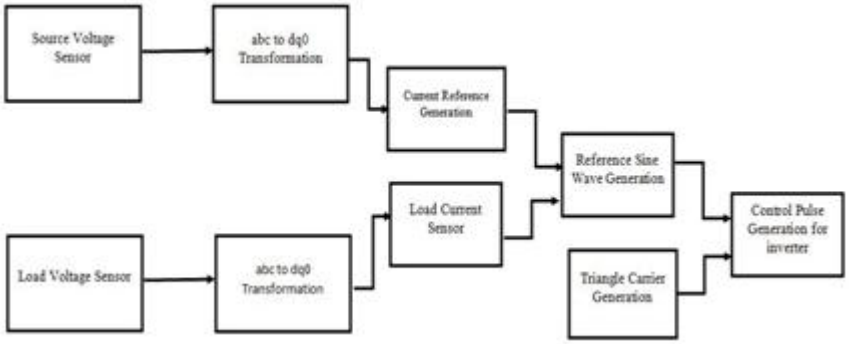




7. Principle of Operation

When system is working in voltage compensation mode the bidirectional switches across each output phase of the inverter will be deactivated. The FCL-DVR operates as a conventional DVR by injecting required voltage to the grid. Control pulses to the rectifier are generated by comparing 800V with the actual dc link voltage then to passing through the proportional integral controller error is compensated. Which is then compared with the PLL and passing through the PI Controller we obtaining the reference sine wave for the modulation. Sine wave reference is compared with the triangular wave gate pulses to the rectifier module is generated.

The stationery reference voltage in dq0 frame is used to generate the current references. Using the obtained current, voltage quadrature and direct axis components control pulses to the inverter are obtained. When system is working in fault current limiting mode the bidirectional switches across faulted phase of the inverter will be activated. Thus path will be shorted and limit the large fault current. Comparison of lower, middle and upper carrier with rectified sinusoidal signal will generate signals A, B and C respectively. Signal D is generated by the detection of zero crossing of fundamental frequency signal. PWM gate signals are generated by combinational logic circuit using signals A, B, C and D. using the better combinations of Logical relations we can generate switching signals for the seven level inverter.



8. System Design Parameters

System design is simpler compared to any other design considerations. Here the matlab parameters are obtained as follows as in ref [2]. So the obtained parameter for matlab simulation model is listed as below.

No	Design Parameter	value
1	Grid supply voltage	11kV
2	Load	1MW
3	Grid frequency	50Hz
4	DC Link voltage/V	800V
5	Compensation capacity/kVA (Injection transformaer rating)	132kVA
6	Shunt transformer ratio	23.5:1
7	Leakage Inductance	2mH
8	DC Link capacitance	1500μF
9	Filter capacitance and inductances	100μF-100H

9. Simulation Results and Analysis

MatLab simulation is carried out to verify the validity of the topology and design methodology. The supply voltage is set at 11 kV with a 1MW resistive load. The FCL-DVR is designed to compensate a voltage fluctuation of 20% of the supply voltage. The maximum fault current is allowed to be six times of the nominal load current. For introducing a sag in the system an inductive load is added in time duration 0.4-0.5Sec. The output voltage waveform before and after FCL-DVR is introducing is as below (fig:10,11)

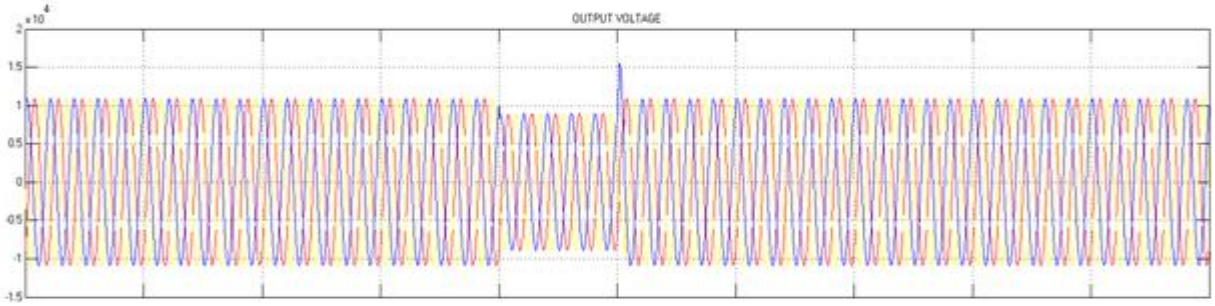


Figure 10: System sag without FCL-DVR

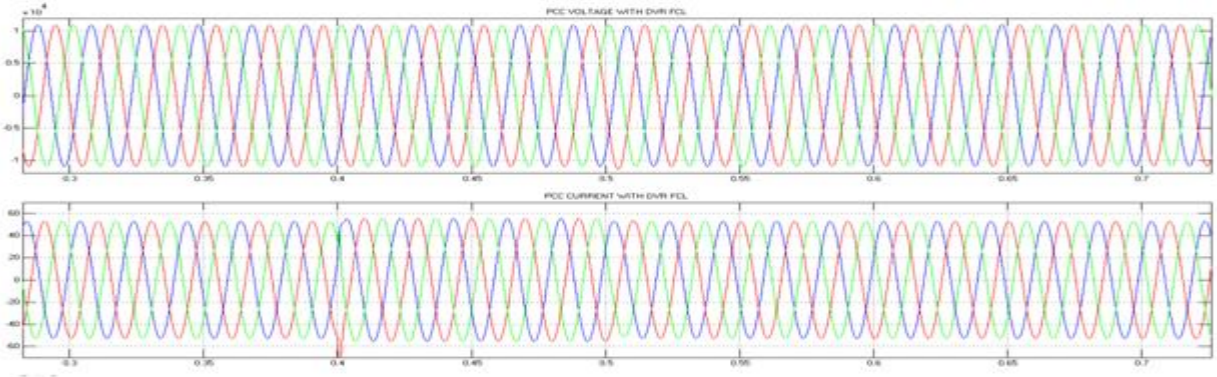


Figure 11: System sag compensation with FCL-DVR

In order to show the fault current limiting function and recovery process, simulations of FCL-DVR for single-phase to ground fault and short-circuit faults are carried out. Simulation results for single phase to ground fault (phase A), phase-to-phase short circuit fault (phases A and B), two-phase to ground fault (phases A and B), and three-phase to ground fault are shown below. Fault is added between the time duration 0.4-0.5sec itself. DC Link voltage is shown to be constant around 800V. Fig(12)

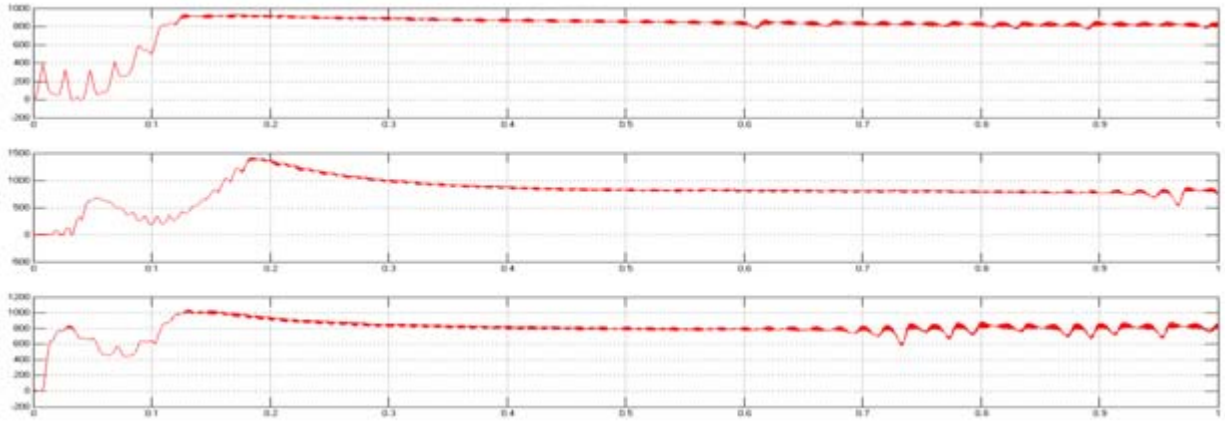


Figure 12: DC Link stabilization achieved during FCL-DVR fuctioning

A. LLG Fault

A double phase to ground fault is introduced at phase A and B between 0.4 to 0.5 sec. Voltage at the faulted phase goes to Zero at the time of fault and current through the corresponding phase increased drastically. Output waveforms of voltage and current before and after the fault current limiting function is as shown below.

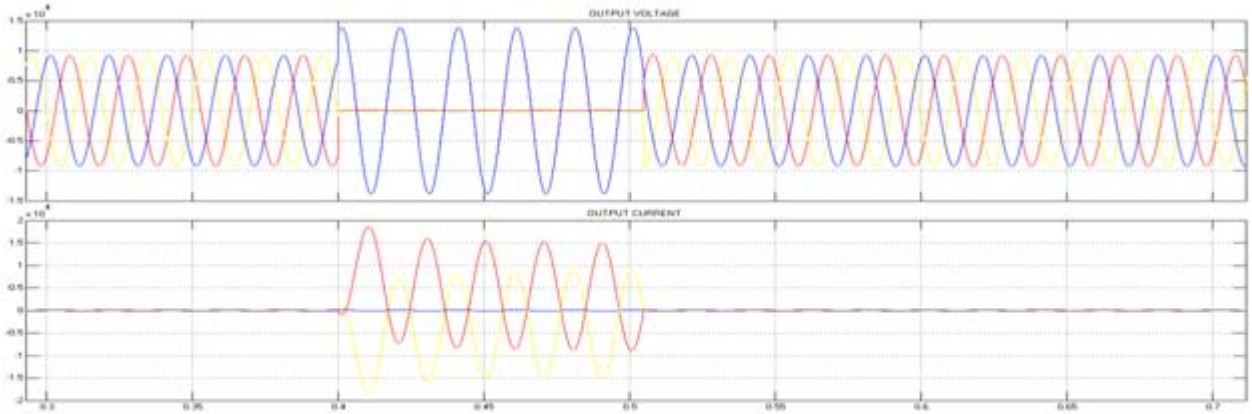


Figure 13: Single line to ground fault output waveform without FCL-DVR

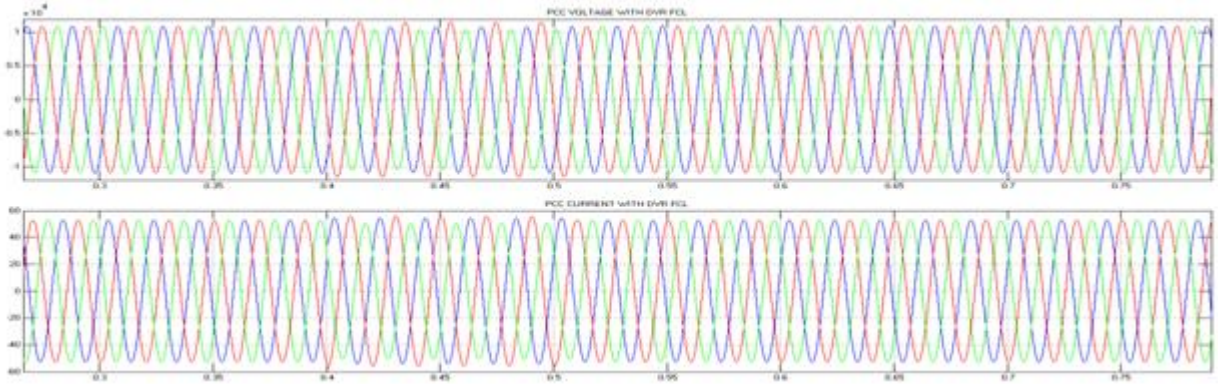
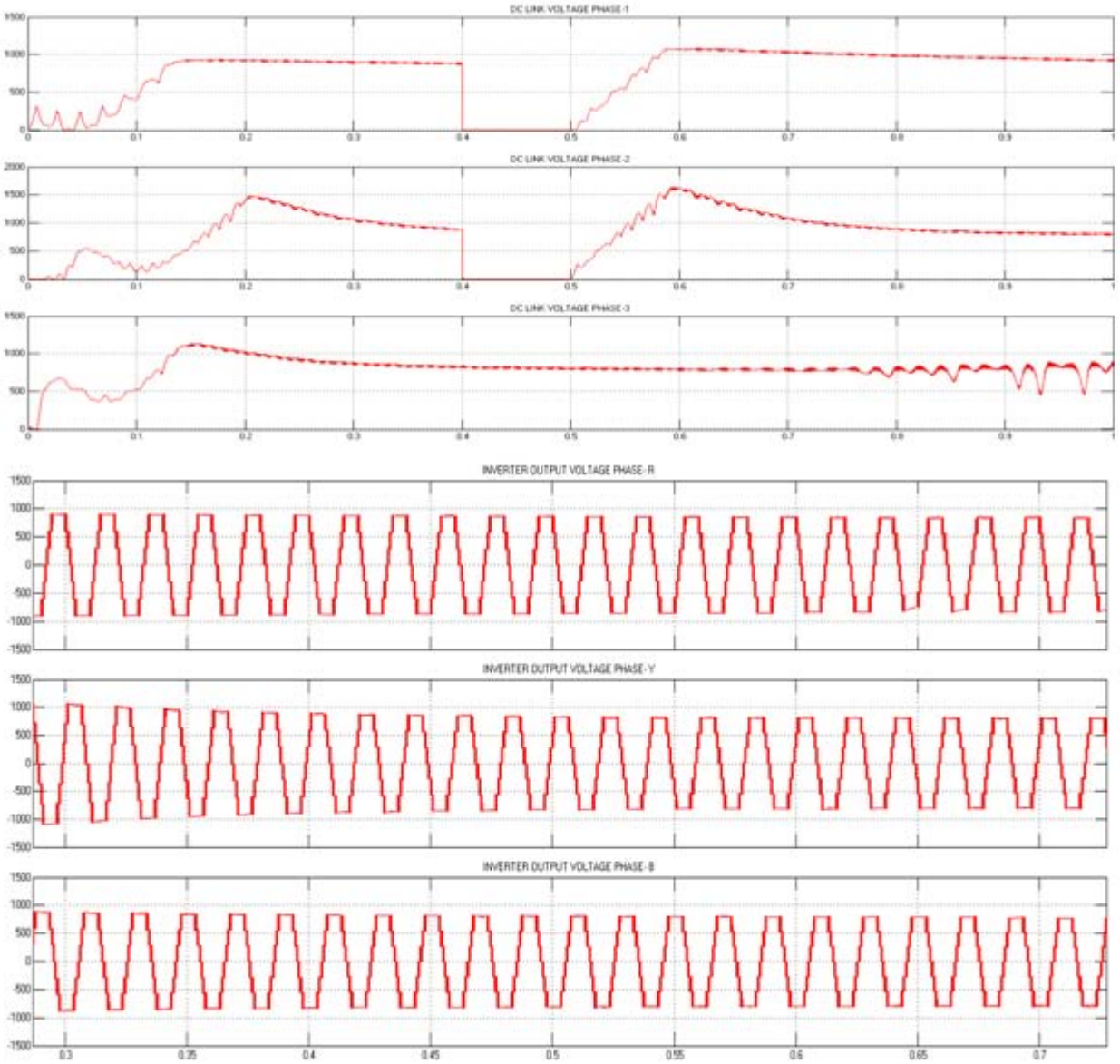


Figure 14: Single line to ground fault output waveform with FCL-DVR

Fault current is limited to a safe value and the DC Link stabilization is achieved to around 800V. For the duration 0.4-0.5 sec where the fault is introduced DC link voltage fall to zero. Beacuse the switches corresponding to the faulted phase are turned on thus the path become shorted. Seven Level Multilevel outputs are also given below.



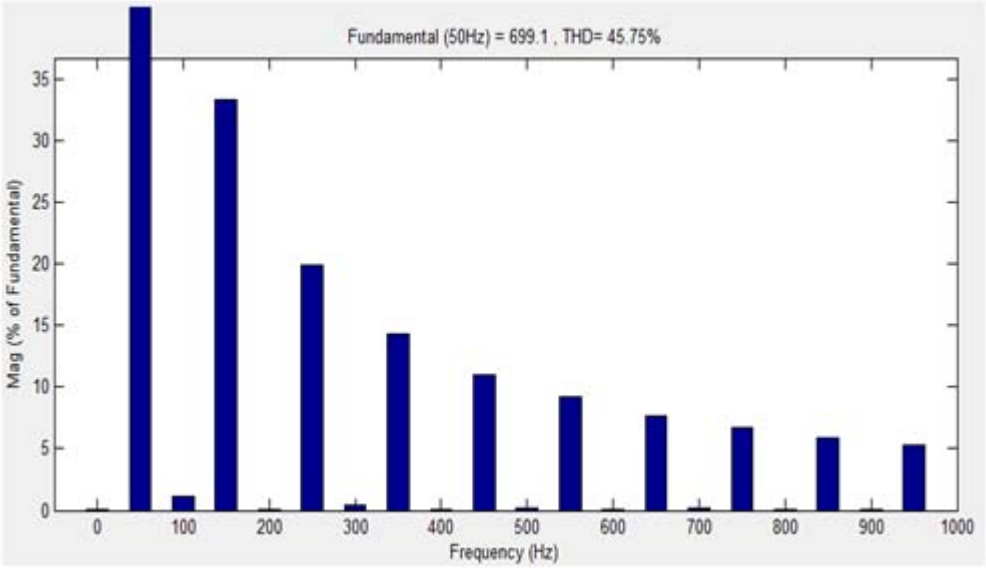
B. LLG & LLLG Fault

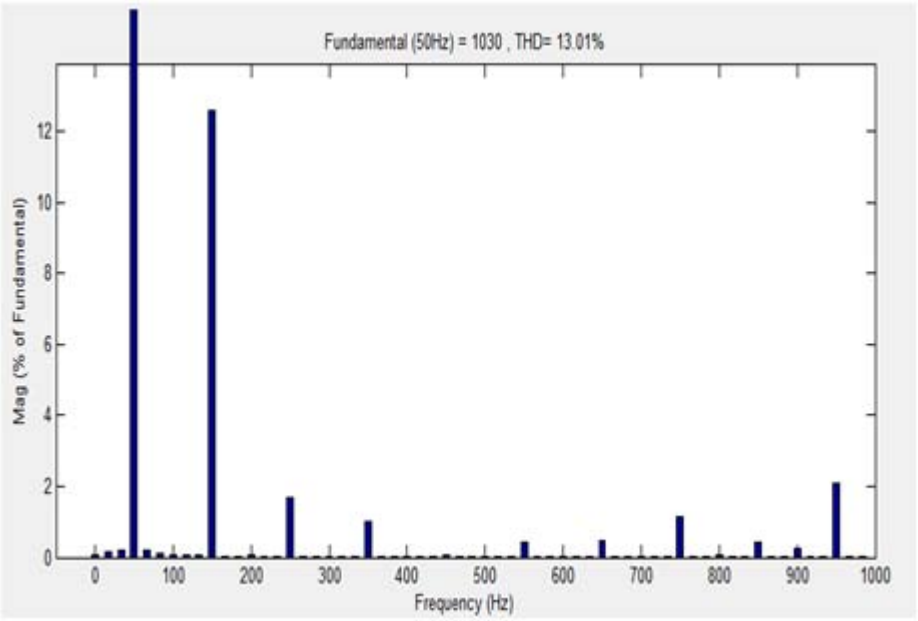
The same model is extended to A double phase to ground fault/three phase fault between 0.4 to 0.5 sec. Voltage at the faulted phases goes to Zero at the time of fault and current through the corresponding phase increased drastically. Output waveforms of voltage and current before and after the fault current limiting function are obtained. In all the system responses is better and DC link voltage stabilization is achieved. It can be summarized as follows. * shows the DC link voltage is not stabilized. It goes increasing as the time moves.

No	Simulation Results chart				
	Type Of Fault/Sag	*DC Link voltage with old control scheme (Rphase)*	*DC Link voltage with proposed control scheme and multilevel inverter (Rphase)*	*THD with old control scheme (Rphase)*	*THD with multilevel inverter scheme (Rphase)*
1	Voltage Sag	950V*	820V	45.75%	13.01%
2	LG fault	900V*	820V	45.75%	13.01%
3	LLG fault	750V*	820V	45.75%	13.01%
4	LLG fault	750V*	800V	45.75%	13.01%

B. THD Results

With new control scheme THD is minimized and better output waveforms are obtained. For all the three phases the values shows the proposed method is far better than the existing control methods. Waveforms obtained before and after the new control scheme for a single phase (R) with voltage sag elimination model is obtained as below.





10. Conclusion

With the proposed control scheme with new multilevel topology THD is minimised and DC Link stabilization is achieved. Based on theoretical analysis and MatLab simulation and experimental study, conclude the following:

- It uses only the load current sensor and voltage sensor which is more simple to install and economical.
- DC Link voltage stabilization is achieved and limited to around 800V for long duration. As the time moves it becomes more stable with out having any disturbances.
- With the new control scheme THD is minimized much obtained the better sine references for the modulation.
- LS-PWM technique yield better output.
- Seven level inverter topology reduces the switching stresses and decrease the number of switches.

Minimization and comparison of THD with different modulation scheme and more multilevel inverter topology can be achieved in future

11. Acknowledgment

As I complete this work, I realize and recognize numerous hands who helped me in numerous ways, and thank them all with my whole heart. I am highly indebted to, Ms. Surumi Hassainar Assistant Professor, Department of Electrical Engineering, for piloting the project through trials and tribulations. I remember our teachers of the Department of Electrical Engineering, who were always a support in our academics.

References

[1] N. H. Woodley, L. Morgan, and A. Sundaram, “Experience with an inverter-based dynamic voltage restorer," IEEE Trans. Power Del, vol. 14, no.3, pp. 11811186, Jul. 1999.

[2] Zhikang Shuai, “Design Considerations of a Fault Current Limiting Dynamic Voltage Restorer (FCL-DVR)," IEEE Transactions On Smart Grid Vol. 6,No. 1, January 2015..

[3] Ali Ajami, “A New Concept of Multilevel DVR Based on Mixed Multi cell Cascaded Topology ,"201O International Conference on Mechanical and Electrical Technology (ICMET 2010).
[4] Mohammad Farhadi Kangarlu, “Dynamic voltage restorer based on multilevel inverterwith adjustable dc-link voltage ",University of Tabriz, 51664 Tabriz, Iran
[5] Vivek P.V, “Multistring Seven-Level Inverter for Standalone Photovoltaic Systems”,IEEE Conference publication.
[6] Changhee Cho,“Active Synchronizing Control of a Microgrid,"IEEETRANSACTIONS ON POWER ELECTRONICS,Vol. 26, No. 12, December 2011
[7] A. Ghosh and G. Ledwich, “Compensation of distribution system voltage using dvr,” IEEE Transactions on Power Delivery, vol. 17, no. 4, pp. 1030–1036, Oct. 2002.1
[8] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, Dynamic voltage restoration with minimum energy injection,"IEEE Trans. Power Syst, vol. 15, no. 1, pp.51?57, Feb. 2000.
[9] S. S. Choi, Member, IEEE, T. X. Wang, and D. Mahinda Vilathgamuwa,Senior Member, IEEE A Series Compensator With Fault Current Limiting Function,"IEEE Transactions On Power Delivery, Vol. 20, No. 3, July 2005
[10] Muralekrishnen.R, Mr.Sivakumar.P., Improving the Power Quality Performance of the Power Quality Performance for Distributed Power Generation ,"2012 International Conference on Computing, Electronics and Electrical Technologies [ICCEET]
[11] Firouz Badrkhani Ajaei,StudentMember,IEEE, Shahrokh Farhangi, and Reza Iravani, Fellow IEEE,Fault Current Interruption by the Dynamic Voltage Restorer,"IEEE Transactions On Power Delivery, Vol. 28, No. 2,April 2013
[12] S.S. Choi, A Series Compensator With Fault Current Limiting Function,"IEEE T. X. Wang, and D. Mahinda Vilathgamuwa, Senior Member,IEEETrans actions On Power Delivery, Vol. 20, No. 3, July 2005
[13] N. H. Woodley, L. Morgan, and A. Sundaram, Experience with an inverter-based dynamic voltage restorer,"IEEE Trans. Power Del, vol. 14, no.3, pp. 1181?1186, Jul. 1999.