

Comparative Analysis of D Flip-Flops in Terms of Propagation Delay

Anu Samanta¹, Madhu Sudan Das²

^{1,2}NSHM Knowledge Campus Durgapur

Abstract: In this paper implementations of the flip-flops are presented which are positive edge triggered using 250 nm CMOS technology. The gate sizes are optimized precisely for low propagation delay without affecting the basic operation of flip-flops with a supply voltage of 5V. There are three important factors in CMOS: i.e. the gate size area, power dissipation and speed of operation which always compromise between them when it is implemented in the field of IC circuit design. This paper proposes high speed design of D Flip-Flops in compared to the existing D flip-flops in terms of its area, aspect ratio, transistor count and propagation delay with the schematic and simulation results in Tanner tool version 16.

Keywords: CMOS, D Flip-Flops, Propagation Delay, Transistor count, W/L ratio

1. Introduction

Flip-flops or the data storage elements are almost an essential component of every sequential circuitry. Among various flip-flops, D flip-flop is commonly used. It captures the value of the D input at a particular predefined portion of the clock pulse (rising or falling edge of the clock) and its output is not affected at other parts of the clock. From the timing perspective, delay produced by flip-flops consumes a large part of the cycle time while the operating frequency increases[8]. There are different techniques for minimizing the propagation delay based on circuit level[10], architecture[4], layout, and process technology[5]. This is an effective approach where flip-flop with less number of transistors[3] for low propagation delay[7] is designed. In this method we used less number of transistors hence it requires less area[11] and therefore consumes lesser power as compared to conventional flip flop having more transistors.

Numerous D flip-flop topologies [6] are available in the literature. Therefore, it becomes very difficult for a circuit designer to choose appropriate one for his design from all those available topologies to meet the given requirement. In the present scenario there is an ever increasing demand for fast[8] and robust[2] devices. So, appropriate selection of

elements at the very basic level, i.e., flip-flops is important to obtain the desired characteristics to benefit the bigger system. Keeping these facts in mind this paper provides the following contributions: 1) It takes seven different D flip-flop circuits and observes their corresponding outputs. 2) Then the outputs are analyzed[1] to check which circuit provides the least propagation delay. 3) Finally, it concludes with the best D flip-flop circuit in terms of propagation delay. Remaining paper is arranged as follows. Section II discusses all the seven D flip-flops used for comparison. Section III provides the simulation results (delay and transistor count) of all the circuits shown in section II. Section IV ends up with the conclusion.

2. D FLIP-FLOP Topologies

This section briefly describes various D flip-flop topologies considered for analysis in this work.

2.1 Conventional D Flip-Flop from JK Flip-Flop

[9] (implementation using 22 transistors in CMOS technology)

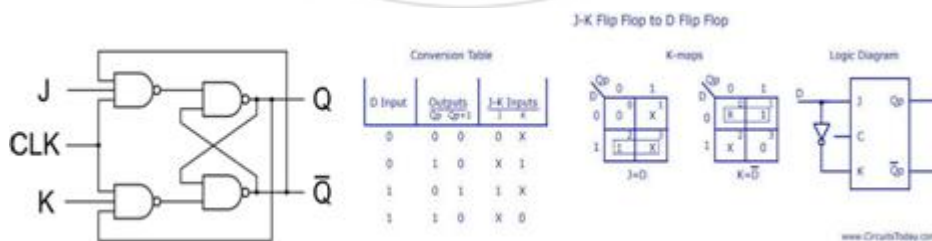


Figure 1: Block Diagram of D Flip-Flop using JK Flip-Flop

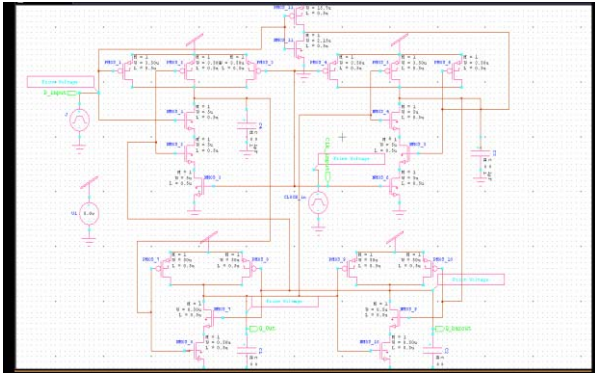


Figure 2: Conventional transistor level implementation of D Flip-flop using 22transistors from Figure 1

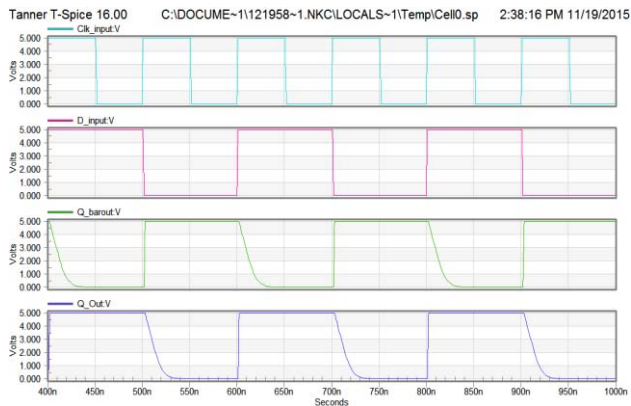


Figure 3: Transient response or output voltage waveform of D Flip-flop of 22 transistors

2.2. D Flip-flop using 12 transistors

Here D_{in} is applied to the power of N_MOS 3 and clock is applied to its gate terminal. When D_{in} and clock is made high, we get logic high from its drain terminal as output. Since the output of N_MOS 3 is fed as one of the input of 2 input NOR gate, the output of N_MOS 3 is high and it turns N_MOS 1 of two input NOR gate ON and hence, we get the output as logic zero which is nothing but Q (bar). At the same time the output of N_MOS 3 is also fed as one of the input for another two input NOR gate followed by an inverter which gives the inverted form of output of N_MOS 3 that is logic zero. As soon as we get logic zero from inverter, P_MOS 8 of two input NOR gate turns ON and we get Q (bar) as logic zero so P_MOS 7 is also ON and hence we get the output as logic high from two input NOR gate i.e., Q.

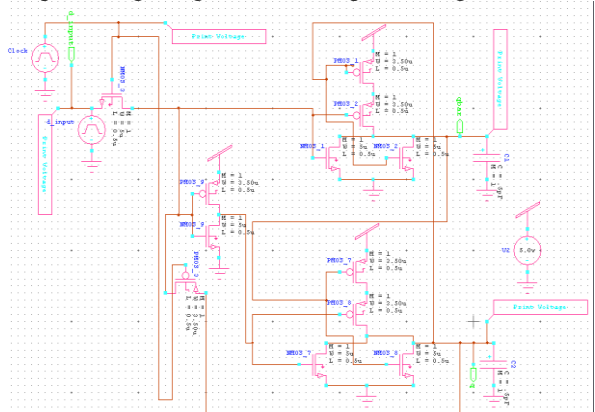


Figure 4: Schematic diagram of transistor level implementation of D Flip-flop using 12transistors

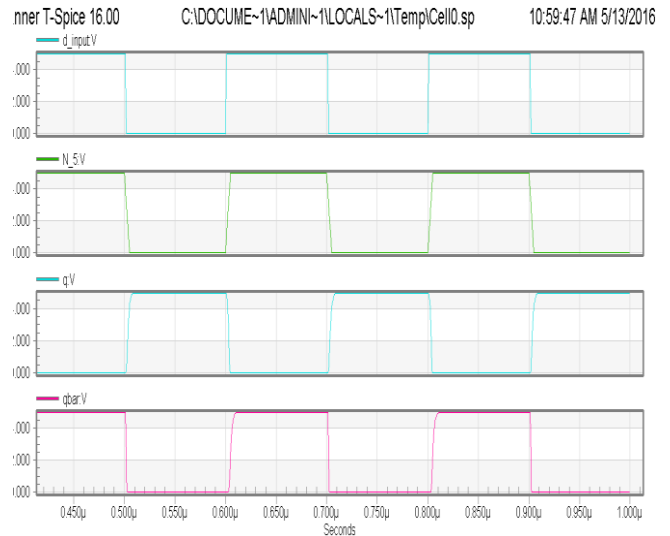


Figure 5: output voltage waveform of D Flip-flop of 12 transistors

2.3 D Flip-flop using 10 transistors

The circuit contains two tri-state inverters, driven by the clock signal and its inverse. The first tri-state inverter acts as the input switch, accepting the input signals when the clock is high. At this time, the second tri-state inverter is at its high impedance state, and the output Q is following the input signal. When the clock goes low, the input buffer becomes inactive, and the second tri-state inverter completes the two inverter loop, which preserves its state until the next clock pulse.

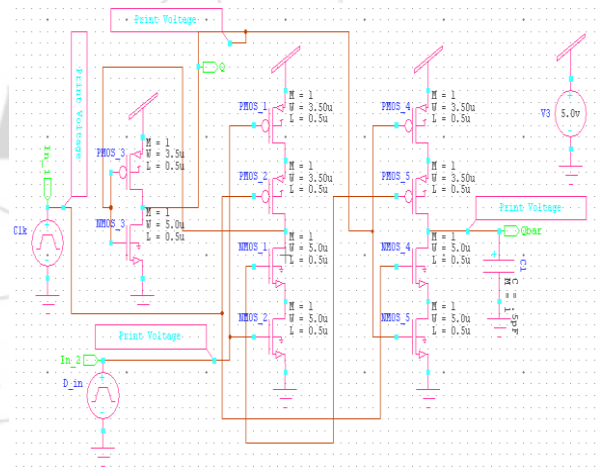


Figure 6: Schematic diagram of transistor level implementation of D Flip-flop using 10transistors

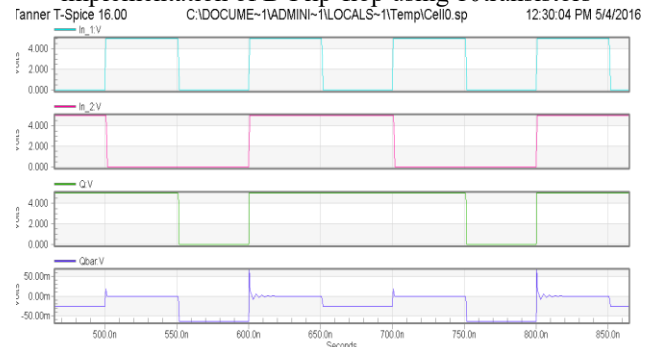


Figure 7: output voltage waveform of D Flip-flop of 10 transistors

2.4. D Flip-flop using 6 transistors

The source of N_MOS 1 is provided with Din whereas the gate of the transistor is provided with an input clock. As soon the clock is set at high, N_MOS tends to pass the input from the source to drain. The inverter circuit with P_MOS 2 and N_MOS 1 inverts Din providing us the value of Q (bar). The inverter circuit 2 with P_MOS 2 and N_MOS 3 on the other hand provides us the value of Q.

P_MOS 3 works as a holding circuit. As soon as the value of clock changes from high to low, P_MOS 3 turns on passing the value of Q to the input of first inverting circuit, thus holding the value of Q and waiting for the clock to turn high.

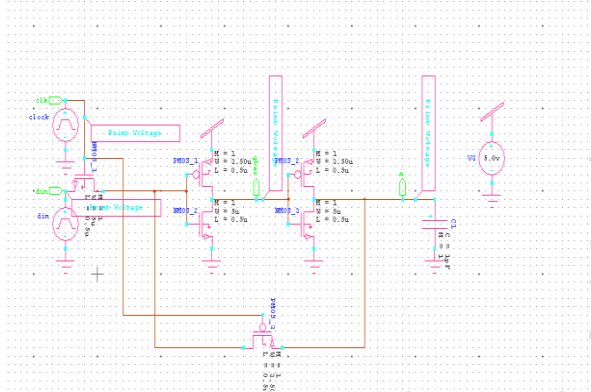


Figure 8: Schematic diagram of transistor level implementation of D Flip-flop using 6 transistors

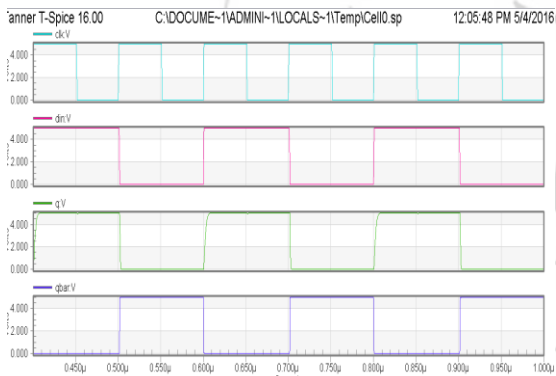


Figure 9: output voltage waveform of D Flip-flop of 6 transistors

2.5. D Flip-flop using 5 transistors

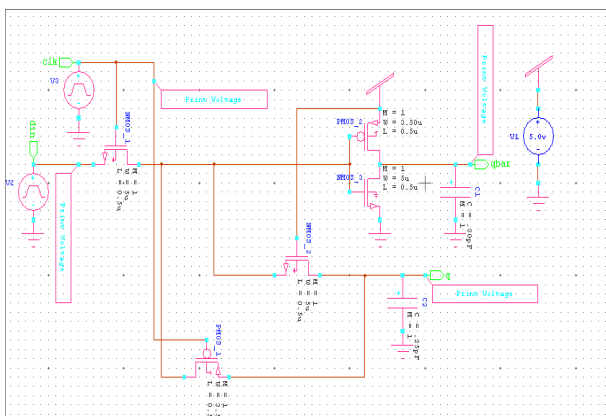


Figure 10: Schematic diagram of transistor level implementation of D Flip-flop using 5 transistors

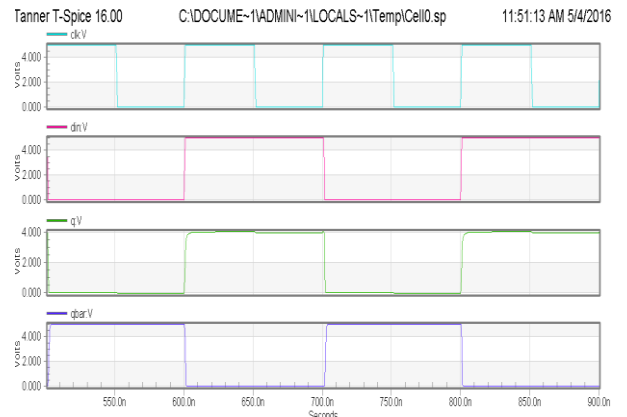


Figure 11: output voltage waveform of D Flip-flop of 5 transistors

2.6. D flip-flop using 3 transistors

The source of N_MOS 1 is provided with Din whereas the gate of the transistor is provided with an input clock. As soon the clock is set at high, N_MOS tends to pass the input from the source to drain. This gives us the value of Q. The inverter circuit with P_MOS 1 and N_MOS 2 inverts the value of Q to Q (bar). A capacitor C1 and C2 are placed just to hold the values of Q and Q (bar) respectively. The best part about this circuit is that we don't need any extra circuitry to hold the state of input Din when clock goes from high to low. It automatically changes its state when clock changes from low to high but never in between.

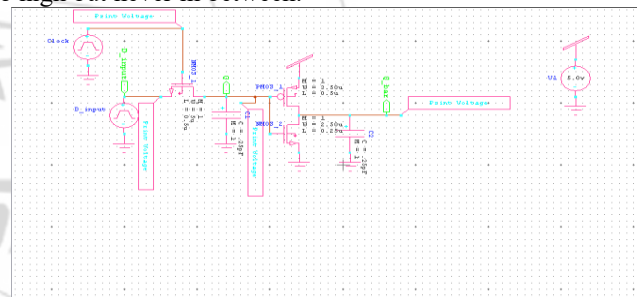


Figure 12: Schematic diagram of transistor level implementation of D Flip-flop using 3 transistors

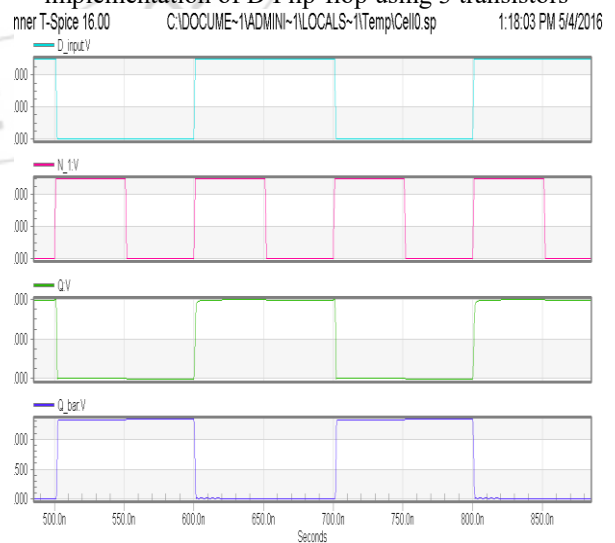


Figure 13: Output voltage waveform of D Flip-flop of 3 transistors

2.6.1. Coding in T-SPICE for D_Flip-Flop (using 3 transistors)

```
include "C:\Documents and Settings\Administrator\Desktop\Tanner Model Files\tanner models\hp05\hp05.md"
CC1 Q Gnd 250f
CC2 Q_barGnd 250f
MNMOS_1 Q N_1 D_input 0 NMOS W=5u L=500n
AS=4.5p PS=11.8u AD=4.5p PD=11.8u
MNMOS_2 Q_bar Q Gnd 0 NMOS W=2.5u L=250n
AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 Q_bar Q VddVdd PMOS W=3.5u L=500n
AS=3.15p PS=8.8u AD=3.15p PD=8.8u
VV1 VddGndDC 5
VClock N_1 GndPULSE(0 5 0 0 50n 100n)
VD_inputD_inputGnd PULSE(0 5 0 0 100n 200n)
.PRINT V(D_input)
.PRINT V(N_1)
.PRINT V(Q)
.PRINT V(Q_bar)
.end
```

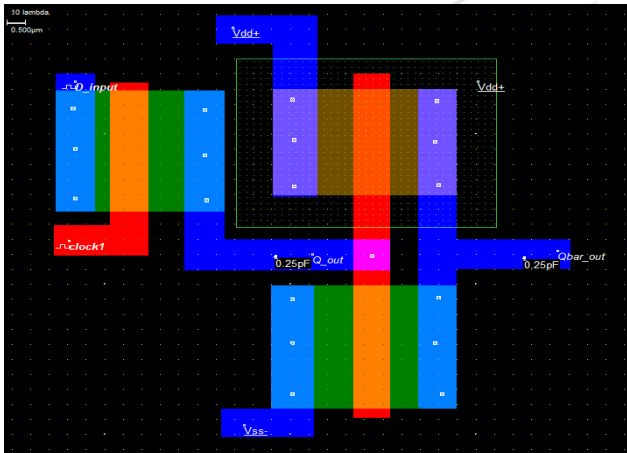


Figure 14: Layout Diagram of D Flip-Flop using 3 transistors

3. Simulation Results and Discussion

This section presents simulation setup and results. Various D flip-flops considered in this work are simulated for estimation of propagation delay and its comparative results are reported in this section.

3.1. Simulation Setup

Start time = 100ns, Stop time = 1000ns, Maximum time step = 1ns, Print start time = 400ns

Table 1: Specifications of elements used for input sources

| Elements | Pulse Width | Pulse Period | Voltage Level |
|----------|-------------|--------------|---------------|
| Clock | 50ns | 100ns | Vh=5v, Vl=0v |
| D_input | 100ns | 200ns | Vh= 5v, Vl=0v |

Table 2: Specification of MOSFETs

| Dimensions | 3 input nand gate 1 | 3 input nand gate 2 | 2 input nand gate 1 | 2 input nand gate 2 | Inverter |
|------------|---------------------|---------------------|---------------------|---------------------|----------|
| Wp | 3.5u | 3.5u | 5u | 5u | 15.5u |
| Wn | 5u | 5u | 0.5u | 0.5u | 2.5u |
| Lp | 0.5u | 0.5u | 0.5u | 0.5u | 0.5u |
| Ln | 0.5u | 0.5u | 0.5u | 0.5u | 0.5u |

3.2. Propagation delay comparison

All transistors are having the same specifications and the transient response of each design is taken, keeping the frequency of clock pulse as well as the D input same.

Table 3: Propagation delay comparison in different transistors

| No. of Transistors | FOR Q | FOR Q' |
|--------------------|--------------------------|--------------------------|
| 22 TRANSISTORS | Tlh= 36.12ns, Thl= 00ns | Tlh= xxx, Thl= xxx |
| 12 TRANSISTORS | Tlh= 6.22ns, Thl= 1.34ns | Tlh= 5.25ns, Thl= 3.53ns |
| 10 TRANSISTORS | Tlh= 0.21ns, Thl= 0.39ns | Tlh= xxx, Thl= xxx |
| 6 TRANSISTORS | Tlh= 6.76ns, Thl= 1.76ns | Tlh= 1.70ns, Thl= 0.84ns |
| 5 TRANSISTORS | Tlh= 3.99ns, Thl= 1.6ns | Tlh= 1.98ns, Thl= 1.17ns |
| 3 TRANSISTORS | Tlh= 2.21ns, Thl= 0.93ns | Tlh= 1.11ns, Thl= 1.25ns |

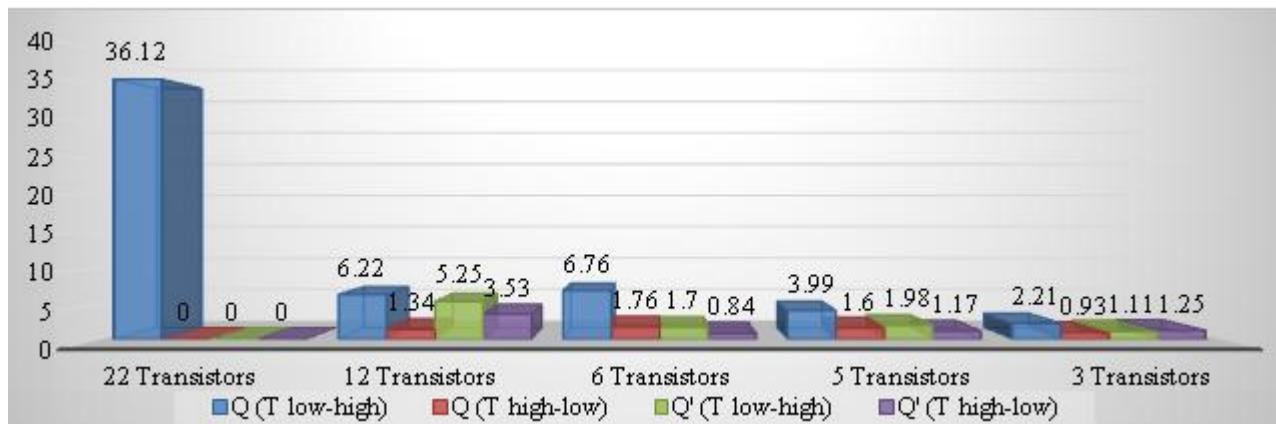


Figure 15: Comparison Chart of D Flip-Flops in terms of Propagation Delay using different transistors

4. Conclusion

In this paper we have designed an advanced or faster D flip flop using CMOS technology having minimum number of transistors and low propagation delay. We have successfully reduced the number of transistors from 22 to 3. It gives us the advantages of less complexity in designing the circuit and less propagation delay in compared to the previous results i.e., initially it was $T_{lh} = 36.12ns$, $T_{hl} = 00ns$ for 22 transistors. Performance has been improved after using 3 transistor where the values of propagation delay are reduced to $T_{lh} = 2.21ns$, $T_{hl} = 0.93ns$.

References

- [1] H. Kumar, A. Kumar, A. Islam, "Comparative Analysis of D Flip-Flops in Terms of Delay and its Variability", 978-1-4673-7231-2/15/\$31.00 ©2015 IEEE
- [2] A. Islam, A. Imran and M. Hasan, "Robust Subthreshold Full Adder Design Technique," IEEE International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT), AMU, Aligarh, India, Dec. 17-19, 2011. pp. 99 – 102.
- [3] S. Borkar, "Designing reliable systems from unreliable components: the challenges of transistor variability and degradation," *IEEE Micro*, vol. 25, no. 6, pp. 10–16, Nov. – Dec. 2005
- [4] K. G. Sharma, T. Sharma, B. P. Singh, and M. Sharma, "Modified SET D flip-flop Design for Low-Power VLSI Applications" in Proc. IEEE Int. Conf. on Devices and Communications ICDeCom), 2011 BIT, Mesra, 24-25 Feb. 2011, pp. 1-5.
- [5] M. Alioto, G. Palumbo, and M. Pennisi, "Understanding the effect of process variations on the delay static and domino logic," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 5, pp. 697–710, May 2010.
- [6] K. Rajasri, A. Bharathi, M. Manikandan, "Performance of Flip-Flop Using 22nm CMOS Technology", *International Journal of Innovative Research in Computer and Communication Engineering (An ISO 3297: 2007 Certified Organization)* Vol. 2, Issue 8, August 2014, ISSN(Online): 2320-9801 ISSN (Print): 2320-9798
- [7] Rishikesh V., Tambat and Sonal A. Lakhotiya, "Design of Flip-Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology", *International Journal of Current Engineering and Technology*, Vol.4, No.2 (Mar 2014), E-ISSN 2277 – 4106, P-ISSN 2347 - 5161 ©2014 INPRESSCO®
- [8] Kaphungkui N K, "Design of low-power, high performance flip-flops" *Int. Journal of Applied Sciences and Engineering Research*, Vol. 3, Issue 4, 2014 ISSN 2277 – 9442 Received on March 28, 2014; Accepted on April 18, 2014; Published on August 30, 2014.
- [9] Pranay Kumar Rahi, Shashi Dewangan, Tanuj Yadav and Md Muzaherul Haque "Design Simulation and Preferences Analysis of JK Flip Flop Using Various CMOS Techniques" *INTERNATIONAL JOURNAL FOR RESEARCH IN EMERGING SCIENCE AND TECHNOLOGY*, VOLUME-2, ISSUE-5, MAY-2015. E-ISSN: 2349-7610
- [10] Hardeep Kaur, Er. Swarnjeet Singh, Sukhdeep Kaur "Design and Analysis of D Flip Flop Using Different

Technologies "International Journal of Innovative Research in Computer and Communication Engineering Vol. 3, Issue 7, July 2015, ISSN(Online): 2320-9801 ISSN (Print): 2320-9798, DOI: 10.15680/ijirccce.2015.0307050

- [11] Nitin Kumar Singh Chauhan, Anshul Jain, "Comparative Analysis of low area and low power D Flip-Flop for Different Logic Values" *The International Journal Of Engineering And Science (IJES)* || Volume || 3 || Issue || 8 || Pages || 15-19 || 2014 || ISSN (e): 2319 – 1813 ISSN (p): 2319 – 1805.

Author Profile



Anu Samanta was born in 1986 in West Bengal, India. She received M.Tech degree in 2012 from NIT, Durgapur, India. She is working as an Assistant Professor in the dept. of Electronics and Communication Engineering at NSHM Knowledge Campus, Durgapur, West Bengal, India. Her research interests are Microelectronics and VLSI Design, VLSI Testing, Mixed signal IC design.



Madhu Sudan Das was born in 1981 in West Bengal, India. He received M.Tech degree in 2010 from Jadavpur University, India. Now he is pursuing PhD from IIT(ISM), Dhanbad, India. He is working as an assistant professor in the dept. of Electronics and Communication Engineering at NSHM Knowledge Campus, Durgapur, West Bengal, India. His research interests are in Control systems, VLSI, Digital Signal Processing, Antenna and Microwave and Communication Systems.