

Design of High Speed Flash Analog to Digital Converter Using Multiplexer and Comparator

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Abstract: A high speed Flash analog-to-digital converter (ADC) using mux based comparator to reduce the number of preamplifiers and comparators is introduced. A conventional N-bit flash ADC requires 2^N-1 preamplifiers and comparators while The high speed flash ADC only needs $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators .For a 6-bit resolution, the high speed flash ADC requires a reduce number of preamplifiers and comparator, compare with those of the conventional flash ADC. The high speed flash 6-bit ADC consists of a reference ladder, a T/H circuit, 10 preamplifiers, 17 comparators, a (2x1)-MUX, 8 (4x1)-MUXs and logic gates for encoder and registers. The high speed flash ADC is simulated in a 1P6M 180nm CMOS process with 1-V supply voltage and consumes 0.432-mW. At 50 MS/s, high speed flash ADC has the effective number of bits of 5.95-bit and the figure of merit of 0.15 pJ/conversion-step effective no of bit is 5.95, signal to noise distortion ratio is 37.60 db and SFDR is 45.4 db.

Keywords: ADC; T/H circuit, Multiplexer, comparator, Buffer.

1. Introduction

The signals in the real world are analog in nature for example light, sound, video etc. In order to achieve digital signal, we need to convert the analog signal into digital form by using a circuit called analog-to-digital converter. Whenever we need the analog signal back, digital-to-analog converter is required. Analog to digital converters are vital to many modern systems that require the integration of analog signals with digital systems. Electronic devices are continuously getting faster, and accordingly there is a growing need for instruments to measure their performance. Digital measuring instruments — which convert analog input signals to be measured to digital signals, and digital signal processors perform some signal processing on them — are becoming popular; hence, ADCs are essential components, and higher performance ones are being demanded. This paper describes high-speed ADC systems implemented. The applications of digital system can range from audio to communications applications to medical applications. These converters are implemented using a variety of architectures, sizes and speeds. The demand for the converter is oriented on area, speed, power of the converters. This has led to the investigation of alternative ADC design techniques. A conventional N-bit flash ADC requires 2^N-1 preamplifiers and comparators while The high speed flash ADC only needs $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators. As a result, the this flash ADC architecture has smaller size and lower power consumption. In addition, the operation speed is improved since the total input capacitance of the preamplifiers and comparators is decreased respectively.

2. High Speed Flash ADC Architecture:

Fig. 1 shows the architecture of the high speed 6-bit Flash ADC using multiplexers. This 6-bit high speed ADC consists of a reference ladder, a passive track and hold (T/H) circuit,

10 preamplifiers, 17 comparators, a (2x1)-MUX, 8 (4x1)-MUXs and logic gates for encoder and registers.

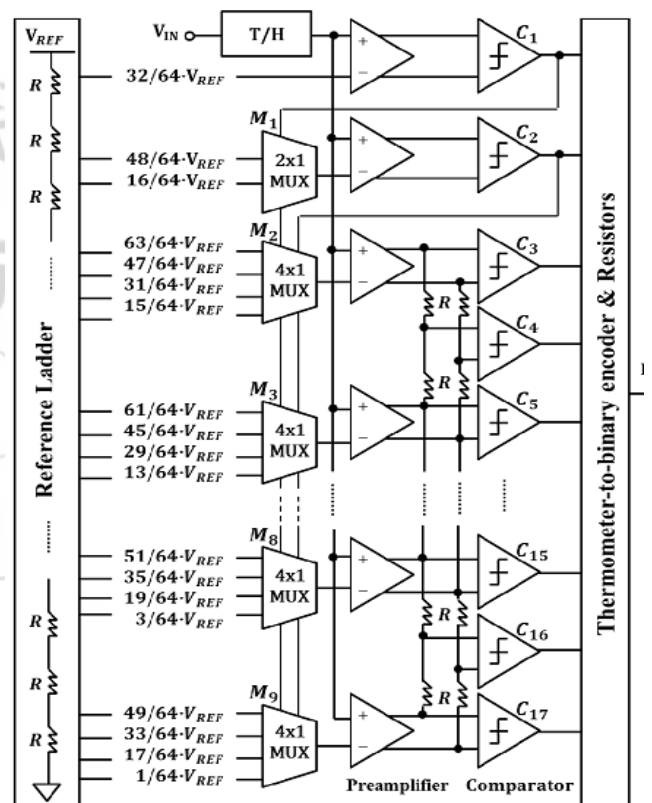


Figure 2.1: High Speed Flash ADC Architecture

The first comparator, C1, compares the sampled and amplified input signal with the middle reference level, $32/64 \cdot V_{REF}$. It decides the most significant bit (MSB) of the digital output and the MSB becomes the control signal for the MUXs, M1 – M9. The second comparator, C2, does the same but its reference signal is either $16/64 \cdot V_{REF}$ or $48/64 \cdot V_{REF}$ through the (2x1)-MUX, which is determined by the control signal from the output of the first comparator. And

then these two MSBs, the outputs of the first and second comparators, decide the reference voltages for the remaining comparators, C3 – C17, through (4x1)-MUXs. In order to reduce the number of preamplifiers and (4x1) MUXs, the interpolation technique using two resistors is applied. The outputs of the remaining comparators are encoded into appropriate values and then all digital bits are output at the same time. The main problem with the conventional flash architecture is that the number of comparators increases exponentially with the number of bits. For N bits, $2^N - 1$ comparators are needed. Due to the large number of comparators the number of bits is usually limited to 10, since the chip area and power consumption would be too large for higher resolutions. One more problem caused by the large number of comparators is the large input capacitance. To drive such a large input capacitance, preamplifiers are needed. Since such preamplifiers consume extra power, it is therefore important to reduce the number of input preamplifier pairs. The interpolation techniques are used to reduce the number of preamplifiers, but the number of comparators still remains at $2^N - 1$ for an N-bit converter. On the other hand, the proposed ADC architecture using multiplexers needs only $2^{(N-3)} + 2$ preamplifiers and $2^{(N-2)} + 1$ comparators. The number of comparators needed for the proposed ADC can be calculated as below. Since the first comparator (C1) decides the MSB with the middle reference level, the number of comparators except for it can be reduced by half, compare to the traditional flash architecture. As a result of this procedure, the number of comparators are reduced from $2^N - 1$ to $2^{(N-1)}$ for N-bit ADC. Similarly, due to the use of the second comparator (C2) with the $1/4 \cdot V_{REF}$ and $3/4 \cdot V_{REF}$, the number of comparators except for these two (C1 and C2) can be reduced by half, resulting in the total number of comparators of $2^{(N-2)} + 1$. The number of preamplifiers required is also reduced from $2^{(N-2)} + 1$ to $2^{(N-3)} + 2$ since the interpolation by two resistor technique was used.

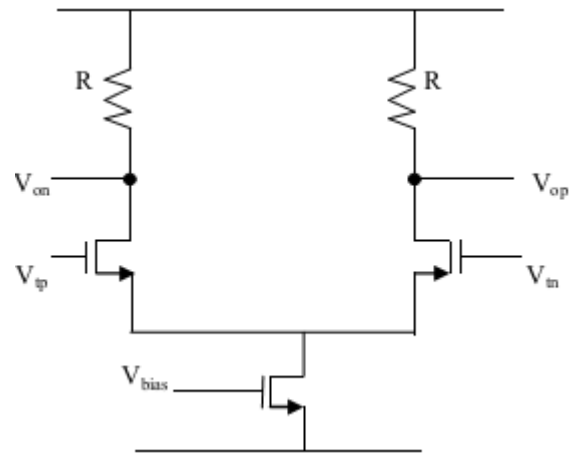


Figure 3.1.1: A Resistive-Load Preamplifier

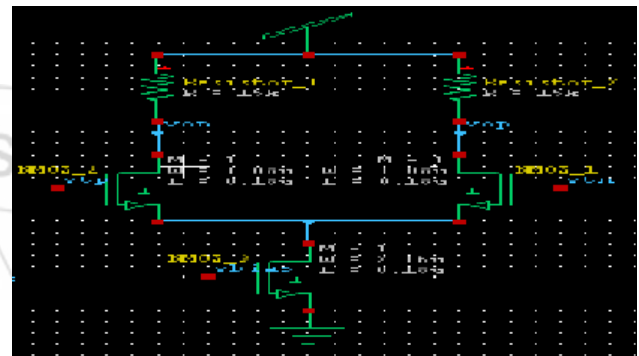


Figure 3.1.2: Simulation of preamplifier

Comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison and works on two phases reset and regeneration phase. It is a very crucial component of an analog to digital converter (ADC). Latch comparators are being used in today's A/D converters extensively because these comparators are high speed, lesser power consumption. It is used to compare the input signal with the reference voltage levels. The cross-coupled inverter placed above the input pair regenerates the input analog signal into a full-scale digital signal. This circuit is connected with SR latch to hold the output from the comparator. This gives the output at clock pulse when the input is greater than the reference voltage level. The fig shows the latch comparator simulation and performance.

Resolution (bit)	Flash		Proposed	
	Preamp	Comparator	Preamp	Comparator
N	$2^N - 1$	$2^N - 1$	$2^{(N-3)} + 2$	$2^{(N-2)} + 1$
4	15	15	4	5
6	63	63	10	17
8	255	255	34	65
10	1023	1023	130	257

3.1 Preamplifier and Latch Comparator

Preamplifier is an electronic amplifier that prepare small electrical signal for further amplification or processing. The preamplifier amplifies the input signal to improve comparator sensitivity and isolates the input of the comparator from switching noise. The Pre-amplifier is shown below in fig.

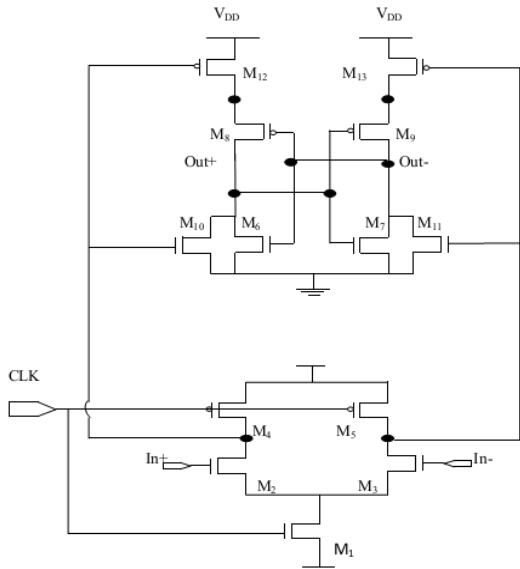


Figure 3.1.3: Latch Comparator

When clock goes high the MOSFETS M1, M2, M5, M6 turn off and M11 turn on. This provides a discharge path to ground for nodes N1 and N2 and these nodes start discharging at different rates depending on the input voltages V_{tp} and V_{tn} at M9 and M10.

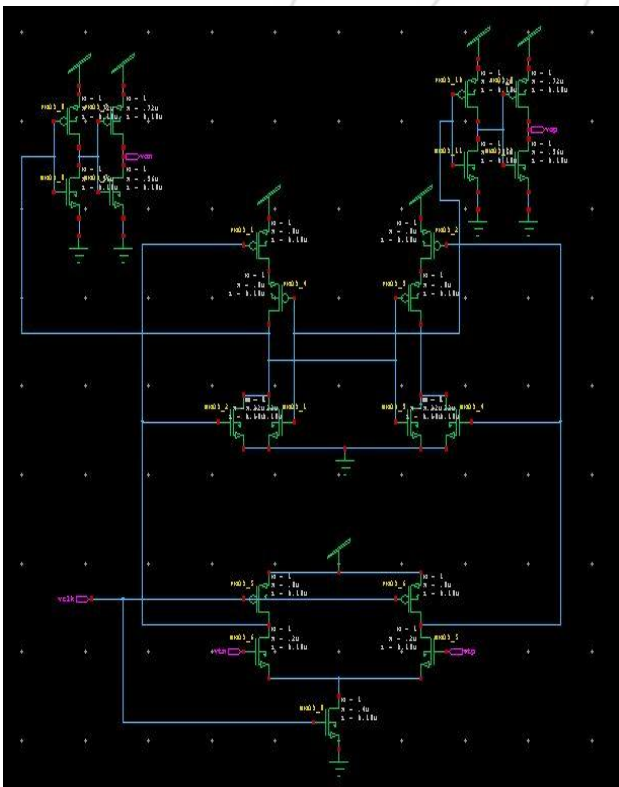


Figure 3.1.4: Simulation Of Latch Comparator

3.2 MUX-Based Thermometer-To-Binary Encoder:

A common approach to encode the thermometer code is to use a binary-ROM based encoder. It is simple to design, but it is a slow and power consuming solution. A Fat-Tree encoder using OR-gates has high complexity that makes large area cost unavoidable and the problem of bubble error. To deal with bubble error, a Wallace tree encoder can be used. It

is built by using full-adders and operates as an ones counter. The encoder is based on binary search algorithm. The inputs (1-7 and 9-15) are given to multiplexers and the middle bit (8) is used as select signal. If I_8 is 0 the inputs 1-7 are passed to second stage and the middle of these is used as select signal and b_2 of output. If I_8 is 1 the upper outputs are forwarded to second stage and same process continues.

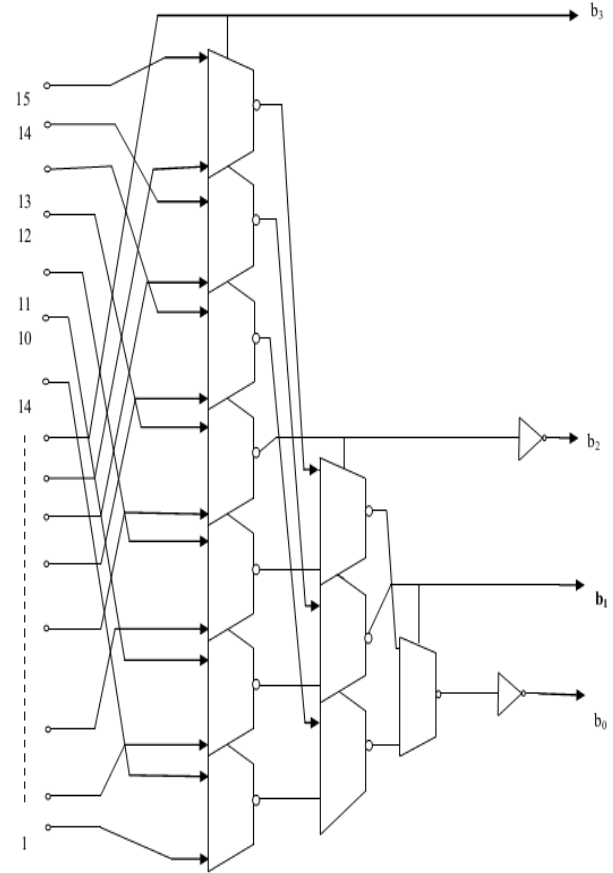


Figure 3.2.1: MUX-based encoder for 4-bit flash ADC

3.3 Reference Ladder Network

The Resistive ladder is provided in the circuit to get different voltage levels and they can be compared with the input signal which correspondingly turns the comparator on or off. In case of resistive ladder, with the help of reference ladder we have generate 16 different Voltage levels and further another reference ladder is used to select different states of multiplexer. Below fig (3.3.1) shown the resistive reference ladder is divided in to two because to increase the reference step size, which can alleviate the design difficulty of the comparator circuits.

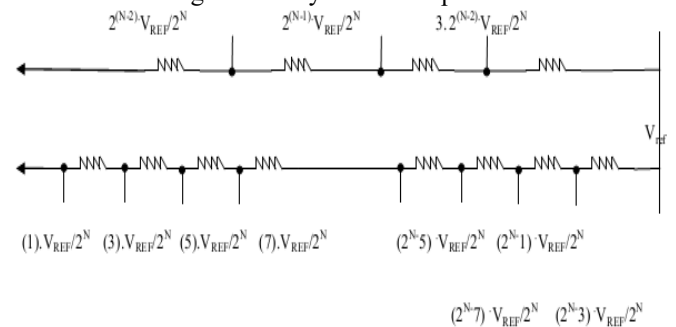


Figure 3.3.1 Two separate resistor ladder

3.4 Simulation Results

This high speed flash 6-bit ADC is designed with an HSPICE using 1P6M 180nm CMOS process with 1-V supply voltage and consumes 0.432-mW. At 50 MS/s, high speed flash ADC has the effective number of bits of 5.95-bit and the figure of merit of 0.15 pJ/conversion-step effective no of bit is 5.95, signal to noise distortion ratio is 37.60 db and SFDR is 45.4 db.

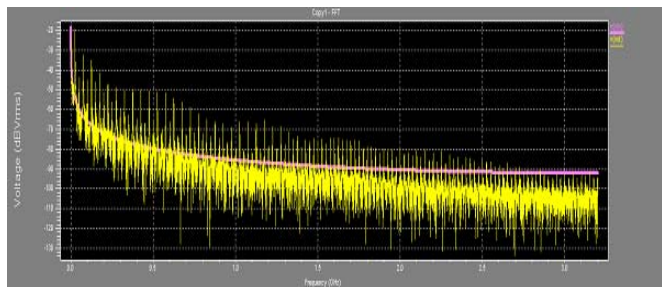


Figure 3.4.1: FFT spectrum at 24-MHz input and 50-MHz sampling

Fig. 3.4.1 shows the simulated FFT spectrum for a full-scale 24-MHz input signal while sampling at 50-MS/s.

The table 1 shows the summary of the high speed flash ADC performance at 50-Ms/s. Table 2 lists the comparison of this work with other 6-bit flash ADCs.

Table 1: Specification Summary

Specification	Simulation Result
Technology	0.18 μ m CMOS
Supply Voltage	1V
Sampling Rate	50 MS/s
Power	0.432Mw
ENOB (@ f_{in} =Nyquist)	5.95 bit
SNDR (@ f_{in} =Nyquist)	37.60 db
SFDR (@ f_{in} =Nyquist)	45.4 db
FOM	0.15 pJ/conv-steps

Table 2: Comparisons To Flash ADCs

Publication Title	MWSCAS '2009	CICC '2011	TENCON 2013	THIS WORK TENCON 2016
Technology	90 nm	90 nm	0.18 μ m	0.18 μ m
Supply Voltage(V)	1	1.2	1	1
Power(Mw)	72	12	0.539	0.432
ENOB (bit)	-	4.94	5.46	5.95
Resolution (bit)	6	6	6	6
Sampling Rate (MS/s)	1000	400	50	50
FOM (pJ/conv.-step)	1.13	0.97	0.18	0.15

3.5 Conclusion

A conventional N-bit flash ADC requires 2^N-1 preamplifiers and comparators while The high speed flash ADC only needs $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators .For a 6-bit resolution, the high speed flash ADC requires a reduce number of preamplifiers and comparator, compare with those

of the conventional flash ADC. As a result, the High speed flash ADC architecture has smaller size and lower power Consumption.

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