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DMC Based Router Architecture for Dynamic Network on Chip

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Abstract: ***Network on Chip is the most viable solution for establishing communication among various modules in a System on Chip. A modified Error correction and detection mechanism is proposed in this paper which is applicable for the Dynamic Network on Chip. In DyNoC, the position and the number of components may vary during runtime The architecture of an such an NoC router is considered and significant modifications are made in the error detection and correction regime. The architecture is modelled using VHDL in Xilinx ISE Design Suite 13.2.***

Keywords: Network on Chip (NoC), DyNoC, Error Correction, Routing Algorithm

1. Introduction

As a result of the rapid developments in the field of VLSI, billions of transistors are supposed to be fabricated in a single chip. For establishing communication among these elements, traditional wiring becomes less reliable. Network on Chip (NoC) is the best available solution for these complex wiring issues in SoC. Network on chip (NoC) has become the most assuring and legitimate solution for connecting many cores in system on chips (SoC). It also increases the throughput without using further channels for interconnection.

Also there should be a routing algorithm that decides the path to be traversed for a data packet from source to destination through the routers. It should be free of deadlock and live lock.

Network topology is the arrangement of routers and processor connection on the device. 2-D mesh topology is the most commonly used topology, which looks like an arrangement of tiles as shown in Fig.1. Normally, the router consists of FIFO buffers, control logic and arbiter.

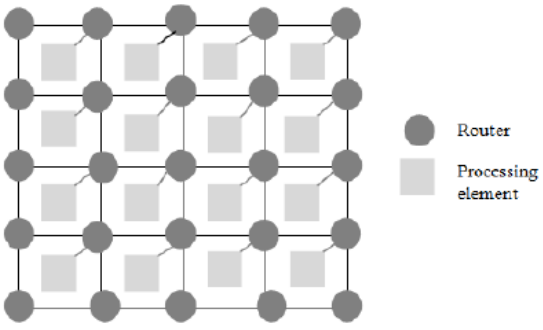

Figure 1: 2D Mesh Topology

Buffers are used for storing the data in order to forward the message in First In First Out basis. Control logic synchronizes the data transmission in the correct order from source to destination. Arbiter helps to avoid the congestion of data due to traffic, and the FSM in the arbiter forwards the data in a Round-robin fashion.

For meeting the real time requirements, the trend of embedded system has been moving towards Multiprocessor System on Chip (MpSoC), where the number of SoC is more. In the earlier period, the peripherals were connected through a shared bus which can be either single or multiple shared busses connected using bypass bridges and point-to-point connection between the peripherals. This development of connection led to the invention of network on chip, where the peripherals are connected by splitting into certain sub circuits via NoC.

One of the main challenges of NoC is that it has to deal with the dynamically placed reconfigurable devices which were further evolved into dynamic NoC. To obtain dynamic reconfiguration of FPGAs, configurable network was designed.

Using the inclusion of certain switching techniques, the NoC is further modified to improve the performance and manage the dynamically placed modules.

Now the focus is towards the data transmission with minimum error that can be achieved by the inclusion of error correcting techniques in the router. The path between the source and the destination is defined through routing algorithms. The routing technique and the router structure of NoC are developed in order to fulfil the requirements of communication between the peripherals and trade off between power, area and time.

2. System Architecture

The architecture mentioned in this paper is an NoC router; which can overcome both dead and live locks. The block diagram of the router is shown in fig 2. It is suitable for a 2-D mesh NoC, having four directions (east, west, north and south). The PES and IPS can be connected directly to any side of a router. So, there is no need of specific connection port for a PE or IP. The proposed architecture is having four loopback modules, routing error detection, routing logic, I/O buffers, I/O ports, ECC and control signals. It's operation based on store and forward method.

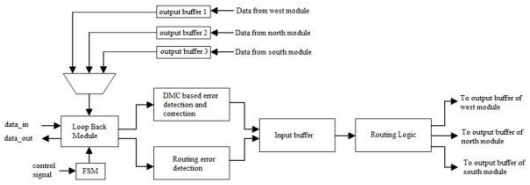

Figure 2: Block diagram of NoC router

In the previous methods, hamming code was used to correct the error in the transmitted bits. But the limitation was that, even if the path and transmitted data is processed correctly, the architecture of hamming coder is prone to fault and it cannot be used to correct burst error. Also hamming code is a single bit error detection and correction technique. So a better method is incorporated in this architecture which can detect and correct errors in multiple bits.

2.1. Routing Logic

Proper routing helps to eliminate deadlock and live lock. The routers have their addresses in the matrix format. For a dynamically reconfigurable network structure, we can use either deterministic or adaptive or a combination of these. In the case of a deterministic routing algorithm, it provides a unique path from a source to destination. XY-routing, which is also known as dimension ordering routing, is a simple deterministic routing algorithm, where the data packets are transmitted fully in each dimension, beginning with the lowest dimension available.

In a 2-D mesh network, XY-routing first routes packets along the X-axis to determine the desired column. Once the packet reaches the destination column, then they are routed along the Y-axis until the destination is reached. So, any packet moving in the Y-direction will never return to the X-direction. To avoid deadlock and live lock this routing logic will follow a loopback module.

2.2. Loopback Module

The loopback module provides a feedback to the same port, if the neighbouring router is found faulty. If there are no faulty routers in the neighbourhood, loopback module just passes the data packets to other routers or ports. Data packets enter and leave the router through this loopback module. The block diagram of loopback module is depicted in Fig. 3. The logic control block checks the availability of the neighbouring router in order to transmit the data packets.

If no loopback is required, a semi-crossbar connects the buffer to the data_out signal in order to send the data packets towards the neighbouring router. Then, a multiplexor connects the input data bus to the data_in bus. When a loopback is required, due to the unavailability of a neighbouring router, the logic control block configures the semi-crossbar block to send the considered data packet on the data_loopback bus.

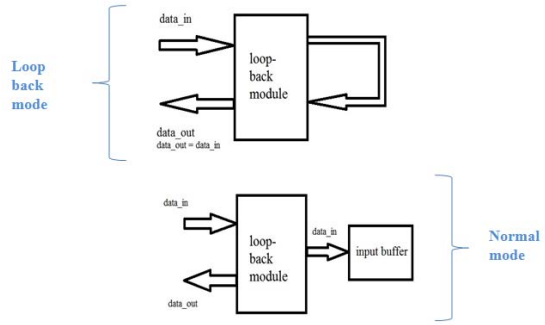

Figure 3: Block Diagram of Loopback Module

Therefore, the data packet is looped back inside the router and will be considered as a new packet. During this step, in order to avoid the reception of a new data packet from the neighbouring switch, the occ_out signal is activated. The functional diagram of loopback module is depicted in Fig. 4

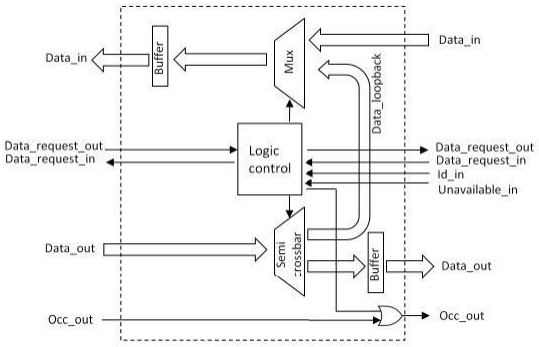

Figure 4: functional diagram of loopback module

2.3 Routing Error Detection

The error may occur due to two reasons: either due to the alternation in the message value being sent or due to the wrong routing path. The routing path in turn causes deadlock and live lock. In order to avoid this, a routing error detection block is added on the RKT switch. When a message is passed from one IP core to another IP core via certain router, it has to check whether the operation is done correctly. For that, a router has to check two things: whether the packet is in the current router and whether the previous router obeys the XY algorithm. If it obeys the algorithm, then the router confirms that the router has no error or else, it checks the availability of the router in the path, by checking the diagonal availability indication. If diagonal availability is unavailable, it then checks whether the input for this router is for bypass operation. If not it confirms the router has an error or else it confirms that the router has no error.

2.4 Error Correction Code

The decimal matrix code (DMC) based on divide-symbol is proposed to provide enhanced memory reliability. DMC utilizes decimal algorithm (decimal integer addition and decimal integer subtraction) to detect errors. The advantage of using decimal algorithm is that the error detection capability is maximized so that the reliability of memory is enhanced. Besides, the encoder-reuse technique (ERT) minimizes the area overhead of extra circuits (encoder and decoder) without disturbing the whole encoding and

decoding processes, because ERT uses DMC encoder itself to be part of the decoder. The structure of 32 bit encoder and decoder is shown in Fig 5 and Fig 6 respectively.

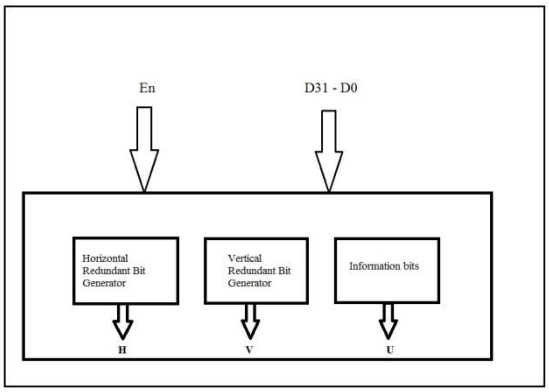

Figure 5: 32-bit DMC encoder

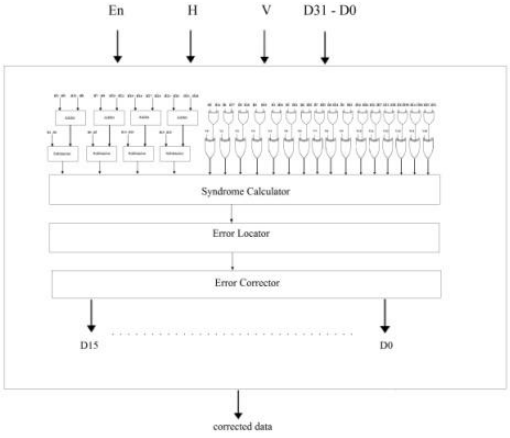

Figure 6: 32-bit DMC decoder structure

3. Experimental results

The NoC architectures is simulated. In this NoC the message takes an alternate path to reach the destination even if there is faults in the propagating path .So the message reach the destination even if the router in the transmitting path is faulty. The data transmitted is free of error due to the efficient exploitation of Decimal Matrix Code. The simulation output for different modules are shown in Figure.7 to 12

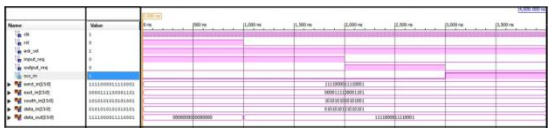

Figure 7: North Module

Figure 8: South module

Figure 9: East module

Figure 10: West module

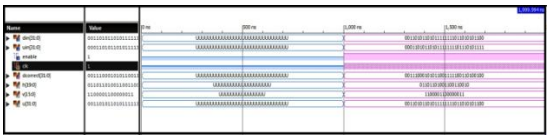

Figure 11: Error Correction Code

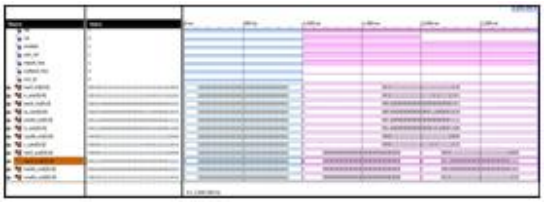

Figure 12: NoC with modification

4. Conclusion

The NoC router is highly reliable when compared with ordinary NoC due to the addition of error detection mechanism in the design and it avoids the dead lock and live lock problem. Hence it shows better performance in operation and due to the presence of error correcting code the repeated usage of the logic elements reduces and hereby it is clear that the designed RKT-NoC is more advantageous than the ordinary NoC.More over the DMC helped to make the architecture more reliable.

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