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Manchester Encoding and QPSK Modulator for SDR

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Abstract: ***Modulator and encoding designs are mostly developed for application-specific integrated circuit (ASIC). Such system suffers great limitation as integrated circuits are not programmable. Field-programmable gate arrays (FPGAs) solve this problem by introducing reconfigurable hardware. Digital communications devices designed on FPGAs have the capability to accommodate multiple communications protocols without replacing existing hardware. For these reasons, FPGAs proves to be the ideal platform for implementing adaptive communications systems. This paper focuses on Manchester encoding and QPSK modulator design which falls as two major entities in modern communication system. The proposed system is designed to achieve low power consumption and reduced size compared to conventional analog devices. The system is developed in Xilinx platform using Verilog system design tool. Verilog enables fast and reliable operation and can be implemented in FPGAs. Thus making system reconfigurable on application.***

Keywords: QPSK, Manchester encoding, SDR, FPGA, Wireless communication

1. Introduction

Software defined radios (SDR) is fast developing field in the field of telecommunication. Recent trend in SDR has been used for rapid prototyping of communication systems. They include radar design, global positioning system. Adaptive optics design.Many real-time applications such as advanced control system design, system performance measurement, data acquisition, and processing use the field-programmable gate array (FPGA) integrated with PCI Extension for Instrumentation (PXI) platform for implementation.

Manchester encoding improves efficiency of SDR system. In telecommunication, Manchester coding is a coding in which each binary data bit is coded as either low then high, or high then low. This type of coding is therefore self-clocking and clock signal can be recovered back from data. In this technique, the actual binary data to be transmitted over the cable are not sent as a sequence of logic 1's and 0's (known technically as Non Return to Zero (NRZ)). Instead, the bits are translated into a slightly different format that has a number of advantages over using straight binary encoding (i.e. NRZ).

Modulation is the process of sending data signal over carrier signal to minimize the noise or fading effect. They are mainly divided into two categories i.e., analog and digital. In analog modulation carrier signal is modulated with the help of analog data signal and in digital it modulates with digital signal. Digital modulation is called shift keying because in this, the carrier signal is shifted in amplitude, frequency or phase by digital input signal. Different PSKs can be obtained by M-ary PSK, where M is the no. of states or no. of phase shifts which is depend upon the no. of signals are combined for modulation. In QPSK two signals are combined for modulation. BER of QPSK is better than higher order PSK signals such as 8-PSK, 16-QAM, 32-QAM etc. which are easily affected by noise. At higher order PSK, larger bandwidth is require for higher data transfer rate and consume more power, whereas QPSK is more bandwidth as well as power efficient.

2. Conventional System

QPSK can modulate a signal with twice bandwidth as compared to BFSK at same bit error rate. Each signal is to be converted from analog to digital, then modulate one signal with sine and another with cosine which gives four different phase shifts with two signals, by adding these two phase shifted signals we get QPSK output signal. QPSK signal is given as:

$$Sqpsk = \frac{\sqrt{Es/Ts}}{1}\cos((2\pi fc + (i-1)\frac{\pi}{2}) \text{ for } i = 1,2,3\ldots\text{etc.}$$

Where

$\sqrt{Es/Ts}$= constant amplitude for Es energy.

fc = frequency of carrier.

i = Phase number of signal.

Conventional system splits the signal to in-phase and quadrature phase which is the multiplied with sine and cosine signal respectively. The above analysis shows that QPSK can be used to double the data rate compared to BFSK signal. The two signals are then superimposed and the resulting signal is a QPSK signal. A non-return to zero encoding is usually performed before processing of binary data. There are many applications where QPSK modulator is used, out of which few are of battery operated devices such as Bluetooth, TDMA cellular communication.

3. Proposed System

Modulation design of proposed design for QPSK modulation and Manchester encoding is discussed detail in following section.

3.1 Manchester encoding

In the Manchester encoding shown, logic 0 is indicated by a 0 to 1 transition at the centre of the bit and a logic 1 is indicated by a 1 to 0 transition at the centre of the bit. Some cases we will see the encoding reversed, with 0 being represented as a 0 to 1 transition. The two definitions have co-existed for many years. The Ethernet Blue-Book and IEEE standards (10 Mbps) describe the method in which a Logic 0 is sent as 0 to 1 transition and a Logic 1 as a one to zero transition (where a zero is represented by a less negative voltage on the cable). The proposed system follows IEEE standard.

A Manchester encoded signal contains frequent level transitions which allow the receiver to extract the clock signal using a Digital Phase Locked Loop (DPLL) and correctly decode the value and timing of each bit. To allow reliable operation using a DPLL, the transmitted bit stream must contain a high density of bit transitions. Manchester encoding ensures this, allowing the receiving DPLL to correctly extract the clock signal. The bi-phase Manchester encoding can consume up to approximately twice the bandwidth of the original signal (20 MHz). This is the penalty for introducing frequent transitions.

Note that signal transitions do not always occur at the 'bit boundaries' (the division between one bit and another), but that there is always a transition at the centre of each bit. The encoding may be alternatively viewed as a phase encoding where each bit is encoded by a positive 90 degree phase transition, or a negative 90 degree phase transition. The Manchester code is therefore sometimes known as a Biphase Code.

Thus frequency is doubled and DPLL is used at receiver. This proposed system implements the same functionality at transmitter. The system is shown in Figure 1.

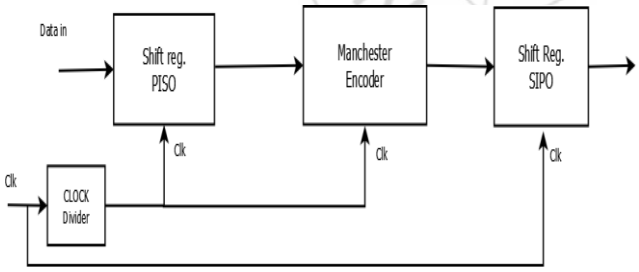

Figure 1: Manchester encoder design

Data rate is doubled after Manchester encoding. Total number of bits in the frame N becomes 2N.

$$d(t) = \sum_{i=0}^{2N-1} (b_i P(t - iT_b)$$

Where b_i is the i^{th} no. of bits in the frame. Thus producing 1 and 0 for every binary 1, 0 and 1 for every binary 0 respectively.

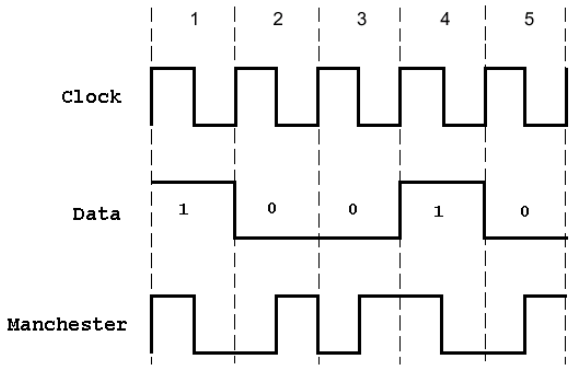

Figure 2: Manchester timing.

3.2 QPSK Modulation

The QPSK modulator can modulate two signals in same frequency band as shown in Figure Each signal is to be converted from analog to digital, then modulate one signal with sine and another with cosine which gives four different phase shifts with two signals, by adding these two phase shifted signals we get QPSK output signal. Conventional systems are analog based system and model that uses circuit approach.

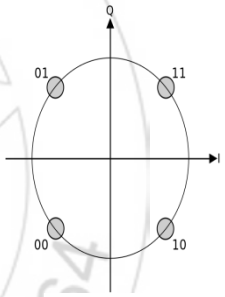

Figure 3: Constellation diagram

The constellation diagram shows (Fig 3.) the phase angle and amplitude of signal when different symbols are used. The transmitted "carrier" can undergo any number of phase changes and, by multiplying the received signal by a sine wave of equal frequency, will demodulate the phase shifts into frequency-independent voltage levels. This is indeed the case in quadraphase-shift keying (QPSK). With QPSK, the carrier undergoes four changes in phase (four symbols) and can thus represent 2 binary bits of data per symbol. Although this may seem insignificant initially, a modulation scheme has now been supposed that enables a carrier to transmit 2 bits of information instead of 1, thus effectively doubling the bandwidth of the carrier.

The phase shift angle may be 0 degree, 90 degree, 180 degree and 270 degree or 45 degree, 135 degree, 225 degree, 315 degree. The proposed system uses shifting from 0 degree.

So, instead of generating the phase shift by multiplying data signal with carrier one, we will just store the signal in ROM and call it for specific symbol from specific phase. It means the output waveform will be the same sinusoidal signal with starting from specific phase angle.

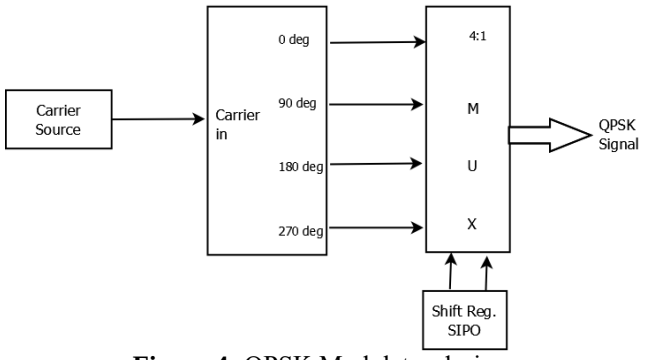

Figure 4: QPSK Modulator design

3.2.1Blocks

The major blocks used to generate the signal and its working is as follows:

- Carrier source provides a carrier signal of a particular frequency. The signal data is stored in memory and read using Verilog coding. This carrier is passed to phase shifter where further processing is done
- Phase shifter changes the phase of carrier into respective angles so as to be selected by multiplexer based on input.
- The data has to be modified and combined to form a pair of two binary bits. This acts as a selection line.

The QPSK signal based on input is produced at the output of multiplexer.

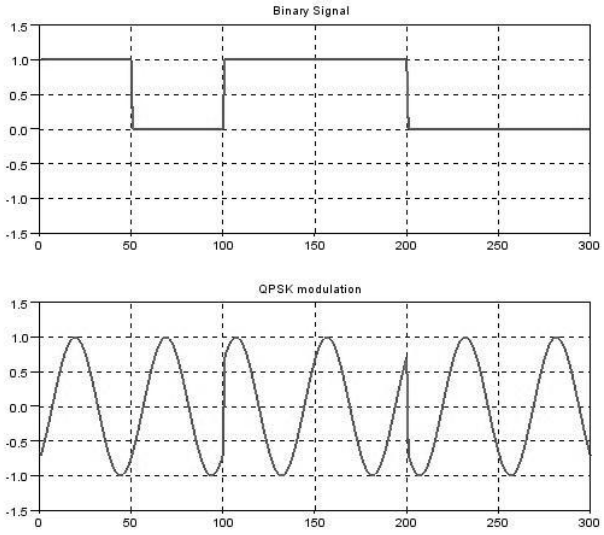

Figure 5: QPSK Timing

4. Simulation Results

Simulation results for Manchester encoding and QPSK obtained when programmed using Verilog coding is shown in figure. The data can be further viewed as wave if plotted using Matlab.

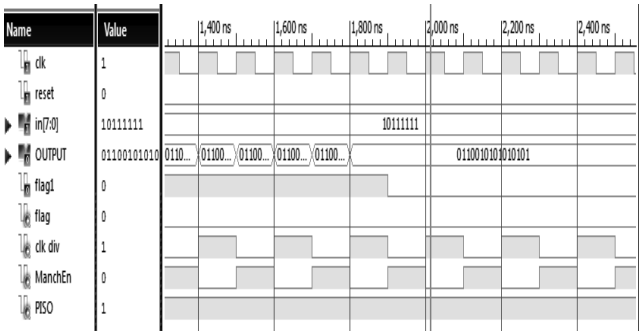

Figure 7: Manchester encoding

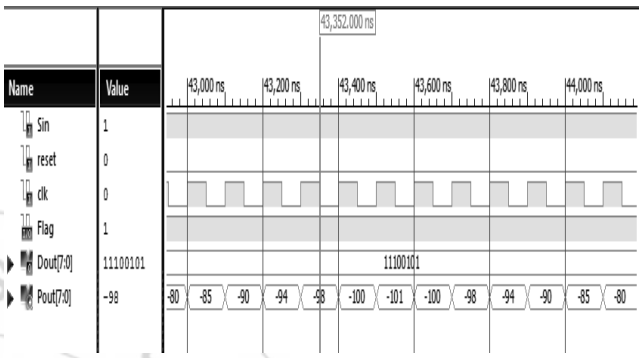

Figure 8: QPSK modulation

5. Conclusion

In this paper, a QPSK modulation design that a Manchester encoder design along with QPSK modulator design is being proposed. This design tries to achieve the same result by reducing the effective size of system. Both designs are expected to achieve reduced power consumption as there is a reduction in size. The system has been designed inXilinx platform using Verilog System Design tool. Verilog enables the system to fast, reliable and easy burning into an FPGA. Analysis of system can be done using study of intermediate processes.

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