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Design and Performance Analysis of TFA Cell Using CNTFET

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Abstract: ***In this paper a clocked ternary full adder cell using Carbon nanotube field effect transistor (CNTFET) is proposed in which pull-up and pull-down networks are used along with a clock reset circuit and a MUX at the output. Ternary logic is preferred for the design over conventional binary logic as it helps to reduce circuit complexity and hence reduces chip area. The performance of proposed TFA cell is evaluated and compared with the reference design in terms of parameter such as power dissipation and delay.***

Keywords: Carbon nanotube FET (CNTFET), Ternary full adder (TFA), pull-up network (PUN), pull-down network (PDN).

1. Introduction

Using ternary logic reduces the chip area as well as the complexity of interconnects by enhancing their information contents [5]. Hence, simplicity and energy efficiency in designing of circuits is obtained as compared to the conventional binary logic. Ternary circuits design is performed using the multiple-threshold method and the desired threshold voltage is achieved by utilizing different diameters of CNT [3-4].

This paper proposes a novel design of CNTFET-based ternary full adder cell. The prime objective of this paper is to improve the power dissipation so that it can be use to obtain high performance in arithmetic operations. A TFA cell adds three input bits and generates two outputs SUM and Cout. The design of ternary full adder is performed using pull-up network, pull-down network [1] and the clocked reset circuit.. Inputs A and B uses the ternary logic while Cin is of binary nature hence it simplifies the design and also reduces the propagation delay and energy consumption in a design. The maximum value of the sum of two 1-bit ternary numbers is at most 5 which produce Cin at most equal to logic 1. Therefore, Cin will have only two logic values 0 and 1.

2. Proposed TFA cell

In the proposed TFA cell PUN, PDN are used along with clocked reset circuit and a MUX at the output. CNTFET based ternary full adder cell discussed in 5.2 turns on pull-UP and pull DOWN networks simultaneously in case when output is logic ‗1'(middle level). In this technique complete circuit works on concept of potential divider and provides intermediate voltage. This is not static operation as CMOS logic and results in a direct path between V_{DD} and GND. This shorting results in more power consumption in a design. In the proposed work our main focus is on this problem and to eliminate this problem of short circuit in TFA clocked reset circuit are used. In this paper, an operating voltage of 0.9V (default value of the CNTFET Stanford model [6]) is used. Therefore, ternary logic values symbolized by 0, 1 and 2 have voltage levels of 0V, 0.45 V and 0.9V respectively. Both the networks (PUN and PDN) used in TFA utilize transistors with diameter of 1.487nm and the threshold voltage, chirality vector of these transistors are 0.282V and (19, 0) respectively.

The schematic of decoder presented in Figure 1 where ‗B' refers to binary gates. It contains negative ternary inverter (NTI), positive ternary inverter (PTI) [8] and binary gates for the generation of different unary functions [2].

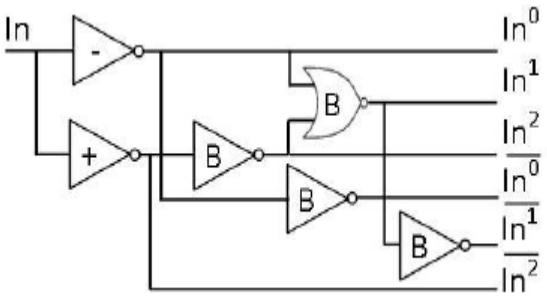

Figure 1: Ternary decoder

2.1 Proposed sum generator

The pull-up and pull-down network outputs are used separately in proposed circuit. The outputs from PUN and PDN drive the MUX and the MUX circuit is designed so as to select correct result at the output. Outputs Su, Sd (from PUN and PDN) are connected to MUX inputs to generate final outputs. Reset logic is used to avoid undriven logic states at the input of MUX therefore reset logic is required to reset inputs Su and Sd (SU=SD=0) by connecting PUN output to GND and PDN output to Vdd. When the clock is in ON state the outputs of PUN and PDN are latched at the input of MUX and corresponding output is obtained while in case of reset clock Su and Sd are at logic ‗0' and hence the sum output through the MUX is also at logic ‗0'.On the basis of table the equation (1),(2) and (3) are written below as;

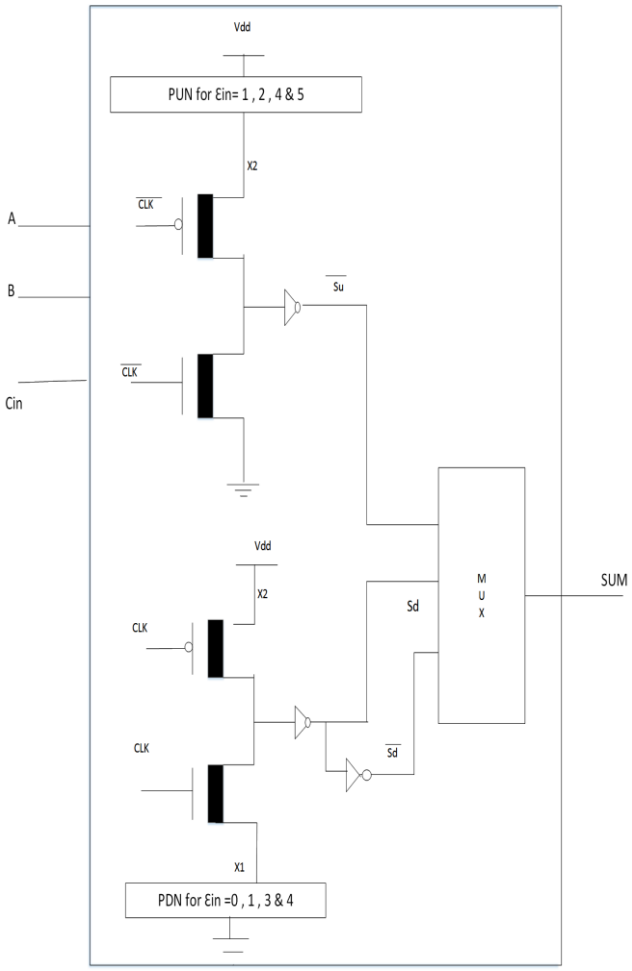

Figure 2: Proposed TFA sum generator

Table 1: Switching in sum and Carry generator

∑in	Sum generator			Carry generator	
	PUN	PDN	SUM	PUN	Cout
0	OFF	ON	0	OFF	0
1	ON	ON	1	OFF	0
2	ON	OFF	2	OFF	0
3	OFF	ON	0	ON	1
4	ON	ON	1	ON	1
5	ON	OFF	2	ON	1

$$X_1 = 0*[A^0(B^0\overline{Cin^2} + B^1Cin^0 + B^2\overline{Cin^0}) + A^1(B^2\overline{Cin^2} + B^0Cin^0 + B^1\overline{Cin^0}) + A^2(B^0\overline{Cin^0} + B^2Cin^0 + B^1\overline{Cin^2})] \quad (1)$$

$$X_2 = 2*[\overline{A^0}(\overline{B^1}Cin^2 + \overline{B^0}Cin^0 + \overline{B^2}\overline{Cin^0}) + \overline{A^1}(\overline{B^2}Cin^0 + \overline{B^0}Cin^2 + \overline{B^1}\overline{Cin^0}) + \overline{A^2}(\overline{B^0}\overline{Cin^0} + \overline{B^1}Cin^0 + \overline{B^2}Cin^2)] \quad (2)$$

$$X_3 = 2*[\overline{A^0}\overline{B^2}Cin^0) + \overline{A^1}(\overline{B^2}\overline{Cin^0} + B^0Cin^0) + \overline{A^2}(B^0\overline{Cin^0} + Cin^0)] \quad (3)$$

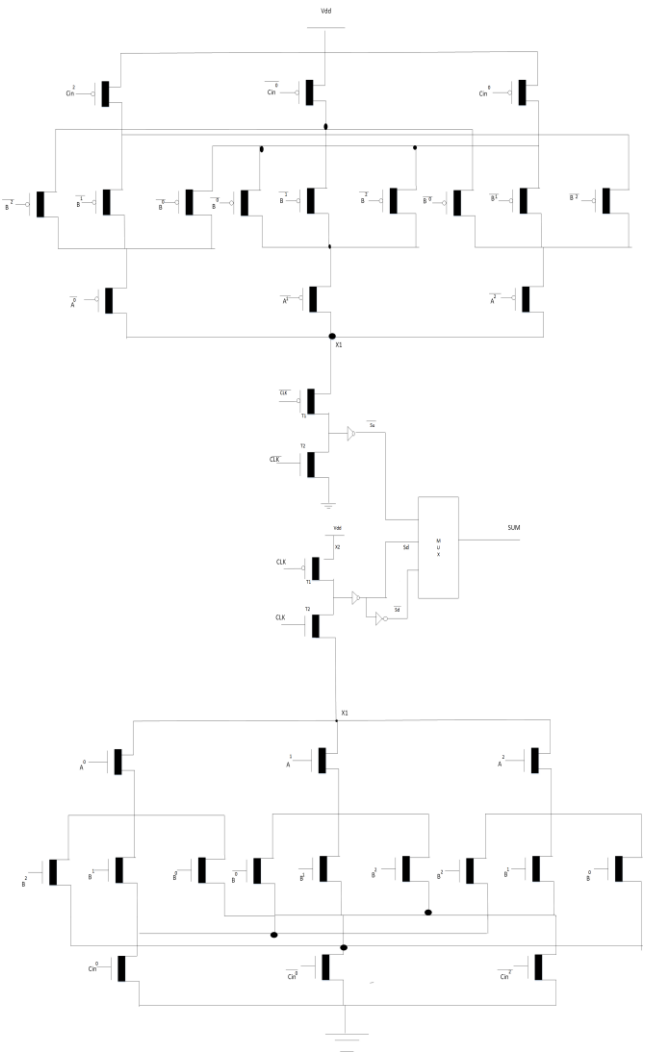

Figure 3: TFA Sum generator using CNTFET

2.2 Proposed carry generator

For carry logic, the pull-down network is eliminated as carry output is either logic ‗0' or logic ‗1' which can be done using Pull-up network and a single pull-down transistor only as shown in figure below. This logic has been used in proposed circuit with integrated MUX to obtain carry output. PUN network is cut-off for the ∑in ≤ 2 at logic ‗0' but for ∑in > 2 it will work and the input condition in the MUX is Cu=1, Cd=0.

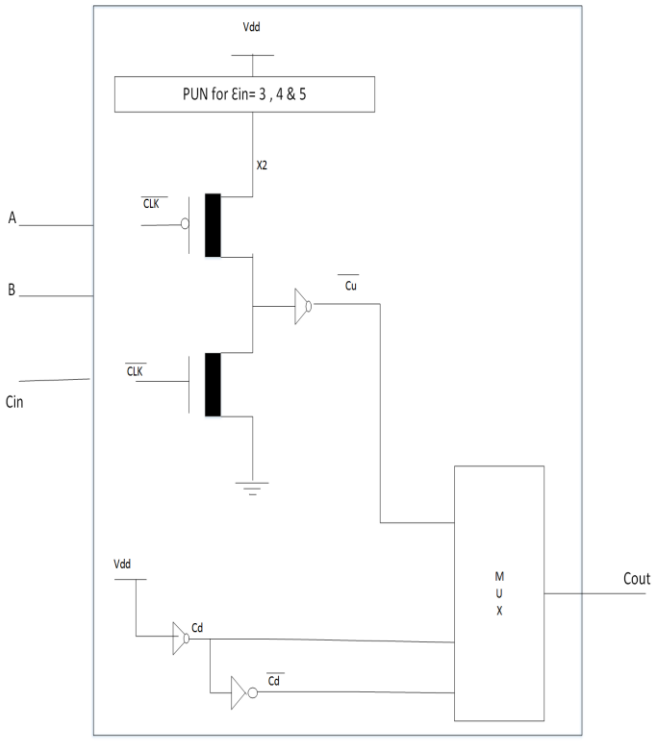

Figure 4: Carry generator with reset clock

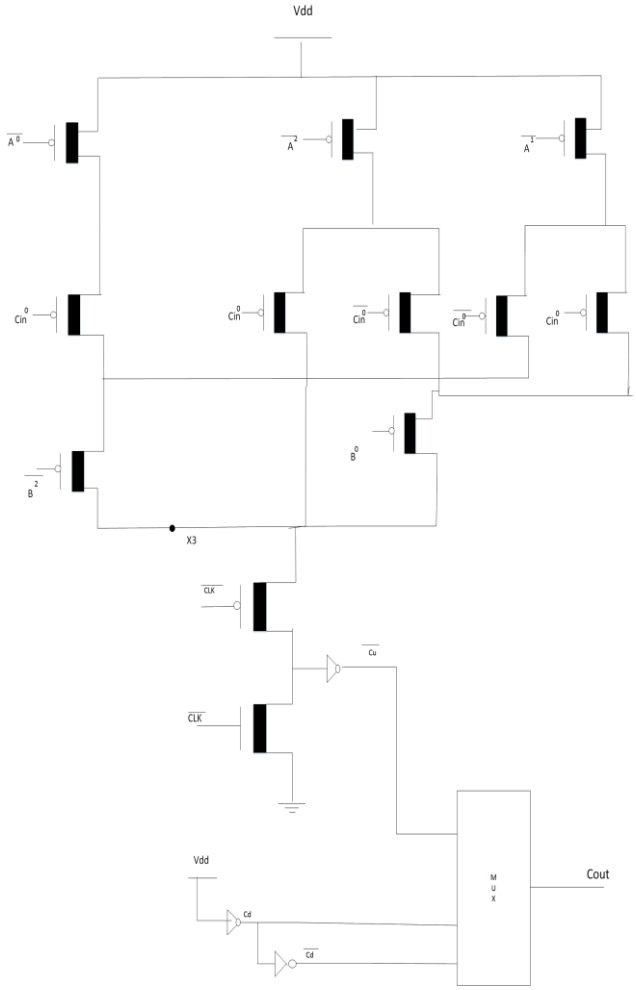

Figure 5: Carry generator using CNTFET

The MUX used at the output is shown below with truth table. When output is logic ‗2', the PU network is active and PD network is cut-off so Sd input of MUX is undriven. When output is logic ‗0', PD network is active and PU network is cut-off so Su input of MUX is undriven while in the case, when output is logic ‗1' both PU and PD networks are active and both inputs are driven Su=Sd=1 (for sum). Reset logic is required to avoid undriven logic states and therefore reset logic resets mux inputs to logic SU=SD=0.

Table 2: MUX logic table

Su	Sd	Out
0	0	0
0	1	0
1	0	2
1	1	1

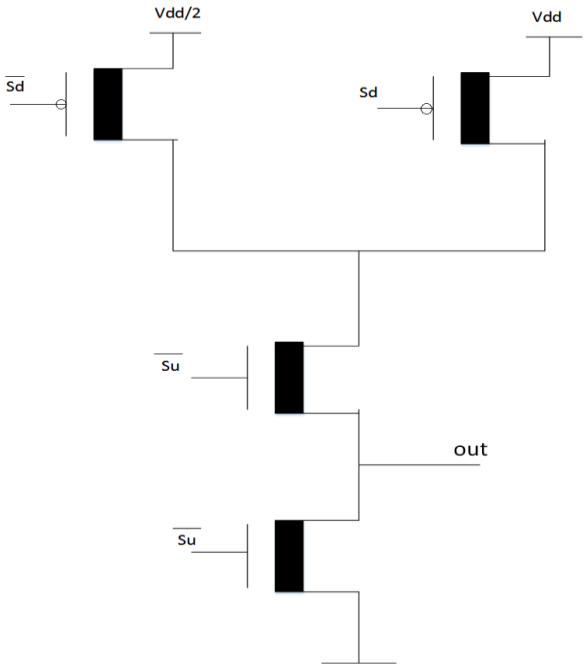

Figure 6: MUX circuit

3. Simulation and Results

The simulation has been performed for supply voltage 0.9V for the proposed TFA cell. We have evaluated propagation delay and power dissipation of the proposed design and comparison have also been made with the reference TFA cell[1] by performing simulation on HSPICE software using 32 nm CNTFET technology. Proposed TFA cell has been simulated and satisfactory result has been obtained compared to the one other reported previously.

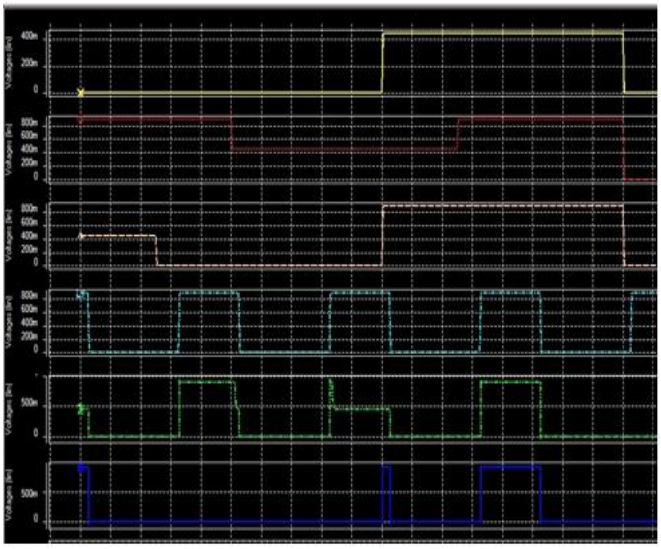

Figure 7: Simulation of TFA cell using clocked reset logic

Table 3: Performance evaluation of proposed design

Parameter	Reference design	Proposed
Power (μW)	2.870	0.047
Delay Sum (Pico sec)	330.2	123.3
Delay Carry(Pico sec)	150.1	128.3

4. Conclusion

In this chapter, a TFA cell has been proposed and the parameter are evaluated and compared with the reference design in terms of power dissipation and delay. The simulation has been performed on HSPICE software using 32nm CNTFET technology of Stanford university‘s CNTFET HSPICE model [6]. The proposed design of TFA cell is intended to achieve the lower power dissipation and the simulation result shows that the proposed design is superior to reported TFA cell.

References

[1] Murotiya, Sneh Lata, and Anu Gupta. "Design of high speed ternary full adder and three-input XOR circuits using CNTFETs." In *2015 28th International Conference on VLSI Design*, pp. 292-297. IEEE, 2015.

[2] Sridharan, K., Sundaraiah Gurindagunta, and Vikramkumar Pudi. "Efficient multiternary digit Adder design in CNTFET technology." *IEEE transactions on Nanotechnology* 12, no. 3 (2013): 283-287.

[3] G. Cho, Y. Kim and Lombardi F.,―Performance evaluation of CNFET based logic gates,” in *Proc. IEEE Int. Instrumentation and Measurement Technology Conf., Singapore*, 2009, pp. 909–912.

[4] K.Y. Bok, Y.B. Kim, F. Lombardi, ―Novel design methodology to optimize the speed and power of the CNTFET circuits,” in *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems 2009*, Cancun, Mexico, 2009, pp.1130–1133.

[5] P. C. Balla and A. Antoniou, ―Low power dissipation MOS ternary logic family,” *IEEE J. Solid-State Circuits*, vol. 19, no. 5, pp. 739–749, Oct.1984.

[6] Stanford University CNTFET Model website [Online].Available:http://nano.stanford.edu/model.php?id=23

[7] J. Deng and H.-S. P.Wong, ―Acompact SPICE model for carbonnanotube field-effect transistors including nonidealities and its application—Part II:Full device model and circuit performance benchmarking,” *IEEE Trans.Electron Device*, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.

[8] S. Lin, Y.-B. Kim, and F. Lombardi, ―Anovel CNTFET-based ternary logic gate design,” in *Proc. IEEE Int. Midwest Symp. Circuits Syst.*, Aug. 2009, pp. 435–438.

[9] K.Roy, S.Mukhopadhyay, H. Meimand-Mehmoodi, ―Leakage current mechanisms and leakage reduction techniques in deep-submicron CMOS circuits,” in *Proc. IEEE*, Feb.2003,vol.91,no. 2, pp. 305–327.

[10] C.Chen, ―Physical design with multiple on-chip voltages,” In:*International Symposium on Physical Design (ISPD'02),* 2002, pp.118-118.

[11] P. Keshavarzian, R. Sarikhani, ―ANovel CNTFET-based Ternary Full Adder,” *Circuits Syst. Signal Process*, vol. 33, pp. 665–679,2013.

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