International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2015): 6.391

Design and Analysis of f2g Gate using Adiabatic Technique

Renganayaki. G[1], Thiyagu.P[2]

[1, 2]K.C.G College of Technology, Electronics and Communication, Karapakkam,Chennai-600097, India

Abstract: ***This paper presents the comparison of conventional and two efficient adiabatic logics ECRL and PFAL. F2G gate is implemented using these two design technique. F2G gates are reversible gates. Reversible computing performed on F2G gates with adiabatic design techniques promises more reduced in power consumption as compared to traditional adiabatic CMOS circuits. Comparison in this paper shows very encouraging results in terms of average power consumption, transistor count. The designs are simulated and implemented on Cadence ICE6.1.5 virtuoso Design Environment using UMC 180 nm transistor model. The simulation results indicate that ECRL is better than PFAL, adiabatic logic at lower value load capacitancein terms of average power consumption and transistor count for implementation of F2G gates at low frequency andlow power application.***

Keywords: ECRL; PFAL;CMOS Adiabatic Logic; F2G Gates; REVERSIBLE LOGIC

1. Introduction

In present scenario of modern technology, low power circuit design methodology plays a vital role in VLSI Design. Large number of portable equipment have been introduced for sustainable green environment. The power requirement should be less with more efficiency, so to achieve this a new and different types of low power design technique is adopted. From the last few years we have been using CMOS logic to reduce power consumption. The power consumed in traditional CMOS design can be given as,

$$P=C_L.V_{DD}^2.f \quad (1)$$

Here the power (P) is proportional to switching frequency (f), capacitance (CL), and square of supply voltage (VDD).

Power consumption can be reduced by minimizing the power supply, capacitance and switching frequency of operation. But as soon as these parameters reduces, it may deteriorate the performance of the circuit. Design using adiabatic principle [1] helps in reducing power consumption at the cost of reduced performance. A method based on adiabatic technique uses an ac power supply rather than dc for the energy recovery. Theoretically adiabatic circuits consume zero power, it shows energy loss due to nonzero resistance in the switches. There are so many papers which describedifferent types of adiabatic technique such as ECRL,2PASCL,PFAL, etc. by which we can reduce power consumption of the circuit [1]. These technique will consume less power as compare to other CMOS circuits.

Due to loss of bits in conventional digital circuits during logic operation, a significant amount of energy is dissipated by the circuit. According to Landauer, the energy dissipated for each irrepressible bit of operation is given by

$$\Delta E=kT\ln 2 \text{ Joules} \quad (2)$$

Where k is Boltzmann's constant and T is temperature at which operation is performed.

If numbers of inputs are equal to numbers of outputs of a logic gate then power consumption can be decreased and this type of gate is called reversible gates. Peres gate, F2G gate and Fredkin gate are such types of reversible gates [2].If these reversible logic gate incorporate with adiabatic techniques, then more power will be saved and can achieve almost 100% of power saving.

Section II discusses necessity of low power. Section III, discusses about adiabatic logic and two different types of it, which are ECRL&PFAL. In section IV, basics of one of the reversible gate i.e. **F2G** gates, has been discussed. Section V shows the proposed circuit diagram and circuit simulated on CADENCE. The compared results are shown in section VI.

2. Motivation

Since last few decades the main challenges were Area, cost, and performance. But these days the power is an important factor instead of cost, performance and area. The device which consumes very less power irrespective of speed such as heart pacemaker, RFID etc. works on the principle of adiabatic logic. The aim of reducing power consumption is application specific, for example the battery operated portable devices such as mobile phones, the aim should be reasonable lifetime of battery, and so the total power dissipation of the circuit should be low. The authors have tried to decrease the power by combining the adiabatic and reversible.

A new method is introduced for f2g gate with ECRL and PFAL reversible adiabatic technique to achieve maximum power reduction with improved performance.

3. Adiabatic Circuits

Adiabatic circuits are basically low power circuits which use to conserve the energy by returning back its output energy to input, so that the same energy can be used for next operation.

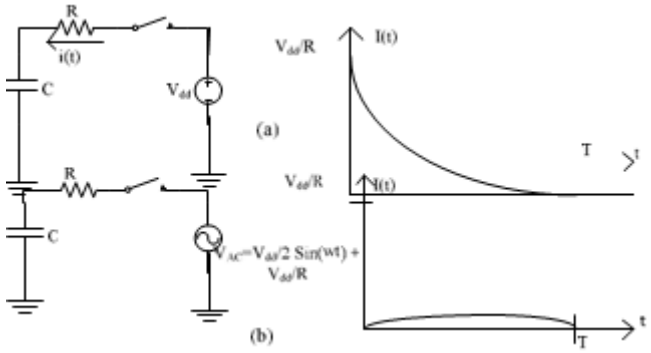

Figure 1: (a) Switching of CMOS (b) Switching of Adiabatic Logic

Adiabatic circuits aims to conserve the charges by following essential rules,

- Avoiding turning on of transistor whenever there is a potential difference across the drain and source (V_{DS}>0).
- Avoiding turning off of Transistor whenever there is a flow of current through drain and source. (I_{DS}~=0).
- The current should not pass through diode.

Adiabatic circuits can have low power dissipation at the cost of complexity of circuits. It reuses the energy stored at the node capacitance instead of discharging.

A. Switching Scheme

For charge to be recovered we use clock with increased transition time such as trapezoidal wave as power supply to decrease the power dissipation.

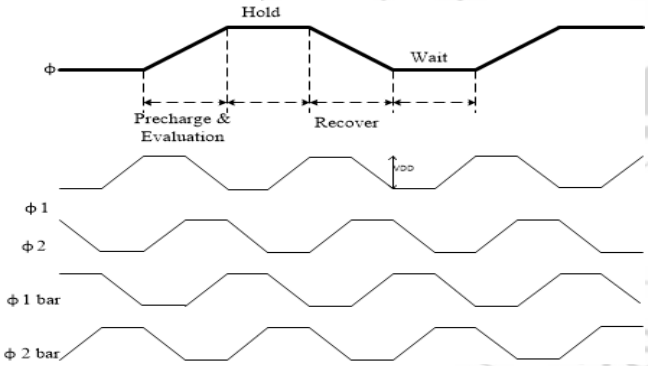

Figure 2: Power supply clock.

Four phases are there in this type of switching scheme, a) Recharge/Evaluation phase

a) Recharge/Evaluation phase
b) Hold phase
c) Recover phase
d) Wait phase

Charging of capacitor is done in pre-charge phase and the logic is evaluated, this logic is kept at hold for next stage. The power is fed back to source in recover phase. The wait phase is used as waiting time to calculate the logic of previous stage. The switching scheme and the cascading of power clock are shown in fig (2).

B. ECRL

Efficient Charge Recovery Logic is one of the useful adiabatic logic families. It is dual-rail logic family based on slandered CMOS family called Differential Cascade Voltage Switch Logic (DCVSL). ECRL logic eliminates the pre-charge diode so the dissipated power decreases. It consist of cross-coupled PMOS loads (P1 and P2), for pre-charge and evaluation as shown in fig 3. The logic in the functional block is realized only with a pair of NMOS Trees in pull-down section. Complete recovery of charges to the power clock is impossible due to the PMOS devices, so this logic is a quasi-adiabatic logic [3].

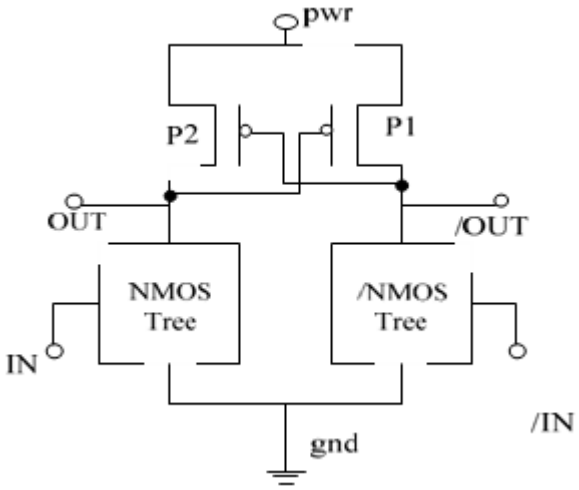

Figure 3: Basic ECRL Adiabatic Logic.

Initially input is in logic high and when power supply clock rises from low to high, output remain at ground due to turning on of P2 and complimentary output follow the power supply clock through P1. When the clock is high, the output holds a valid logic level, which is maintained till hold phase and uses it as inputs for evaluation of next phase. After this when clock goes back to low, complimentary output returns its energy back to clock and delivered energy is recovered. Wait phase is used for clock symmetry and this is used as the preparation phase for Valid logic level to next stage. Due to cross-coupled PMOS devices in both pre-charge and recover phasea full swing can be observed in the output[4]. But the circuit suffers from non-adiabatic losses due to threshold voltage of PMOS transistors.

C. PFAL

Positive Feedback Adiabatic Logic is also a dual-rail adiabatic logic like ECRL as shown in fig. 4. It is based ona pair of cross-coupled inverter consisting of two PMOS (P1 and P2) and NMOS (N1and N2) transistors that avoid degradation in logic level of output. The logic in functional block can be realized only with the pair of NMOS Tree [5].

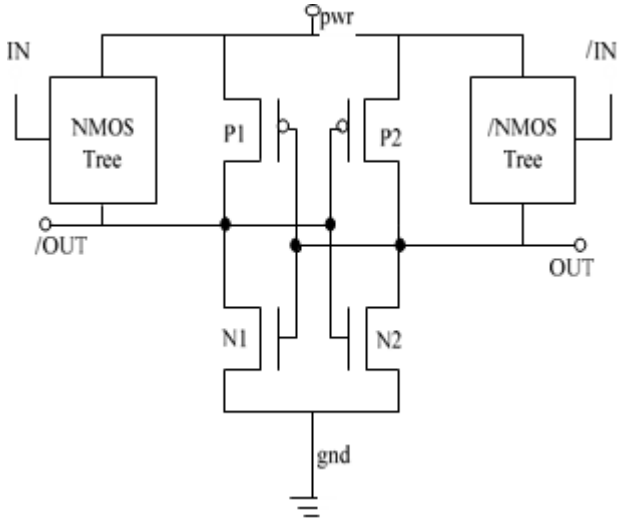

Figure 4: Basic PFAL Adiabatic Logic.

Its operation is similar to ECRL operation. Initially input is given high and when power supply clock rises from low to high NMOS functional tree will work. Output bar follows the clock due to turning on of N2and output at ground. At the time when clock is high, the output holds a valid logic level, which is maintained till hold phase and uses this value as inputs for evaluation for next phase. After this when clock goes back to low, complimentary output returns its energy back to clock and delivered energy is recovered. Wait phase is used for clock symmetry, and this is used as the preparation phase for valid logic level to next stage [5].

4. F2G GATE

Computing reversibility implies that information of computation can never be lost. Reversible logic gate is a n-input and n-output logic device which are having one-to-one mapping. So it can recover any stage by computing backward. This is termed as logical reversibility. It can only gain its benefit after employing physical reversibility, which is practically impossible to achieve [6,7]. The logic function which shows the property of reversibility is "XOR" whereas "XNOR" is also good. The relationship of input A and B and the result of A XOR B, can create a fully reversible gate which is considered as the basic reversible gate known as Feynman gate or Controlled-NOT Gate.

$$P=A,\ Q=A\oplus B,\ A=P,\ B=P\oplus Q \qquad (3)$$

Equation 3 shows the output of Feynman gate, similarly Double Feynman gate can be represented as equation 4.

$$P=A,\ Q=A\oplus B,\ R=A\oplus C$$
$$A=P,\ B=P\oplus Q,\ C=P\oplus R \qquad (4)$$

F2G gate is a reversible gate which is three-input gate, and this gate is useful for duplication of the required outputs. In f2g gate the inputs from 1 to (n-1) are passed to output and n^{th} output is controlled by 1 to (n-1) output. The input and output relation of f2g gate is shown in equation 4. Since the number of inputs are same as number of outputs, there are no loss of bits and therefore reduction in power consumption can be observed [8].

The F2Ggate output can be written as

$$P=A,\ Q=B\oplus \bar{A},\ R=A\oplus C$$
$$A=P,\ B=Q,\ C=(P.Q)\oplus R \qquad (5)$$

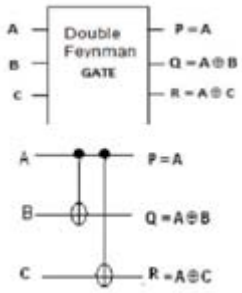

Figure 5: F2G Gate.

Table 1: Truth Table of F2G Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

5. Circuit and Simulation

All circuits are designed on cadence ICE6.1.5 virtuoso EDA design environment using 180nm transistor model. The proposed circuit of f2g gate consist of one buffer, two XOR gate. In figure 6, the circuit is implemented using dual rail adiabatic logic ECRL. The source of cross coupled PMOS is connected to power supply and drain is connected to NMOS logic functions. In figure 7, the circuit is implemented using dual rail adiabatic logic PFAL. Two cross coupled inverters are used to avoid degradation of logic level and the logic function is realized using NMOS transistors.

Single power supply of ramp function of voltage 1.8V is used for two buffer circuits to get the output A and B. Two different ramp function of voltage 1.8V having a phase difference of 90^0, is used as power supply for AND gate and XOR gate. So the evaluated values of previous stage hold for the next stage of operation to get correct outputs. The buffer circuits also give inverted output, so the compliment of A and B can also be calculated. As per the equation 5, the output P and Q are the outputs of buffers. To get the output R of f2g gate it requires to cascade AND gate and XOR gate. The output R of f2g gate is XOR of AB and C.

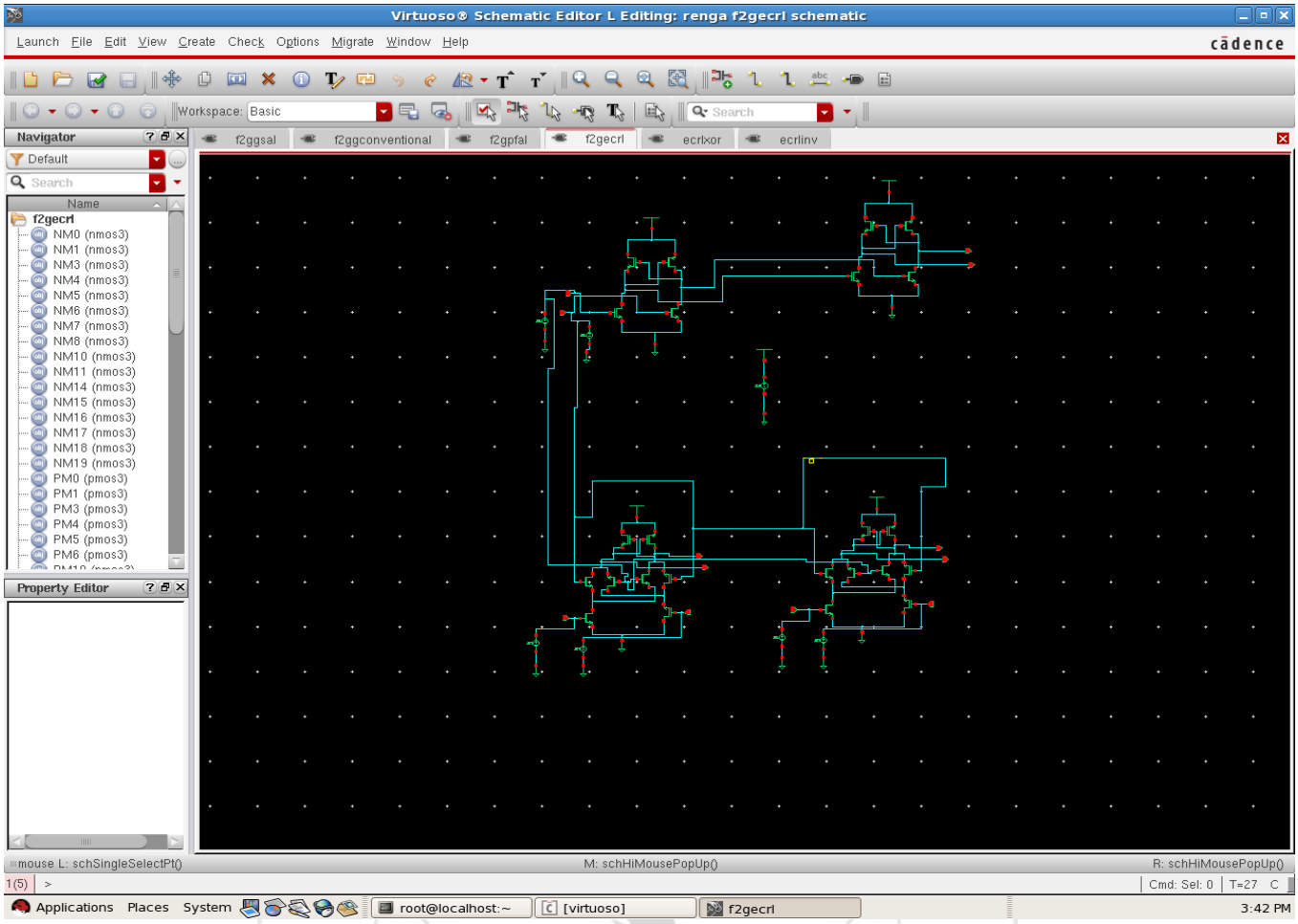

Figure 6: F2G Gate using ECRL

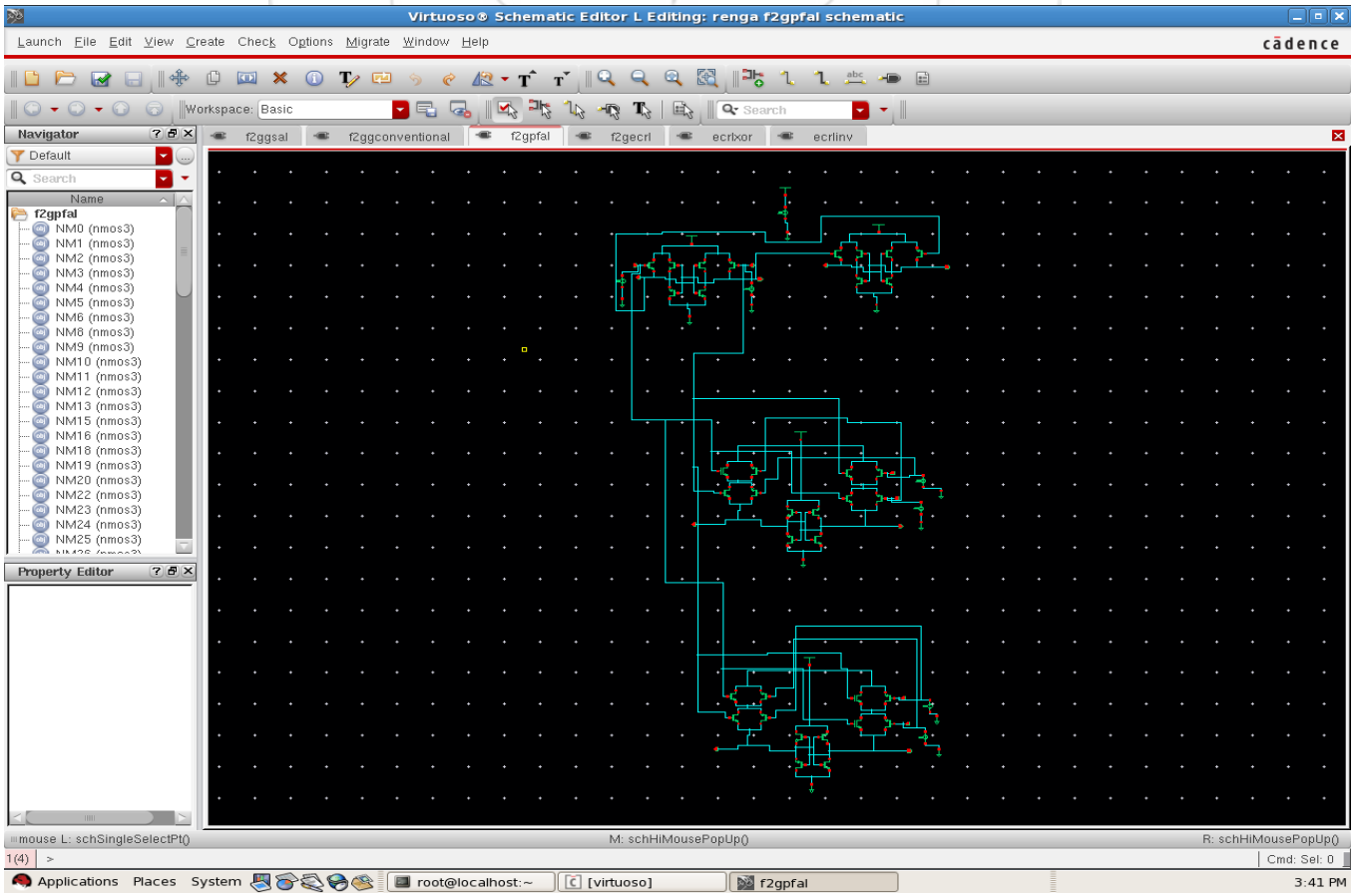

Figure 7: F2G Gate using PFAL

6. Results and Conclusion

The F2G gates are implemented on Cadence UMC 180nm technology for both PFAL and ECRL. Simulation has been done for all possible inputs and observed the output voltage swing, power consumed by the circuits, delay in output, number of transistors used and maximum operating frequency. Two values of load capacitor $4f$ F only used taken here to stabilize the output and tabulated below.

Table 2: Average Power Consumption at 4F F

Average Power Consumed		
Frequency (MHz)	*ECRL (µw)*	*PFAL (µw)*
5Mhz	11.6	12.8
10Mhz	15.8	18.5
20Mhz	18.3	24.9
25Mhz	20.7	32.7
50Mhz	27.2	36.4

In this paper, it has been shown that PFAL takes more power than ECRL at low frequency and lower value of load F2G gate is 22 for ECRL whereas it is 32 for PFAL. With capacitance. The delay is more in PFAL than ECRL reference to number of transistor count ECRL is better in any case. Number of transistor used in ECRL is less than PFAL which implies ECRL consume less area. This reversible gate can be used in the application where requirement is less such as both area and power nanotechnology, optical computing devices, quantum computers etc.

References

[1] B Dilli kumar & M Bharathi "Design of Energy Efficient Airthmetic Using Charge Recovery Adiabatic Logic" International Journal of Engineering Trends and Technology- (IJETT) volume4,Issue ,pp.31-40,apr2015.

[2] Prashant R. Yelekar, Sujata S. Chiwande, "Introduction to Reversible logic Gates & its Application",2National Conference on Information and Communication Technology (NCICT), pp. 5-9, November,11.

[3] K.W.Ng and K.T.Lau, "ECRL Based low Power Flip-Flop Design," Microelectronics Journal, Volume 31, Issue 5, pp. 365-370, May, 2000.

[4] Youg Moon and Deog-Kyoon Jeong, "An Efficient Charge Recovery Logic circuit", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Volume31, Issue 4, pp. 514-522, April, 1996.

[5] Arun Kumar and Manoj Sharma "Design and analysis of MUX using Adiabatic technique ECRL and PFAL", IEEE International Confrence on Advances in Computing, Communications and Informatics (ICACCI), pp. 1341-1345, 22-25 August, 2013.

[6] J. Willingham and izzet Kale "Using Positive Feedback Adiabatic Logic to implement Reversible Toffoli Gates", IEEE Nordic Microelectronics Events (NORCHIP 2008), pp. 5-8, 16-17 November 2008.

[7] Himanshu Thapliyal and Nagarajan Ranganathan, "A New Design of the Reversible Subtractor Circuit," 2011 11th IEEE Confrence on Nanotechnogy (IEEE-NANO), Portland, Oregon, USA, pp. 1430-1435, 15-18 August, 2011,