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Low Area, Low Power and Wide Bandwidth Operational Amplifier by 130nm CMOS Technology

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Abstract: ***A high performance two-stage Operational Amplifier is presented in this paper having the specifications of less Area and wide bandwidth which is operated on low power i.e. 1.3V supply. Miller capacitor with resistor is used for compensation which also significantly improves the bandwidth. Design of Operational Amplifier is demonstrated with only CMOS transistors. The Amplifier exhibits a gain of 59 dB, 1.25 MHz 3dB bandwidth, 605 MHz Unity gain bandwidth, 269 dB CMRR, 106 dB PSRR, 1.6 V/µs Slew rate with the power dissipation of 0.43 mW.***

Keywords: Op-amp; low power; less area; two-stage; CMRR.

1. Introduction

The Mixed signal applications increased with ICs contains digital and analog parts, along with technology scaling motivates for development of a device which can be used for both. Operational Amplifier (commonly referred as Op-amp) attracts our own side for this type of design. It is the basic element of many analog integrated circuit designs beyond to this it uses vastly different levels of complexity to comprehend functions ranging from dc bias generation to high speed amplification or filtering. It is not only limited for amplifying the signals but it can perform large number of operation also such as mathematical operation, A/D and D/A conversion, clipping, clamping, zero-crossing detection, pulse generatoretc. In the era of advance technology researchers move to work with low power supplywhich is very useful for portable devices such as laptops, tablets, mobiles, pacemaker etc. so that it can operate with low supply as well as power dissipation is can be easily managed which is the major issue for designing any system. High speed device required for fast processing applications, considering this parameter a method is proposed for obtaining high bandwidth in this research work. Miller compensation with resistor is used for maintaining stability for this Op-amp.In this technique a resistor is connected in series with capacitor. This resistor and capacitor takes large die area but in the today's technology the demand of low area for high chip density. In this work both these components are replaced with MOS transistors which takes very small area compared to this.Along with this current source is used in the conventional Op-amp to maintain transistors in proper region. This is also to be designed with MOS transistors. So finally in this research work less area, low power and wide bandwidth Op-amp is presented.

2. Used Compensation Technique

For designing any analog circuit compensation is required for maintaining stability. In this proposed Op-amp miller compensation with resistor is used for maintaining stability. This is also to be referred as nulling resistor compensation technique. In this technique a resistor is connected in series with miller capacitor across the second stage which provides more stability compared to miller compensation technique. This technique also improves the 3dB bandwidth. The configuration of this technique is shown below.

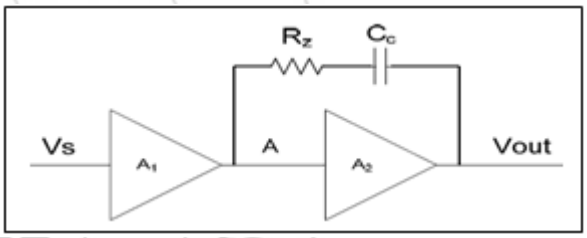

Figure 1: Nulling resistor compensation

As in the previous Op-amp miller compensation technique is used which splits the pole i.e. dominant pole which is nearest to origin and non-dominant pole which is far away from origin. As well as it generates the RHP zero which affects the stability. This RHP zero is generating due to feedforward current flow in the feedforward path. This feedforward path is created due to the direct connection of the output stage to internal stage. The location of poles in miller compensation is given as

$$P_1 = \frac{1}{R_1 C_1} \quad (1)$$

and

$$P_2 = \frac{1}{R_2 C_2} \quad (2)$$

Where R_1,C_1 and R_2,C_2 are the resistor and capacitor of stages A_1 and A_2 respectively. The RHP zero location which is generated during miller compensation is given by

$$Z_1 = \frac{g_{m2}}{C_C} \quad (3)$$

This zero is to be shifted from RHP to LHP for maintaining stability by employing nulling resistor compensation. The resistor used in the proposed techniquehelps to move this zero from one plane to another plane. The location of poles in this technique is same as the miller compensation however this technique also generates one another pole which is very far away from origin and not taken into consideration.

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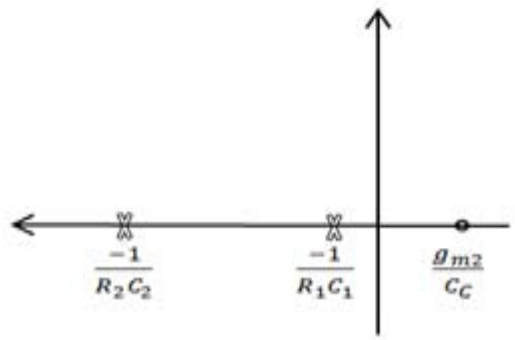

Figure 2: Location of poles and zeros

The new location of zero after employing this technique is given as

$$Z_1 = \frac{1}{(\frac{1}{g_{m2}} - R_z)C_C} \quad (4)$$

Where

R_z= Nulling resistor

The zero moves to infinity for the value of $R_z = \frac{1}{g_{m2}}$ and for $R_z > \frac{1}{g_{m2}}$ the zero moves from RHP to LHP and maintains the stability. This technique also improves the 3dB bandwidth. The bandwidth is the reciprocal of the product of the resistor and capacitor if this resistor value is decreased the bandwidth improves.

The schematic design of Op-amp is shown in below figure which is designed by using six PMOS and five NMOS transistors including miller capacitor and resistor. In the proposed Op-amp this capacitor and resistor is designed with MOS transistor which reduces area. The transistor M_{11} behaves as a capacitor whereas transistor M_{10} is act as a resistor. For operating transistor M_{10} as a resistor, it is operated in triode region. In Op-amp current source used for

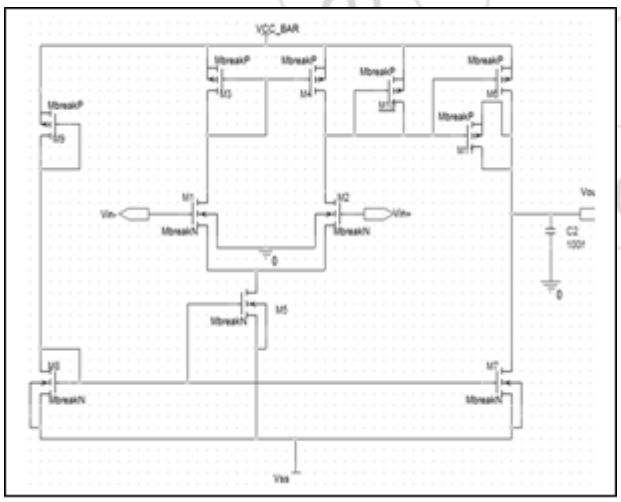

Figure 3: Design of Op-amp

maintain the transistors in particular region, which is also designed with MOS transistor. The design of Op-amp includes two basic part i.e. differential amplifier and gain stage. In this Op-amp the differential amplifier which is also referred as "Heart of Op-amp" includes transistors from M_1 to M_5. This amplifier includes current-mirrorconfiguration, input transistor pair and a current source at the bottom which is generally replaced with NMOS transistor. Each part is responsible for various parameters of Op-amp. The current-mirror configuration is responsible for high Input common mode range and act as a load for input stage. This first stage also provides important parameters such as Power supply rejection ratio (PSRR), Common mode rejection ratio (CMRR), high input impedance and low output impedance. The Gain-bandwidth product is depended upon input transistor pair and slew rate is given by transistor M_5. A second stage is used to improve the gain of first stage which also converts the differential input to single ended output. In the second stage, transistor M_6 act as a load and provide maximum output voltage swing whereas minimum output voltage swing is provided by transistor M_7. The gain of the first stage and second stage is given as

$$A_V = A_1 A_2 \quad (5)$$

where

$$A_1 = g_{m1} R_1 \quad (6)$$

$$\text{and } A_2 = g_{m2} R_2 \quad (7)$$

where g_{m1} and g_{m2} is the transconductance of stage A_1 and A_2 and R_1 and R_2 is given as

$$R_1 = r_{ds2} || r_{ds4} \quad (8)$$

$$\text{and } R_2 = r_{ds6} || r_{ds7} \quad (9)$$

where

r_{ds} = Drain to Source resistance of transistor

3. Op-Amp Design Issue

1) The proposed Op-amp uses Dual input single ended output differential amplifier which directly provide input to second stage. This is also referred as Dual input unbalanced output differential amplifier.
2) A load capacitance of 100f F is used for obtaining output with the compensation capacitor of 50f F, which is obtained from the expression
$$C_C \geq 0.22 C_L \quad (10)$$
From this value of load capacitance, C_C is given as
$$C_C \geq 22fF \quad (11)$$
So for this Op-amp choose the 50fF compensation capacitor which is suitable for obtaining this output.
3) Due to highly demand for low power devices for many applications this Op-amp is work with low power i.e. 1.3V supply voltage. Hence there is no any issue of large power dissipation also used Vss of -1.3V.
4) Overall design is simulated with only MOS transistors to reduce the area.
5) Aspect ratios of each transistor are calculated and put this value with slightly changes to obtain better response.
6) Sinusoidal input is applied at both input terminal i.e. inverting and non-inverting having magnitude of 0.5V of opposite phase.
7) Op-amp parameters such as CMRR, PSRR, Slew rate, DC offset, Settling time etc. are also calculated. CMRR which is the ratio of differential mode gain to common mode gain achieve higher value due to the low value of the common mode gain.

4. Results and Discussion

For simulation of this Op-amp PSpice EDA tool is used with 130nm digital CMOS technology. BSIMv3.0 is used as a model library. Comparative table on previous work is shown

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in TABLE I whereas TABLE II represents simulated results of this work.

Table 1: Comparative Table of Previous Work

Parameter	[1]	[2]	[3]	[4]	[5]	[6]
Power Supply(V)	1.8	1.8	3	5	2.5	3.5
Gain (dB)	65	58.1	49	77	36.74	48
f_{3dB} BW (MHz)	-	0.25	-	0.0013	7.33	-
UGB (MHz)	2300	205	2020	14	16.54	40
CMRR (dB)	96	-	39	80.9	133.6	-
PSRR (dB)	62	-	154	-	179.3	-
Slew rate (V/µs)	450	-	1.41	10.3	12.5	-
DC Offset (µW)	2%	-	-	-	-	-
Powerdiss. (mW)	25	-	0.039	-	0.804	-
Area (mm^2)	0.04	-	-	-	-	-
Phase Margin	-	84°	60°	53.4	48.1°	49.8°
Technology (nm)	180	500	180	350	180	180

Table 2: Simulation Result Of Proposed Op-amp

Parameter	Obtained Value
Power Supply	1.3 V
Gain	59 dB
f_{3dB} Bandwidth	1.25 MHz
Unity Gain Bandwidth	605 MHz
CMRR	269 dB
PSRR	106 dB
Slew rate	1.6 V/µs
DC Offset	121 mV
Power dissipation	0.43 mW
Area	125 μm^2
Technology	130 nm
Phase margin	54°
Settling time	1.46 µs
Output Resistance	15.7 Ω

Frequency response of this Op-amp is shown in fig. 4 where magnitude is in dB and frequency is in logarithmic plot as well as bode plot is shown in fig. 5. The bode plot shows 59 dB gain is obtained for this Op-amp as well as phase margin of 54°is achieved.

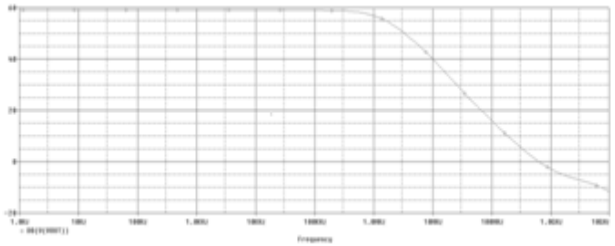

Figure 4: Frequency response of Op-amp

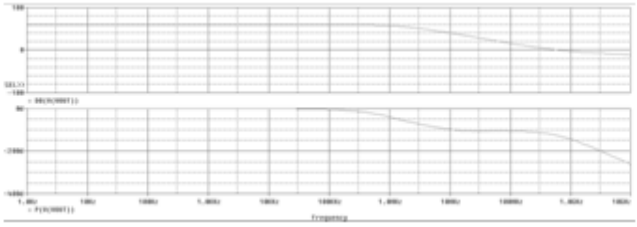

Figure 5: Bode Plot of Op-amp

5. Acknowledgment

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