

Low Voltage and High Gain Bandwidth Constant Current Source using 90nm CMOS Technology

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Abstract: Current source circuit is found as one of the basic element in designing of analog integrated and mixed mode circuits. In this paper a current source with low input impedance, high output impedance, and high gain is proposed. This current source circuit is designed by using seven n-type and four p-type MOSFETs. Simulation process of the proposed circuit is performed using 90nm CMOS technology. Input impedance, output impedance and accuracy are the most important parameters to observe the performance of the Current Source. The proposed current source circuit is operated at the supply voltage of 0.8V.

Keywords: Constant Current Source; CMOS; Low voltage

1. Introduction

As the need for portable and wireless devices is increasing the designers are now more focused towards circuits with low power consumption and enhanced bandwidth. We require low voltage current source for low voltage applications. Area minimization is also an important task to perform in order to achieve reduction in the size of silicon chip. Recently supply voltage and threshold voltage requirements are diminishing very speedily. Low voltage application refers to the low input and output voltage as well as low supply voltage requirements. Constant current can be used to generate a constant current which is independent of the voltage across it. It is necessary to create chips of small size, using low power and lesser area consumption to move with the rapid developments. Constant current source can be used to generate a constant current which is independent of the voltage across it. The preceding sections include contents are as follows: literature review, proposed current source, result of the proposed circuit and conclusion respectively.

2. Literature Review

Some current mirror circuits have been reported in [1-4]. Kuo-Hsing Cheng [1] proposed a current mirror whose performance better than a regulated cascode current mirror. It uses a reference current of 160 μ A. Manish Tikyani [2] has proposed a current mirror using four p-type and five n-type MOSFET. This circuit is designed with supply voltage of 1.3V. Houda bdiri gabbouj [3] has been proposed a low voltage current mirror which provides low input impedance high output impedance with high performance. A. Torralba [4]

has proposed a low voltage high performance current mirror using CMOS technology which provides bandwidth in the range of hundreds MHz. J. Ramirez-Angulo [5] has proposed a Low supply voltage high performance CMOS current mirror with low input and output voltage requirements" which is designed with 0.15V input and output voltage requirements, 40MHz bandwidth, 100 Ω input resistance and 200M Ω output resistance.

3. Proposed Current Source

Constant current source is a power source which provides a constant current for a load even if the load resistance value is changed. For low voltage application it is mandatory to use the

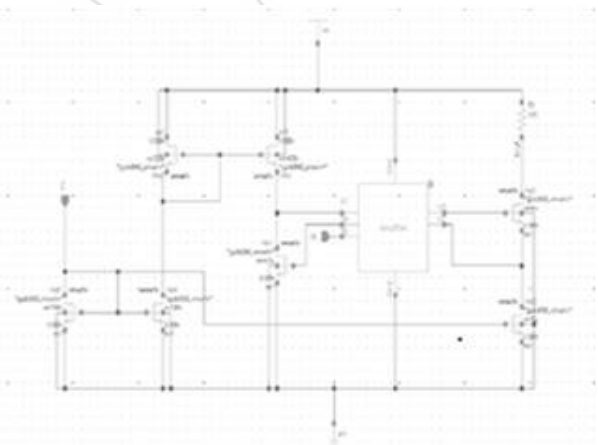


Figure 1: Low voltage constant current source

low voltage current source. Current source can be used in biasing and loading of a circuit. Regulated cascode current mirror provides approximately equal currents in input and output stages. At output stage cascading of transistors is performed to achieve enhanced output impedance. Higher output impedance is achieved by using regulated cascode current mirror as compared to Wilson current mirror. This circuit is advantageous because it doesn't require any bias current at the input side. A stable current is achieved at the output of this circuit. In the proposed circuit negative feedback is provided used to stabilize the output current. Transistor MN2 is biased by the transistors MN0 and MN4. For biasing of PM0 we use transistor PM1. Thus we can say that the circuit is self-biased i.e. no external biasing voltage or current is applied to the regulated cascode current mirror. Self-biasing is done because if input current is too large then the device may get short circuited. Input impedance of this circuit is given as

$$R_{in} = r_0 \quad (1)$$

Output impedance of the circuit is given by

$$R_{out} = \frac{g_m r_0^3}{2} \quad (2)$$

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An Amplifier circuit is used at the output to enhance the gain of the current source. Settling time of a current source proves significant parameter to enhance the performance of the current source circuit. For high speed applications the settling time of the circuit should be as low as possible. The proposed circuit should also be able to operate at the high frequencies.

4. Full Balanced Pseudo Amplifier

An amplifier is used at output side in order to amplify the difference between the drain source voltages of two transistors. It is also referred as full balanced pseudo amplifier. This amplifier is made by using two NMOS transistors and two PMOS transistors. Both the NMOS transistors are operated in saturation region in order to provide equal drain source voltages for input and output mirror transistor. For both the NMOS transistors to operate in saturation region a biasing voltage is provided to the gates of respective transistors. Both the PMOS transistors are also operated in the saturation region in to get amplification at the output of the circuit. This amplifier uses less number of transistors than a conventional differential amplifier.

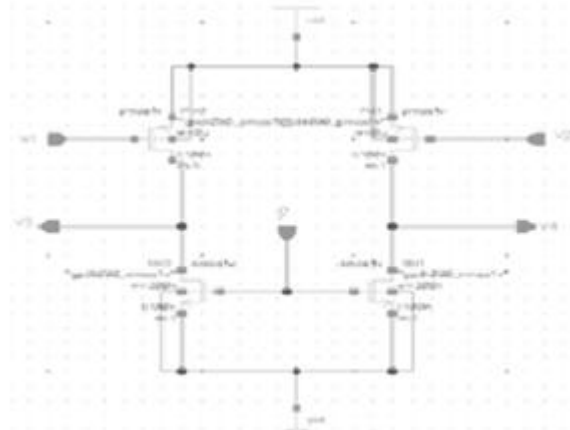


Figure 2: Pseudo Amplifier

In conventional differential amplifier a high voltage drop is available across the tail current source. Therefore to avoid the voltage drop across the tail current source fully balanced pseudo amplifier is used.

5. Transistor Sizes

The aspect ratio of transistor used for designing the constant current source is given in TABLE I.

Table 1: Transistor sizes and component values

Transistor	W/L ratio
MN0	180n/100n
MN1	4.5u/100n
MN2	6u/100n
MN3	5u/100n
MN4	120n/100n
MN5	120n/100n
MN6	450n/100n
PM0	120n/100n
PM1	120n/100n
PM2	8u/100n
PM3	8u/100n

6. Result and Discussion

The simulated result of proposed constant current source is given below. A low voltage current source circuit has been designed and simulated using Cadence EDA tool. Threshold voltages for NMOS and PMOS are 0.169V and 0.135 respectively. A load resistor of 1kΩ with the supply voltage of 0.8v is used for simulation. Transistor sizes of the proposed current source are reduced for reduction in silicon chip area of the circuit. A dc sweep of the input current is performed for a range of 0u to 100u. Power consumption of the circuit is reduced. All the results are obtained at the room temperature i.e. 27°C.

Table 2: Simulated Results

Parameter	Value
Supply voltage	0.8 V
Input current	50 μA
Bandwidth	40MHz
Gain	47.7dB

The dc sweep plot of this work is shown below.



Figure 3: dc sweep plot

7. Conclusion

A low voltage high performance constant current source has been designed using CMOS 90nm technology. Cadence virtuoso EDA tool is used for simulation of the proposed current source. This proposed current source circuit is very efficient in terms of area, power consumption and speed.

8. Acknowledgment

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