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A Brief Review on Soft Errors and LDPC Codes

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Abstract: ***In current scenario, due to high demand of technology scaling and higher integration density, the designers are using nanodevices for computer system and other memory system. Despite having many advantages such as lower area overhead and lower power consumption, these devices has major disadvantage that they are more prone to soft errors. Due to this reason the reliability of these systems are severely affected. Many error detection and correction codes have been studied to reduce this error. There are vast classes of such codes; some of them are hamming codes, turbo codes, BCH codes and LDPC codes. But among these codes LDPC codes achieve better performance and lower decoding complexity. LDPC codes were originally discovered by Robert G. Gallager. But after the rediscovery of LDPC codes by Mackay and Neal in 1995 interest on LDPC codes increases because of its bit error performance approaches asymptotically the Shannon limit. An LDPC code is a special class of linear block codes whose parity-check matrix H has low density of one's i.e. sparse. Due to this sparsity in LDPC codes there is low complexity decoding and its implementation is also simple. Also LDPC codes provides large degree of parallelism that can be exploited in the decoder and in LDPC codes information block length are long enough. In addition LDPC codes provides wide range of trade-offs between performance and complexity. LDPC codes find its application in many areas such as satellite transmission of digital television. LDPC codes are also used for 10GBase-T Ethernet that transmits data at 10 gigabits per second over twisted pair cable***.

Keywords: LDPC, EG-LDPC, FSD, BER, MBU

1. Introduction

To meet the insatiate demands of consumer's for higher density, functionality and lower power, the operating voltages and dimensions of electronic devices used in computers and other electronic memory systems are reduced. Due to these reasons the sensitivity to radiation of these devices has been increased dramatically. The excess of radiation may cause from data disruptions to permanent damage ranging parametric shifts to complete device failure. Due to this reason the reliability of these systems are severely affected. One of the major effects is the "soft" single event effects (SEE). The name single event effects imply that device failure caused by single radiation event. The energetic ions generated by radiation on the nanodevices, are responsible for the generation of soft errors. There are many sources of ionizing particles such as, Alpha particles emission from thorium impurity and trance uranium in packaging material, Cosmic ray events and ionizing particles in electronic devices radiated from the interaction of low-energy cosmic ray boron and neutron. To mitigate the soft error designer should to get rid of radiation sources. Semiconductor manufacturer are using high purity processes and materials, production screening of all material with low background alpha emission material to reduce emission of alpha particles. Manufacturer also attached additional capacitance to all sensitive nodes for increasing Q_{crit} of logic devices and SRAM [1]. Another approach is to use multiple storage nodes and transistors for each data bit stored within the device. But most effective way to deal with soft error in memory application is using additional circuits for error detection and correction.

Many error detection and correction codes have been studied to reduce this error. There are vast classes of such codes; some of them are hamming codes, turbo codes, BCH codes and LDPC codes. But among these codes LDPC codes achieve better performance and lower decoding complexity. LDPC codes were originally discovered by Robert G. Gallager. But after the rediscovery of LDPC codes by Mackay and Neal in 1995 interest on LDPC codes increases because of its bit error performance approaches asymptotically the Shannon limit. An LDPC code is a special class of linear block codes whose parity-check matrix ***H*** has low density of one's i.e. sparse. Due to this sparsity in LDPC codes there is low complexity decoding and its implementation is also simple. Also LDPC codes provides large degree of parallelism that can be exploited in the decoder and in LDPC codes information block length are long enough. In addition LDPC codes provides wide range of trade-offs between performance and complexity.

A sub class of the LDPC code is Euclidean geometry low density parity check code. This code has properties of both LDPC codes and Finite geometry codes. The main advantage of EG-LDPC code is that it is a one step majority logic decodable code [6], which enables the designer to design the decoder with reduced complexity. This paper represents a brief survey on the soft errors, the LDPC codes and EG-LDPC codes. Section 2 represents the literature review on soft errors and LDPC codes. Section 3 represents the summary of this paper.

2. Literature Survey

Robert C Baumann explains the details of soft errors and their causes and their mitigation options [1]. The operating voltages and dimensions of electronic devices used in computers and other electronic memory systems are reduced to meet the insatiate demands of consumer's for higher density, functionality and lower power. Due to these reasons the sensitivity to radiation of these devices are increased dramatically. The excess of radiation may cause from data disruptions to permanent damage ranging parametric shifts to

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complete device failure. One of the major effects is the "soft" single event effects (SEE). The name single event effects imply that device failure caused by single radiation event. When the data state of flip-flop, latch, and register or memory cell are reversed or flipped due to the charge disturbances caused by radiation event, then the soft error occurs. This error is known as soft error because in this event the radiation does not damage the circuit permanently, when we write a new data on that particular bit, the device stores it correctly. Such type of error, soft error, is also known as single event upset (SEU). When the energy of radiation event is high then more than one bit may be affected, these creates a multi-bit upset (MBU).

The energetic ions generated by radiation are responsible for the generation of soft errors, i.e. disturbances and its magnitude depends on the ion's linear energy transfer (LET). The energy and mass of the particle and the material in which ion is travelling decides the LET. Higher LET appears in more energetic and massive particle in denser materials. Due to this movement of ions, charges are collected at junction of semiconductor devices, which occurs within a few microns of the junction and depends on types of ion, its trajectory and its energy over the path near or through the junction.

When the radiation event occurs, then energetic ions generated and due to which, a cylindrical track of electron hole pair having submicron radius and very high carrier concentration is formed. The whole process can be explained as: When the resultant ionization track lying across or approaches the depletion region carriers are collected rapidly by the electric field resulting in a large voltage/current transient at that node. Due to this event there is a concurrent disruption of the potential into funnel shape. This funnel by the extension of high field depletion region dipper into the substrate enhances the efficiency of the drift collection. The funnel size is substrate doping function, i.e. the distortion increases when substrate doping decreases. Additional charge is accumulated by electron diffusion into depletion region for long time, until all excess carriers have been collected, recombined or diffused away from the junction area. When this event occurs away from the junction, smaller amount of charge will be collected and chance of occurrence of soft error reduced.

The magnitude of collected charge ($\boldsymbol{Q_{coll}}$) depends on factors such as substrate structure, size of the devices, device doping, biasing of various circuit nodes, type of ions, and its trajectory, and its energy, state of the device and initial position of the event with the device. The device sensitivity not only depends on the collected charge ($\boldsymbol{Q_{coll}}$) but also on critical charge ($\boldsymbol{Q_{crit}}$) is defined by operating voltage, node capacitance and strength of feedback transistor. In simple isolated junction, soft error occurs if a radiation event appears close enough to a sensitive node, i.e. when $\boldsymbol{Q_{coll}} > \boldsymbol{Q_{crit}}$ otherwise soft error will not occur.

Michael A. Bajura et al.; represented the hardening approach to reduce the soft error rates [2]. Two approach of hardening is given which are critical circuit based hardening and system based hardening. In first method, both the memory array's control structure designs and individual memory cell are hardened by layout circuit radiation hardening by design (RHBD) technique or custom radiation hardened by foundry processes. In the circuit based hardening approach the BER of the SRAM is approximated by the individual or physical BER of memory cell and system design. The power, speed and area requirements are more in this approach. But due to process generating scaling the technological gains are as expected.

In second approach of hardening, the periodic scrubbing of memory, i.e. periodic memory error checking and error correcting codes (ECCs) are used to enhance the effective bit error rate of a system over its physical bit error rate. This method requires a proper balance between scrubbing rate SEU-induced mechanisms, physical cell BERs and ECC redundancy that can increase the usage of power. He also suggested an advanced method that is a hybrid design, which hardens only the control circuits of the memory array by use of RHBD circuit and layout techniques and ECC. These approach intact the technological scaling, the commercial density and intrinsic physical BER of memory cell. The bit interleaving, ECCs and memory scrubbing are used in this approach to lower the overall effective BER with no use of custom radiation hardened foundry process.

Shalini Ghosh and Patrick D. Lincoln proposed a method to sort out the issue of soft errors [3]. In that paper, a special variant of low density parity check codes (LDPCs), which is Euclidean geometry low density parity check (EG-LDPC) codes is proposed. The EG-LDPC codes are capable of correcting the soft errors dynamically. Sparsity is one of the properties of EG-LDPC codes which enable the dynamic adjustment of the error correcting capacity to improve the system performance.

The error correcting system uses for nanodevices must have following properties:

a) To handle the high soft error rates, the error correcting system should have high error detection and correction capability.
b) To synthesize the encoder and decoder by using simple modular hardware, they should have sparse modularity.
c) To make balance between system performances and error correction, they must have dynamic error correcting capabilities, when there is a variable fault rate.

In Euclidean geometry LDPC codes $\boldsymbol{H}$ matrix can be interpreted as incidence matrix in a finite geometrical space spanned by m-tuples over $\boldsymbol{GF\ (2^s)}$. This code is one step majority logic decodable code, so there is no need of complex iterative decoder. EG-LDPC code enables us to correct the errors dynamically, because their parity check matrix and encoder have regular modular structure. This modularity is possible in EG-LDPC codes because EG-LDPC codes are sparse in nature.

Shalini Gosh and Patrick D Lincoln also presented that it is possible to correct errors online by using EG-LDPC codes [4]. Due to systematic structure of type-I EG-LDPC code and modular structure of parity check matrix of type-II EG-LDPC codes, dynamic error correction is possible. Also the

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implementation of EG-LDPC decoder using nanoscale hardware is easy because of sparseness in EG-LDPC codes. They give the details of properties of LDPC and EG-LDPC codes. A finite Euclidean geometry has following advantages:

a) The structure $EG(m, 2^s)$ makes it easier to construct H matrices of LDPC. This structure facilitates the designer to design H matrix efficiently for any memory size by using GF operation.
b) Due to regular structure of EG-LDPC codes, it is not necessary to use iterative decoding because in this case the LDPC codes are multistep majority logic decodable. This property makes the decoding fast.

They also suggested that by using ML decoding, the number of errors e can be corrected when $e < \gamma/2$, where γ is the number of syndrome equations. But if $e > \gamma$, then this ML decoding algorithm fails. To handle this situation another improved approach of ML decoding is used which uses the bit flipping algorithm. The bit flipping algorithm uses simple comparison, sum and majority operations and is therefore easier to implement using nano-PLA.

Helia Naeimi and Andre Dehon introduced the reliable memory system that can tolerate multiple transient errors in the memory words as well as transient errors in the encoder and decoder (corrector) circuitry [5]. They suggested a fault secure detector (FSD) error correcting codes (ECC), which can be used for any ECC. They introduced FSD-LDPC code. FESD-LDPC code can tolerate up to 33 errors in each memory word or supporting logic that requires only 30% area overhead for memory blocks of 10kbits or larger, so the larger codes can achieve higher reliability and lower area overhead [5].

There are many codes like Hamming codes that can be used to protect memory systems against transient upset of data bits, but the problem with these codes is that they only corrects the errors in the memory word. They cannot correct the errors in the encoder, decoder and other supporting logics. These supporting logic devices are not immune to soft errors. So there is a need of an error correcting code that can secure this supporting logic also from the transient faults. So they proposed such a system. They used Euclidean geometry and projective geometry codes to design fault secure detector. These codes have following properties:

a) For memory application the required encoder and decoder have low latency.
b) By using these codes, it is possible to design a fault secure detector, which allows fault tolerant in supporting logic of memory system.

In there suggested system the fault secure detector unit checks the output of the encoder and the corrector circuitry and if there is any error in the output of either of this unit, that unit has to redo the operation to generate the correct output vector [5]. By using such an operation known as detect –and –repeat, it is possible to correct transient errors in supporting logic circuitry such as encoder and decoder.

If e_m, e_e and e_c is the number of errors in the memory, encoder and the corrector, and, if $e_m \leq E$ and $e_e = e_c = 0$, then error correction is possible in the existing system. But the author guarantees that the system can correct error combination as long as $e_m \leq E$, $e_e + e_{de} \leq D$ and $e_m + e_c + e_{dc} \leq D$, where e_{de} and e_{dc} are the number of errors in two separate detectors , monitoring, the encoder and corrector unit and D and E are maximum number of error bits that the code can detect and correct.

Based on the hyper plane of the two different dimensions in the finite geometries, *Heng Tang et al.;* presented a new approach for construction of codes, which results in three classes of low density parity check codes and a class of multistep majority logic decodable codes [6]. LDPC codes, when decodes iteratively, gives near Shannon's limit performance. Also there is another class of codes known as finite geometry codes. Finite geometry code has good minimum distance and its decoding is simple when decoded with majority logic. Finite geometry codes are constructed based on geometries over finite field [6]. By using the properties of both codes, LDPC and finite geometry codes, another class of code was discovered known as finite geometry LDPC code. The construction of finite geometry LDPC code is based on points and lines of finite geometries. The tanner graph of finite geometry codes is free of cycles of length 4 and also they have good minimum distance. Because of these properties, finite geometry codes give good performance with iterative decoding using the sum product algorithm (SPA) and perform close to Shannon's limit. In these codes the constructions of codes are done algebraically, also these codes are either cyclic or quasi cyclic [6]. Due to these reason the encoder of finite geometry LDPC codes can be implemented by feedback shift register in linear time. This codes can also decoded by majority logic decoding and gives high error performance, fast decoding and reduced decoding complexity.

Shi-Fu Liu et al.; presented a method for error detection for difference set cyclic code with majority logic decoding [7]. Majority logic decodable codes have capability to correct a large number of errors, so they are suitable for memory applications. But the problem with this code is that time required for decoding is large. They also suggested a method to reduce this decoding time, if there is no error in data read. In plain majority logic decoding the entire codeword bits is cyclically shifted to check the errors. If there is error in any of the codeword bit then that will be corrected by the corrector circuit. In their proposed technique all the codeword bits are cyclically shifted for correction of errors. If the size of the codeword will be small then there will not be any issue. But if the size of the codeword is large then time taken will be large in shifting all the codeword bits cyclically, for the detection and correction of errors. So they suggested a new approach to reduce this time. According to them if most word bits are error free, then we can stop decoding after three iterations. If no error was found in the first three iterations, then the decoding can be stopped. There is no need to check the remaining bits. But if error occurs in this three iterations, then corrector circuit corrects that error. So in this way the memory access time greatly reduced.

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3. Summary

The survey on the soft errors and LDPC codes conclude that LDPC codes are one of the best codes for mitigation of soft errors. LDPC codes are sparse in nature this property of the LDPC code enable the designer to design the encoder simple for construction. One of the major advantages of using LDPC codes is that it is one step majority logic decodable code. Due to this property decoder can be constructed by using simple circuitry. But due to iterative decoding it takes large time to decode. Future work includes the reduction in the decoding time.

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