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A Trench Gate Power MOSFET with Reduced Gate Charge - A Review

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Abstract: ***In this paper we have written the review of the work done by Ying Wang, Yan-Juan Liu, Cheng-Hao Yu, and Fei Cao in simulating a novel trench gate power MOSFET with reduced gate charge. They worked with a 2-dimensional device simulator named ATLAS and simulated their MOSFET to obtain input, output and transfer characteristics. It is found that the gate charge is reduced by 49.5% without increasing the value of R_{on}. This is done so as to increase the switching speed of the device.***

Keywords: Gate Charge, Switching Speed, R_{on}

1. Introduction

A Trench MOSFET is the most used MOSFET design available in present times. This is because of the various advantages of a Trench MOSFET over its counterparts. These advantages include High Cell Density, less onresistance due to formation of accumulation layer in the drift region [2], [5]. Various disadvantages of a Trench MOSFET include switching delays mainly due to the gate charge [5]. Hence, if the gate charge is reduced without changing onresistance much, the switching speed can be increased [3]. This is done in the proposed MOSFET by introducing an n^+- p junction in the gate of the MOSFET. Simulations reveal that this structure is successful in reducing the gate charge by appreciable amount without affecting the breakdown voltage or on-resistance.

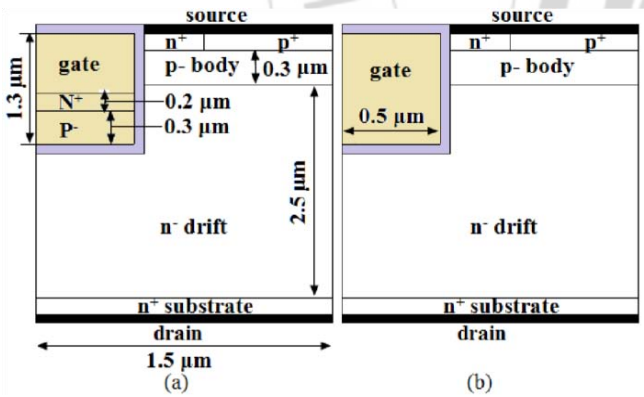

Figure 1: The structure of the (a) proposed Device and (b) the conventional Device.[1]

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2. Device Structure and Simulation Setup

The Conventional structure and the proposed structure are given in figure 1(b) and 1(a) respectively. The thickness of The gate oxide was 50 nm, the gate depth was 0.8 μm and 1.3 μm in the proposed structure and the conventional structure, respectively. It must be noted that the gate depth was lesser in case of the proposed structure which further eases the process of fabrication of the proposed structure. The doping profiles of the n+ region were taken to be the standard $1.0*10^{19}$ cm^{-3} and that of the p-region to be $1.7*10^{17}$ cm^{-3}.The doping of the drift region was $5.6*10^{15}$ cm^{-3}. The n_+ source thickness was 0.2 μm, the p-body thickness was 0.3 μm and the width of the Gate Trench in each half-cell was taken to be 1.5 μm. All the other measurements can be inferred from the figure. An important point to be noted is that the width of both n^+ and p regions in the n^+-p junction in the trench have the same thickness as the n^+ source and the p body region. This is done on purpose to further reduce the fabrication complexity, as now these regions can be grown along with the body and source. Moreover, the n^+-p junction is made out of polysilicon just like the gate of the conventional structure.

The simulation is done using 2-Dimensional ATLAS device simulator. In the simulation, the mobility and carrier statistic models used include bandgap narrowing, auger recombination, impact ionization, and equivalent model of a MOSFET and concentration's dependence on lifetime.

3. Characterization and Discussion

In this structure, we establish how the proposed structure is better than the conventional structure. This is done after comparing the transfer, output and gate charge- gate voltage characteristics of both the proposed structure and the conventional structure.

The transfer characteristics, shown in figure (2), reveal that the threshold voltage in case of the proposed structure is lesser from the conventional structure by 0.5 volts. This can be explained from the fact that in the proposed structure, the gate terminal, as it is connected to the n+ terminal of an n+-p junction, has an inherent self-potential of approximately 0.6 volts. This is due to the built in voltage in an n+-p junction. This reasoning is further backed if we observe the potential distribution in the trench channel region at 0 gate voltage and Source-drain voltage. Fig (3).

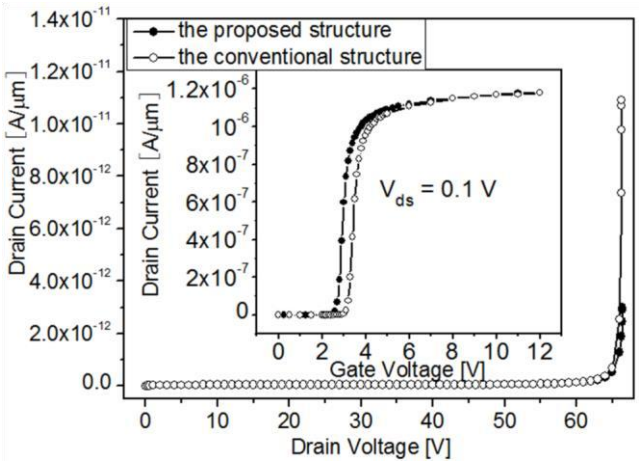

Figure 2: The transfer characteristics and input characteristics of both the structures [1].

In order to obtain the output characteristics (Fig. 4), the doping of the p region is changed to $2.2*10^{17}$ so that the value of threshold voltage of the proposed structure becomes equal to that of the conventional structure. Under this condition the characteristics reveal that the two structures exhibit identical current drive capability. However, both the original and the proposed structure show a kink effect at drain voltage equal to 21 volts and gate voltage equal to 7V. This is explained considering impact ionization in the original text [4]. The explanation claims that the increase in the impact ionization rate while going from 20 to 21 volts in case of 8V is 3 to 5 times the increase in case of 6 V(). This can be verified from Fig (6) Hence, the drain current increase much more rapidly in case the gate voltage is greater than 6 volts.

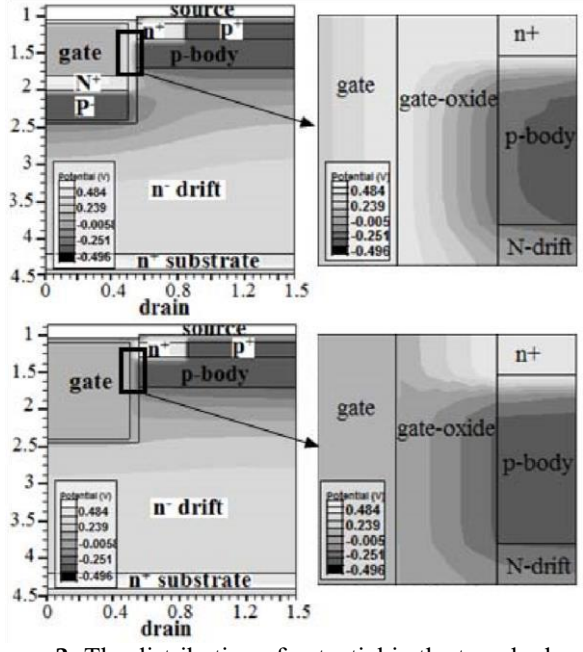

Figure 3: The distribution of potential in the trench-channel region atV_{gs}= *V*ds= 0.0 V in the proposed structure (above) and the conventional structure (below)[1]

The fig (5) reveals that the proposed structure has many advantages over the conventional structure as far as gate charge and hence, switching speed are being analyzed. Fig (5) shows that the proposed structure has less gate charge at any gate voltage before the threshold is reached. Also, the threshold is reached at a lower value of gate charge in case of the proposed structure. This can be explained by consider the inherent potential of the n+ region. We know that the capacitance is related to charge and voltage across its terminals as-

$$Q=C\times V$$

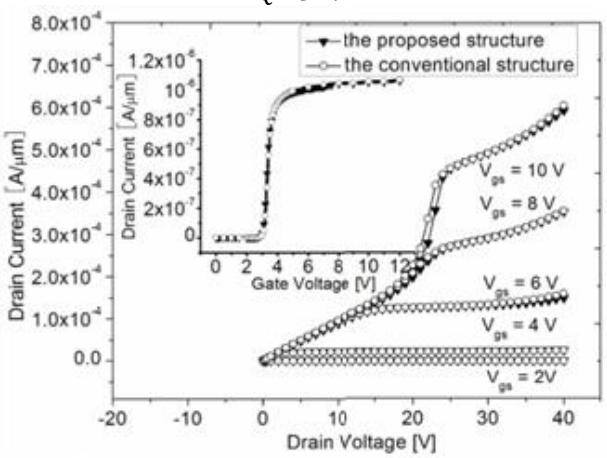

Figure 4: The comparison of output characteristics.[1]

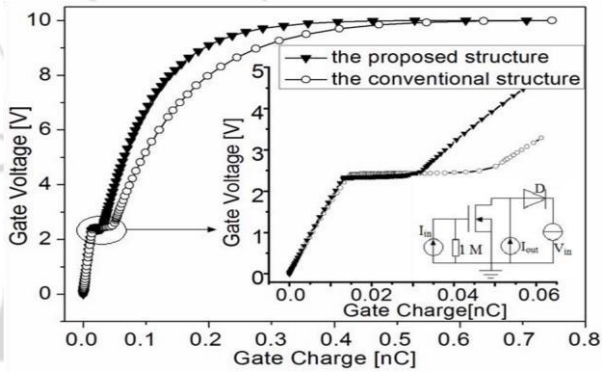

Figure 5: Gate Voltage vs gate charge characteristic. [1]

Also, in case of the proposed structure, the presence of depletion layer would decrease the gate drain coupling and hence, the overall capacitance decreases which, from Eq-1, results in decrease in gate charge and hence an increase in the overall switching speed.

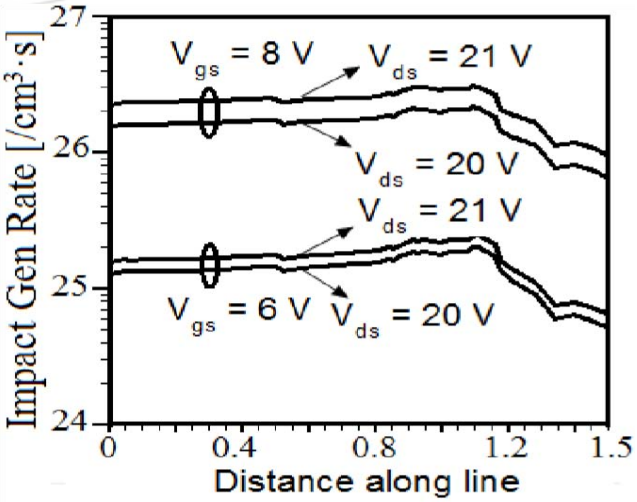

Figure 6: Impact Ionization Rate.[1]

4. Conclusions

A novel trench gate power MOSFET with 49.5% reduction in gate charge was analyzed with the help of various characteristics. It was established that the n+-p junction introduced was successful in reducing the gate charge. Also, it was established that the fabrication of this new MOSFET structure can be done by slight changes in the process and hence does not lead to large increase in the cost of the overall manufacturing process. The other parameters of the MOSFET were not adversely affected by the introduction of this P+-n junction and the only appreciable change other than that of the gate charge was the decrease of the terminal voltage by 0.6V. Also, the principle of reducing the gate charge is different from [6], [7], and [8].

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