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Design and Analysis of Full Adder Using Adiabatic Logic

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Abstract: ***Power dissipation is an increasing concern in VLSI circuits. New logic circuits have been developed to meet these power requirements. Power dissipation can be minimized by using various adiabatic logic circuits. In this paper an Adder circuit has been proposed based on 2PASCL and ECRL logic and then compared with Positive Feedback Adiabatic Logic(PFAL), Two-Phase Adiabatic Static Clocked Logic(2PASCL) respectively. Comparison shows significant power saving.***

Keywords: adiabatic switching, energy dissipation, power clock, 2PASCL, ECRL

1. Introduction

In recent times, researchers have been focused on increasing clock and logic speed to enhance the performance of portable electronic devices. The power consumption is proportional to the square of the power supply voltage. Therefore voltage scaling is one of the important methods used to reduce the power consumption. To improve the circuit performance the transistor threshold voltage is scaled down according to supply voltage [1].

Various adiabatic logic families have been proposed emphasizing the energy recovery principle. In adiabatic circuits power dissipation is significantly less than that of CMOS circuits. Hence, adiabatic circuits are promising candidate for low-power circuits which can be operated in the frequency range in which signals are digitally processed. In this study, we design, simulate and compare the power consumption of 1-bit full adder using PFAL, 2PASCL and ECRL-2PASCL technologies.

2. CMOS Circuits Vis-A-Vis Adiabatic Logic Circuits

1. CMOS Circuits

In CMOS power dissipation occurs during device switching. The PMOS and NMOS can be modeled by an ideal switch in series with a resistor as shown in figure1 [9]. The pull-up and pull-down network is connected to the load capacitance C_L. When the logic level is "1", there is a sudden flow of current through R. The charge transferred by power supply to C_L is $Q = C_L V_{dd}$. Hence the energy drawn from the power supply is $Q.V_{dd} = C_L {V_{dd}}^2$ [10]. The energy stored in the load capacitance is $E_{stored} = \frac{1}{2} C_L {V_{dd}}^2$. The remaining energy is dissipated in R.

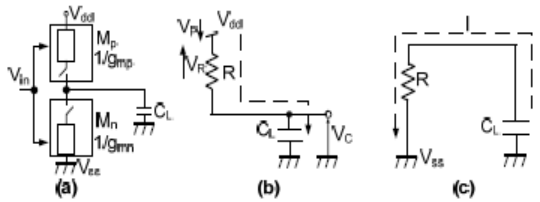

Figure 1: (a) A CMOS model showing an ideal switch in series with resistor. (b) Charging. (c) Discharging

The equal amount of energy is dissipated during discharging process. Therefore total amount of energy dissipated during charging and discharging process is

$$E_{total} = E_{charge} + E_{discharge}$$

$$= \frac{1}{2} C_L {V_{dd}}^2 + \frac{1}{2} C_L {V_{dd}}^2 = C_L {V_{dd}}^2$$

From the above analysis it is clear that the energy consumption can be reduced by reducing V_{dd}. By decreasing the switching activity in the circuit, the power consumption ($P = dE/dt$) can also be decreased.

2. Adiabatic Logic Circuits

The term adiabatic switching is used to minimize energy loss during charging and discharging. The term ADIABATIC is taken from Greek language that is used to explain the thermodynamics process in which no exchange of energy occurs between the system and the external environment. A constant current is used to charge or discharge the nodes during adiabatic process. This is obtained by using AC power supplies to initially charge the circuit during specific adiabatic phase and then discharge the circuit to recover the supplied charge.

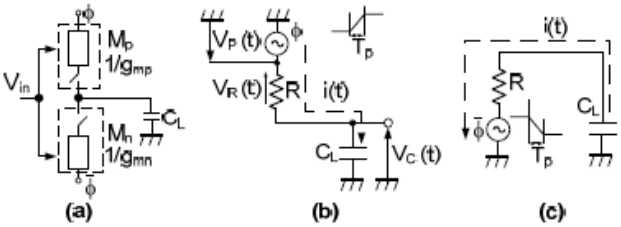

Figure 2: (a) Model of adiabatic logic showing an ideal switch in series with resistance and two complementary voltage supply clocks. (b) Charging. (c) Discharging.

In fig.2 the energy dissipation process in an adiabatic circuit is shown [9]. Due to the use of a time varying voltage source, the rate of the switching transition in adiabatic circuit is decreased. Each voltage changes with time [9], as shown in figure 3.

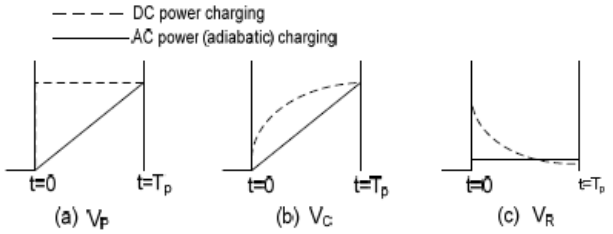

Figure 3: Graph showing the changes of voltage in adiabatic circuits to conventional dc power supply at the (a) power supply V_P (b) node capacitance V_C (c) resistance V_R

The uniform charge transfer over entire time duration provides reduced peak current in adiabatic circuits. Therefore the overall energy dissipation during the transition phase is

$$E_{diss} = \hat{I}^2 R T_P = \left(\frac{C_L V_{dd}}{T_P}\right)^2 R T_P = \left(\frac{RC_L}{T_P}\right) C_L {V_{dd}}^2$$

According to above equation the power dissipation can be decreased by increasing T_P.

When $\overline{\emptyset}$ changes from HIGH to LOW discharging process takes place through NMOS. The energy stored in the capacitors is drawn by the system and is used. Thus the energy dissipation does not occur and it is recycled.

3. Adiabatic Logic Families

The adiabatic logic families can be divided in two categories – Fully Adiabatic and Partial Adiabatic. All the charges stored on the load capacitor is recovered and fed back to the power supply in fully adiabatic circuits. Due to this the fully adiabatic circuits becomes slower and complex as compared to partial adiabatic circuits. Pass Transistor Adiabatic Logic (PAL) and Split-Rail Charge Recovery Logic (SCRL) are popular fully adiabatic techniques.

In Partial Adiabatic or Quasi Adiabatic circuits some charge is allowed to transfer to the ground. Therefore a part of the energy can be recovered. Efficient Charge Recovery Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL), 2N-2N2P adiabatic logic, NMOS Energy Recovery Logic (NERL), Clocked Adiabatic Logic (CAL), Two Phase Adiabatic Static Clocked Logic (2PASCL) etc are example of partial adiabatic logic.

1) 2PASCL

The schematic of 2PASCL inverter [10] is shown in figure 4. Two MOSFET diodes are used charge recycling and to improve the discharging speed of internal nodes. In which one is connected between output node and power clock and other is connected between the NMOS and the other power source. This circuit uses two split level sinusoidal waveforms. Due to this voltage difference between current carrying electrodes can be minimized which results in reduced power dissipation. It works in two phases: Evaluation and Hold. $\emptyset$ swings up and $\overline{\emptyset}$ swings down in evaluation phase and vice-versa takes place in hold phase. The charging/ discharging process does not occur after every clock cycle which results in minimum number of dynamic switching. It will suppress the node switching activities.

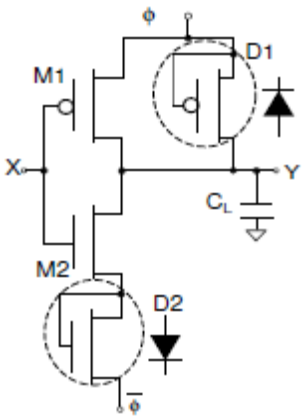

Figure 4: 2PASCL inverter circuit

The circuit operation is divided in two phases:

a) Evaluation Phase

- Output node Y is low and PMOS is ON then C_L is charged through PMOS and output becomes in high state.
- If node Y is Low and NMOS is on then no transition occurs.
- If Y is high and PMOS is ON then no transition occurs.
- If node Y is High and NMOS is ON then discharging process takes place through NMOS and D_2 and output becomes at 0 logic.

b) Hold Phase

- If node Y is Low and NMOS is ON then no transition occurs.
- When the preliminary state of Y is High and PMOS is ON, discharging through D_1 occurs.
- The charging/discharging process does not necessarily occur during every clock cycle, so the number of dynamic transitions decreases, which results in reduced power dissipation.

2) ECRL

The schematic of ECRL proposed by Moon and Jeong [13] is shown in figure 5. It's structure is similar to cascade voltage switch logic with differential signaling. The supplied energy is recovered and reused by using an AC power supply. The power clock generator can always drive a constant load capacitance independent of the input signal by generating both out and /out.

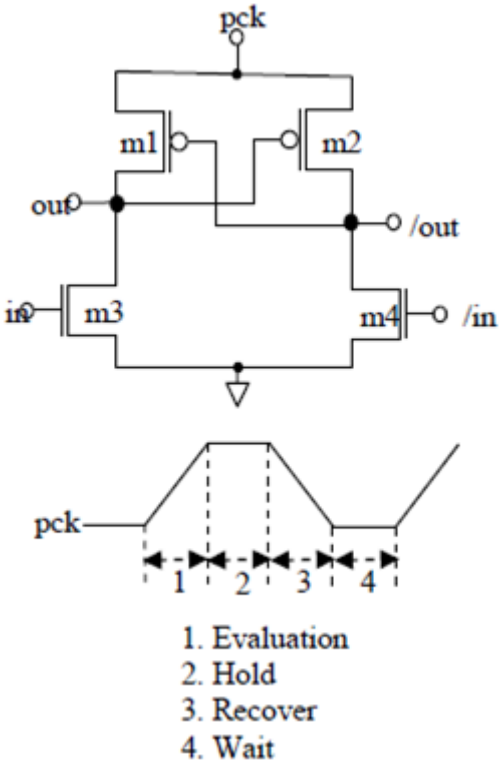

Figure 5: Schematic of ECRL inverter and power clock.

For efficient recovery process ECRL also uses four phase clocking such as 'evaluation', 'hold', 'recovery' and 'wait'. Initially, input 'in' is high and input '/in' is low. When power clock rises from zero to VDD, since m3 is on so output 'out' is connected to ground. In evaluation phase /out follows the power clock pck. When pck reaches to V_{dd} the out hold 0 and /out hold V_{dd}. When power clock goes from V_{dd} to 0 /out returns it's energy to power clock. Wait phase is used to maintain the clock symmetry.

3) PFAL

The schematic of PFAL [15] logic is shown in figure 6. It is a dual rail circuit with partial energy recovery. The core of all the PFAL gate is an adiabatic amplifier a latch made by the two PMOS *M1-M2* and two NMOS *M3-M4*, to avoid a logic level degradation on the output nodes. PFAL generates two complemented outputs. For the purpose of adiabatic charging a time varying source is used that is known as power clock which have four phases. Let us consider the case when input is high. Then transistors m5 and m1 are in on state when the value of power clock increases. Due to this out is connected to ground and /out will follow the changes of power clock. When the power clock comes to V_{dd}, out will be zero and /out will be V_{dd} which will act as input for the next stage. When power clock varies from V_{dd} to 0 then the energy will be recovered through the m1.

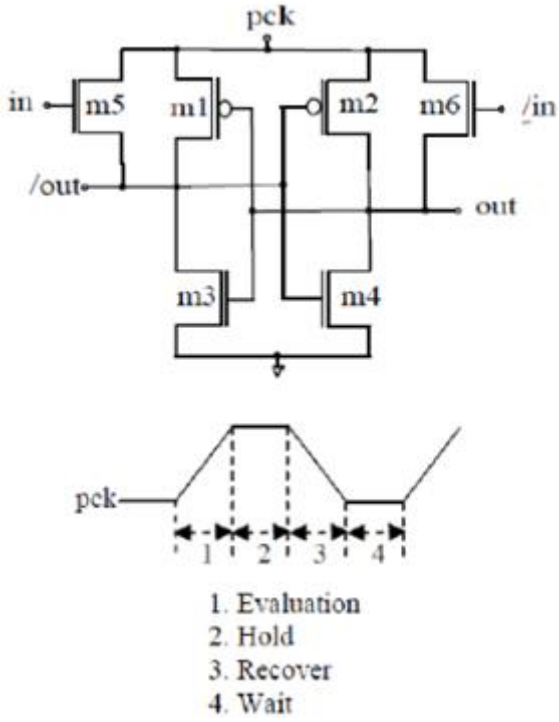

Figure 6: PFAL logic circuit

4. Proposed Design

In this paper we have proposed a new design of 1-bit full Adder circuit which is a combination of ECRL and 2PASCL logic. The schematic and waveform of the proposed design is shown below.

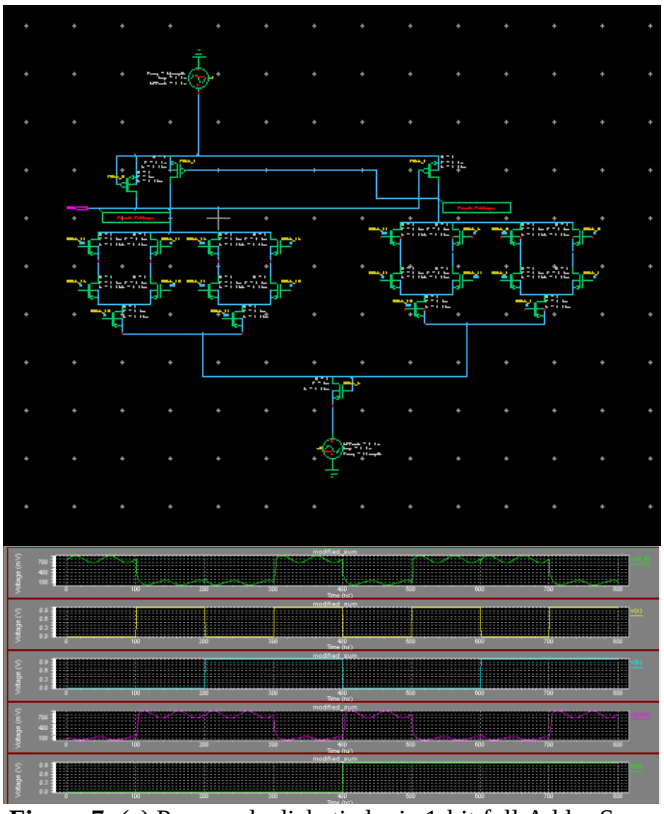

Figure 7: (a) Proposed adiabatic logic 1-bit full Adder Sum schematic and waveform

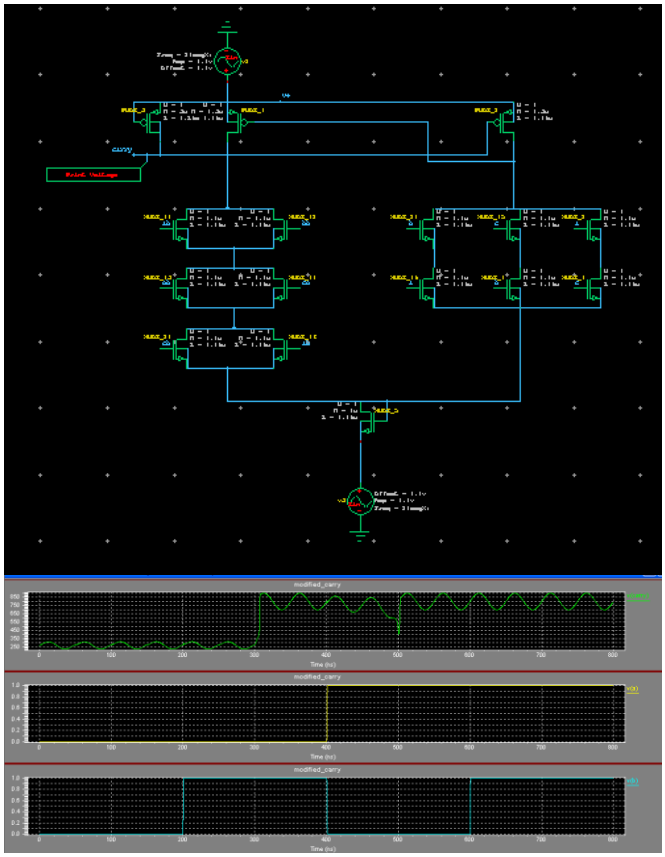

Figure 7: (b) Proposed adiabatic logic 1-bit full Adder Carry schematic and waveform

Parameter \ Logic		PFAL	2PASCL	PFAL-2PASCL	Proposed
Total Power (µW)	Sum	1.14	14.87	1.31	0.09
	Carry	0.63	14.9	0.8	0.39
Delay (ns)	Sum	2.015	0.61	7.14	2.46
	Carry	2.01	0.69	3.14	6.41

Figure 8: Performance analysis of various design techniques at 20MHz

5. Simulation

The simulation is performed using a tanner tool at 90nm CMOS technology node. The simulation results obtained for 1-bit full Adder of proposed logic and comparison with different adiabatic logics has been shown in figure 8. The simulation is performed at operating frequency of 20MHz. Two split level sinusoidal power supply has been used in this design.

6. Conclusion

In this paper we have designed and simulated 1-bit full adder using energy efficient adiabatic logic and two phase adiabatic static clocked logic. The simulation result shows that power consumption of the proposed design is considerably less than that of PFAL, 2PASCL and PFAL-2PASCL techniques. From this analysis it clear that the proposed design is very power efficient technique in low power VLSI regime.

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