the xnor gate is driven by the outputs of last 2 scan cells in the same chain sck1 and sck. The output of the xnor gate connects to multiplexer selects input and it is assumed there is no inversion between sck and sck1. When sck and sck1 have different values the xnor output will be zero and d flip flop holds its previous values. Otherwise d flip flop will be updated by phase shifter output.

4. Results

4.1 Simulation Results

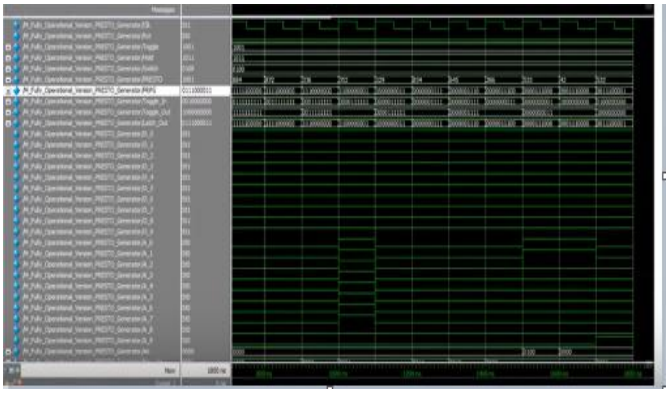

Figure 5: Fully operational PRESTO generator

Figure 5 shows the simulation of fully operational PRESTO generator with separate toggle and hold cycle. Figure 6 shows simulated result of proposed architecture LP decompressor with transition controller.

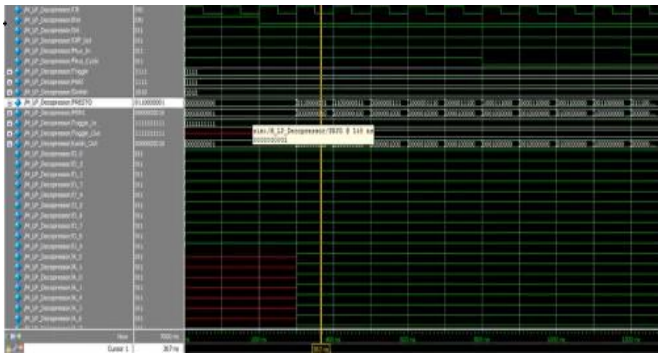

Figure 6: LP decompressor

4.2 Comparison with and without transition controller

Table 1: Comparison of 2 units

Cycles	Scan Chain Values	Without Transition Controller		With Transition Controller	
		Scan Chains	Transitions	Scan Chains	Transitions
	001010	011001		011001	
1	00101	001100	6	001100	6
2	0010	100110	9	100110	9
3	001	010011	11	110011	6
4	00	101001	13	111001	4
5	0	010100	14	111100	2
6	-		10	011110	6
Total			63		33

4.3 Power Report

Table 2: Power Report

	Architecture	Power Consumption
1	PRESTO Generator	.492W
2	Fully Operational PRESTO Generator	.344W
3	LP Decompressor With Transition Controller	.224W

5. Conclusion

Using low power decompressor with transition controller pseudo random test patterns are generated with reduced Switching activity and thus power consumption is reduced. The efficiency of the work is analyzed using s27 benchmark circuit of ISCAS 89 family. Xilinx is the tool used for simulation and interpretation. Scan chain is formed with the flip flop from s27 circuit. The resultant test vector can yield desired fault coverage faster than conventional pseudo random patterns also reducing toggling rates to desired level. It I therefore an attractive low power test scheme which allows for trading off test coverage, pattern counts and toggling rates in a very flexible manner

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