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Realization of Programmable PRPG with Enhanced Fault Coverage Gradient

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Abstract: ***This paper describes a low power programmable pseudorandom pattern generator with desired toggling level and also enhanced fault coverage compared with other BIST based on PRPG. It comprised of finite state machine LFSR driving a phase shifter and it allows the device to produce binary sequence with preselected toggling activity. Generator is automatically controlled providing easy and precise tuning. Furthermore, this paper introduces a test compression method to avoid repeated pattern generation for testing the same device. The main highlight of this paper is to reduce the test data volume and test data memory.***

Keywords: BIST, low power test, PRPG, test data volume compression

1. Introduction

Test compression has become the main stream DFT methodology nowadays. LBIST which provides very robust DFT is increasingly used with test compression. This hybrid approach is an evolutionary step. Hybrid scheme consumes more power than CUT due to high data activity. The test power can be reduced by preventing transition at memory element. This is achieved by introducing gating logic between scan cell output and logic they drive. The advent of low power BIST has added a new dimension to the BIST with low power. Switching activity is reduced and satisfactory fault coverage is obtained. Power consumption can easily exceed the maximum rating when testing at speed scan patterns must be shifted at a low speed and last few cycle at maximum frequency. In this paper a PRPG for LP BIST application is proposed along with LP decompressor. All the methods which is discussed above is used with the architecture presented in order to reduce power consumption. All the three architecture proposed in this paper aims at reducing switching activity during scan loading due to its preselected toggling levels. This is the first LP test compression scheme that is integrated in every way with the BIST environment. This will let the designers to shape the power envelope accurately.

This paper is organized as follows section 2 introduces existing methods. PRESTO generator and fully operational PRESTO generator with operation is explained in detail. Section 3 introduces proposed work in detail. Section 4 gives the simulated and comparison results. This paper concludes with variety of experimental results and finally wraps up with section 5.

2. Existing Methods

2.1 PRESTO Generator

Given figure shows the structure of a preselected toggling (PRESTO) generator. The kernel of the generator is a n bit random pattern generator connected with a phase shifter feeding scan chains which will produce pseudo random test patterns. PRPG is formed by linear feedback shift register (LFSR) or a ring generator. There are n hold latches between the PRPG and the phase shifter. Hold latch are controlled by toggle control register. When the latch is enabled, it is transparent for the data which is going from PRPG to the phase shifter and it is in toggle mode. When the latch is disabled, the corresponding bit of PRPG is captured and saved for a number of clock cycles and thus feeding the phase shifter with a constant value. Every scan chains remains in a low power mode provided only disabled hold latches.

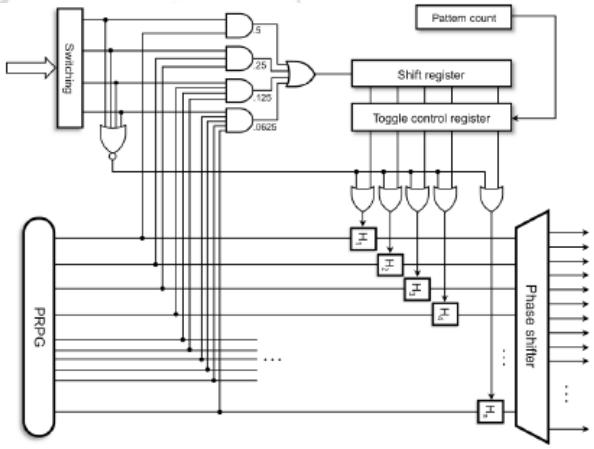

Figure 1: PRESTO Generator

The contents of toggle registers are zeros (0s) and ones (1s). 1s indicate latches in the toggle mode, thus transparent for data. Their fraction determines a scan switching activity. The control register is reloaded once per pattern with shift register content. The enable signals injected into the shift register are produced in a probabilistic fashion. Using the original PRPG with programmable set of weights. The weights are determined by four AND gates producing 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate allows choosing of probabilities beyond simple powers of 2. A 4-bit register switching is used to activate AND gates, and allows selecting a user-defined level of switching activity. For example, if the switching code 0100, 25% of the control register will set to 1, and thus 25% of hold latches will be enabled

An additional 4-input NOR gate detects the switching code 0000, which will switch the LP functionality off. Note that when working in the weighted random mode, the switching level selector ensures statistically stable content of the control register in terms 1s it carries. As a result, the same fraction of scan chains will stay in the LP mode even when low toggling chains will keep changing from one test pattern to another. It will correspond to a certain level of toggling in the scan chains.

2.2 Fully operational PRESTO generator

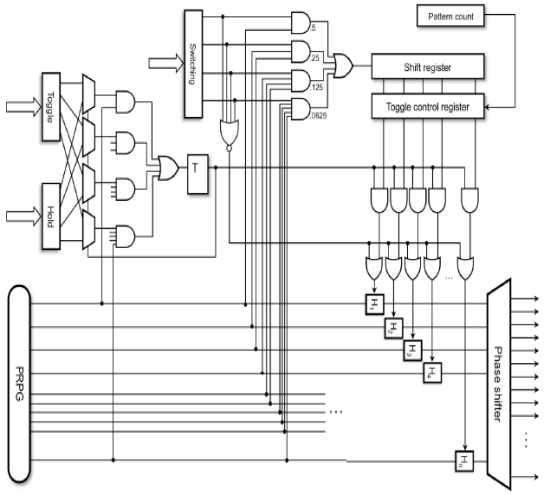

Figure 2: Fully operational PRESTO generator

This section presents additional features that make the PRESTO generator fully operational in a wide range of desired switching rate. This approach splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals. We use a T-type flip-flop to move the generator back and forth between these 2 intervals. T FFs switches whenever there is a 1 on its input data. If it is set to 0, the generator enters the hold period with all latches temporarily disabled. This is accomplished by placing AND gates on the control register outputs which will allow freezing of all phase shifter inputs. Only a single scan chain crosses a given core. Its abnormal toggling may cause unacceptable heat dissipation that can only be reduced due to temporary hold periods. If the T flip-flop is set to the toggle period (1), then the latches enabled by the control register can pass data moving from the PRPG to the scan chains. Two additional parameters kept in Hold and Toggle registers determine how long the entire generator remains either in the hold mode or in the toggle mode. To terminate from modes, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced similar to that of weighted logic used to feed the shift register. The T flip-flop also controls four 2-input multiplexers routing data from the Toggle and Hold registers. It allows selecting a source of control data that will be used in the next cycle to possibly change the operational mode of the generator. For example, in toggle mode the input multiplexers observes the Toggle register. The flip-flop toggles once the logic output is 1 and as a result all hold latches freeze in the last recorded state. Until another 1 occurs on the weighted logic output they will remain in the same state. The occurrence of this event is now related to the content of the Hold register, which determines termination of the hold mode.

3. Proposed Method

The architecture consists of an additional block transition controller at the output of the phase shifter. The core principle of the decompressor is to disable both weighted logic blocks and deploy deterministic data control. The content of the toggle control register can now be selected in a deterministic manner due to a multiplexer placed in front of the shift register. The Toggle and Hold registers are employed to alternately preset a 4-bit binary down counter, and thus to determine durations of the hold and toggle phases. When this circuit reaches the value of zero, it causes a signal to go high in order to toggle the T flip-flop. The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state. Both the down counter and the T flip-flop need to be initialized during every test pattern. The initial value of the T flip flop decides whether the decompressor will begin to operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, and determines that mode's duration.

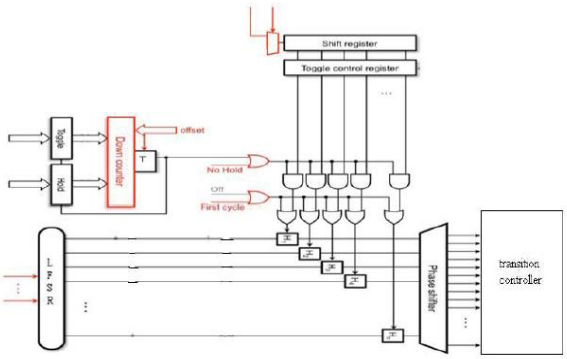

Figure 3: LP decompressor with transition controller

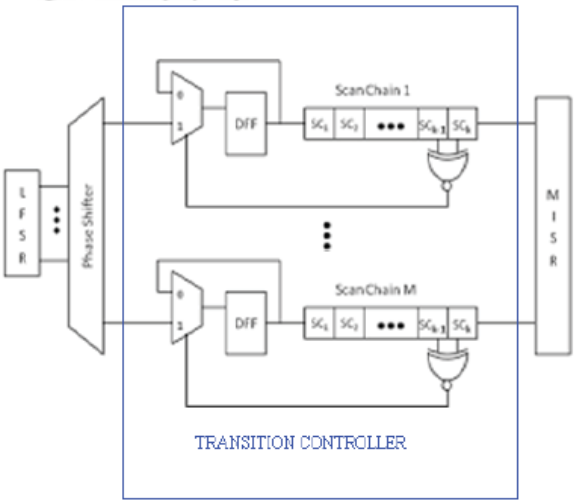

Figure 4: Transition Controller

An adaptive technique is applied to reduce the shift power to improve the power reduction in logic BIST. To get the required power reduction an additional module called transition controller is implemented. Transition controller consists of a mux, xnor gate and a D flip flop. The input of

the xnor gate is driven by the outputs of last 2 scan cells in the same chain sck1 and sck. The output of the xnor gate connects to multiplexer selects input and it is assumed there is no inversion between sck and sck1. When sck and sck1 have different values the xnor output will be zero and d flip flop holds its previous values. Otherwise d flip flop will be updated by phase shifter output.

4. Results

4.1 Simulation Results

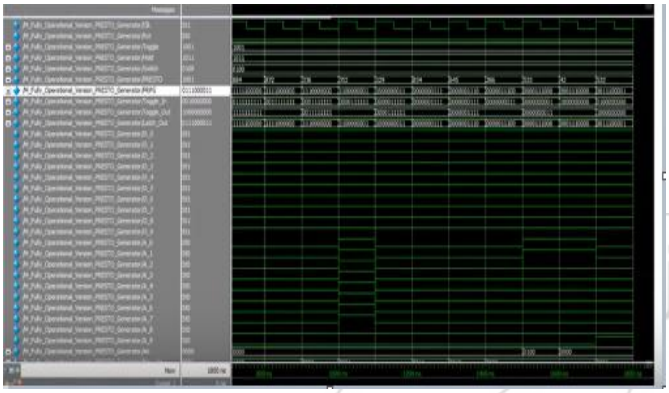

Figure 5: Fully operational PRESTO generator

Figure 5 shows the simulation of fully operational PRESTO generator with separate toggle and hold cycle. Figure 6 shows simulated result of proposed architecture LP decompressor with transition controller.

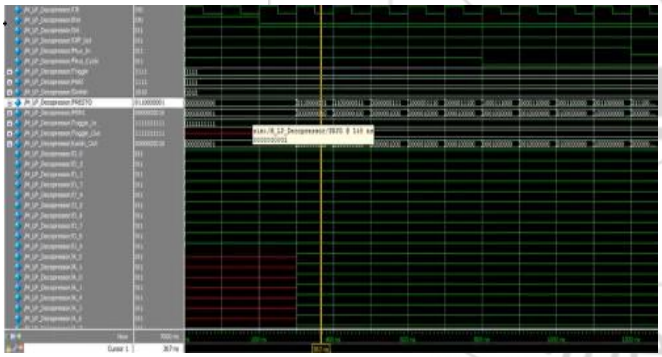

Figure 6: LP decompressor

4.2 Comparison with and without transition controller

Table 1: Comparison of 2 units

Cycles	Scan Chain Values	Without Transition Controller		With Transition Controller	
		Scan Chains	Transitions	Scan Chains	Transitions
	001010	011001		011001	
1	00101	001100	6	001100	6
2	0010	100110	9	100110	9
3	001	010011	11	110011	6
4	00	101001	13	111001	4
5	0	010100	14	111100	2
6	-		10	011110	6
Total			63		33

4.3 Power Report

Table 2: Power Report

	Architecture	Power Consumption
1	PRESTO Generator	.492W
2	Fully Operational PRESTO Generator	.344W
3	LP Decompressor With Transition Controller	.224W

5. Conclusion

Using low power decompressor with transition controller pseudo random test patterns are generated with reduced Switching activity and thus power consumption is reduced. The efficiency of the work is analyzed using s27 benchmark circuit of ISCAS 89 family. Xilinx is the tool used for simulation and interpretation. Scan chain is formed with the flip flop from s27 circuit. The resultant test vector can yield desired fault coverage faster than conventional pseudo random patterns also reducing toggling rates to desired level. It I therefore an attractive low power test scheme which allows for trading off test coverage, pattern counts and toggling rates in a very flexible manner

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