4. Simulation Results

The proposed aging aware multipliers are implemented in verilog-HDL using Xilinx ISE 14.7v tools. The results are simulated for different input vectors using Xilinx ISim Simulator.

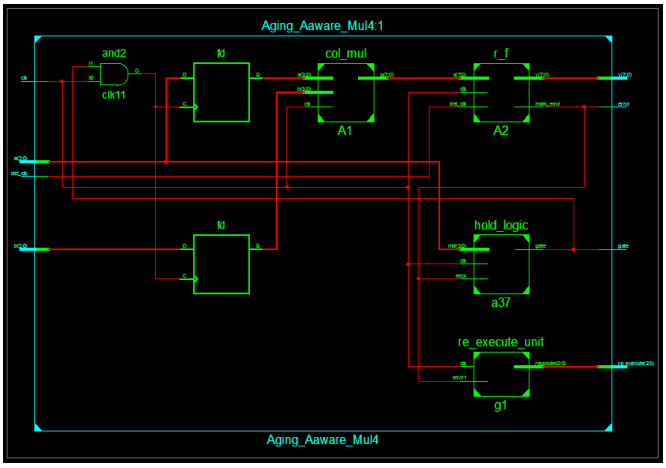

Figure 8: RTL Schematic.

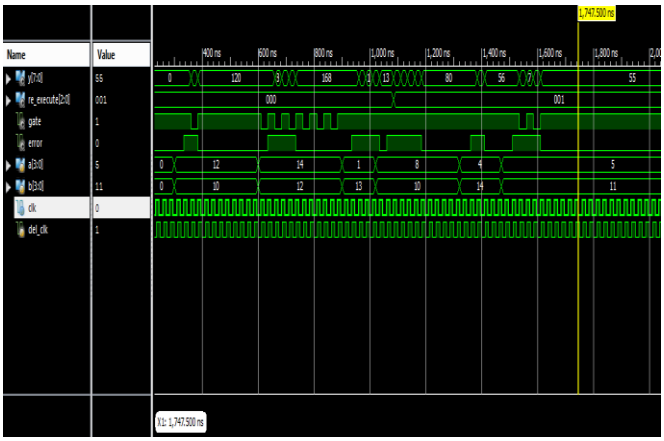

Figure 9: Simulation waveforms

5. Conclusion

In this the AHL circuit is proposed which decides whether the operations require one cycle or two cycles based on the number of zeroes in the input bits. The Razor flip-flops detect the number of errors and generate the error signal and acknowledge the AHL circuit to re-execute the operation. By using the AHL the timing violations due to aging effects can be avoided and overcome the performance degradation of the multiplier.

This variable latency design is used with the column by-passing multiplier and row bypassing passing multiplier to minimize the power requirements to the multiplier and the speed of operations can be achieved.

References

[1] Ing-Chao Lin, *Member*, *IEEE*, Yu-Hung Cho, and Yi-Ming Yang. "Aging-Aware Reliable Multiplier Design with Adaptive Hold Logic" IEEE transactions on very large scale integration (VLSI) systems, vol. 23, no. 3, march 2015.

[2] Y. Cao. (2013). Predictive Technology Model (PTM) and NBTI Model[Online]. Available: http://www.eas.asu.edu/ptm

[3] S. Zafar et al., "A comparative study of NBTI and PBTI (charge trapping) in SiO2/HfO2 stacks with FUSI, TiN, Re gates,"in Proc. IEEE Symp. VLSI Technol. Dig. Tech. Papers, 2006, pp. 23–25.

[4] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Threshold voltage instabilities in high-k gate dielectric stacks," IEEE Trans. Device Mater. Rel., vol. 5, no. 1, pp. 45–64, Mar. 2005.

[5] H.-I. Yang, S.-C. Yang, W. Hwang, and C.-T. Chuang, "Impacts of NBTI/PBTI on timing control circuits and degradation tolerant design in nanoscale CMOS SRAM," IEEE Trans. Circuit Syst., vol. 58, no. 6, pp. 1239–1251, Jun. 2011.

[6] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and miimization of pMOS NBTI effect for robust naometer design," in Proc. ACM/IEEE DAC, Jun. 2004, pp. 1047–1052.

[7] H. Abrishami, S. Hatami, B. Amelifard, and M. Pedram, "NBTI-aware flip-flop characterization and design," in Proc. 44th ACM GLSVLSI, 2008, pp. 29–34

[8] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesis of digital circuits," in Proc. ACM/IEEE DAC, Jun. 2007, pp. 370–375.

[9] A. Calimera, E. Macii, and M. Poncino, "Design techniqures for NBTI-tolerant power-gating architecture," IEEE Trans. Circuits Syst., Exp. Briefs, vol. 59, no. 4, pp. 249–253, Apr. 2012.

[10] K.-C. Wu and D. Marculescu, "Joint logic restructuring and pin reorder-ing against NBTI-induced performance degradation," in Proc. DATE, 2009, pp. 75–80.

[11] Y. Lee and T. Kim, "A fine-grained technique of NBTI-aware voltage scaling and body biasing for standard cell based designs," in Proc. ASP-DAC, 2011, pp. 603–608.