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Performance Evaluation of CNTFET Based Ternary Basic Gates and Half Adder

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Abstract: ***The shrinkage in size of VLSI chips as well as improved energy efficiency is the need of the modern digital era. Using ternary logic instead of conventional binary logic helps to reduce circuit complexity and hence reduces chip area. Carbon nanotubes FET (CNTFET) are preferred over CMOS for logic design due to its high performance i.e. excellent transport property, low resistivity and higher current on-off ratio. The performance of ternary based logic gates is evaluated in terms of parameter such as power dissipation and delay.***

Keywords: Carbon nanotube (CNT), Single walled CNT (SWCNT), Multiple valued logic (MVL), Carbon nanotube FET (CNTFET).

1. Introduction

Multiple Valued logic (MVL) such as Ternary logic is considered over binary logic due to its considerable advantages such as reduced interconnects, chip area [3], faster serial, serial-parallel arithmetic operations. MVL logic enhances the performance of CMOS technology in the logic design [6].

Scaling down the dimensions in Si FET is the necessity in modern era but situation like short channel effect where electron are transferred directly between source and drain restricts further scaling as such effect causes parameters variation[9]. Using CNTFET, a nanoelectronic device provides the way for scaling process. Voltage mode MVL circuits are achieved through multi threshold design [7]. In CMOS, multi threshold is obtained by altering voltage across bulk terminal while in CNTFET it can be achieved by just using different diameters.

2. Carbon nanotube based FET

Single walled CNT (SWCNT) is made by rolling graphene sheet into cylindrical shape so that the structure is one-dimensional. SWCNT is used to design electronics devices [8] in CNTFETs. CNT has excellent chemical, mechanical, electrical property. The chemical bond in CNT consists of sp^2 which provides it chemical strength. CNT is a good alternative since it provides carrier transportation in one-dimensional thereby suppressing the scattering effect and also it has low power dissipation. SWCNTs electrical property can be either metallic or semiconducting depending on its chirality. Chirality (n, m) is decided by the chiral angle at which graphene sheets are rolled. The CNT is metallic when n = m and it is said to be semiconducting when n-m=3i, where I is an integer. Threshold voltage can be altered by changing the diameter of CNT. Chirality vector (n, m) depends on diameter as follows [14-16]:

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm}$$

Where a_0= 0.142 nm is a interatomic distance between carbon atoms. Schematic diagram of CNTFET is shown in figure 1[14-16]:

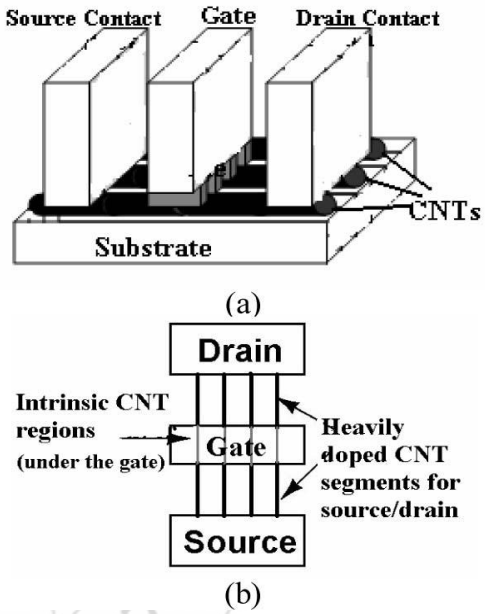


Figure 1: CNTFET (a) Schematic diagram (b) Top view

The working of CNT based FET is similar to Si based device as in CNTFET also gate acts a current controller. Moreover the I-V characteristics of both devices are also alike. Threshold voltage of CNTFET is inversely proportional to its diameter and is given by the relation [14-16], i.e.

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}aV_\pi}{3D_{CNT}}$$

3. Ternary basic gates

Ternary logic function is represented by 0, 1 and 2 which denote false, undefined and true value in a function. The voltage level representing these logic functions is as follows:

Table 1: Ternary logic representation

Voltage level	Logic
0	0
1/2 V_{dd}	1
V_{dd}	2

The power supply voltage [14] used is 0.9V. The logic 1 is represented by a voltage level between 0.3-0.6V whereas logic 0 corresponds to voltage level below 0.3V and logic 2 corresponds to voltage level above 0.6V. The chirality vector used are (19, 0), (13, 0) and (10, 0).The diameter corresponding to above chirality vectors are 1.48 nm, 1.018nm and 0.783nm respectively and hence the threshold voltages are 0.289, 0.428 and 0.559V respectively [6].

3.1 Ternary inverter

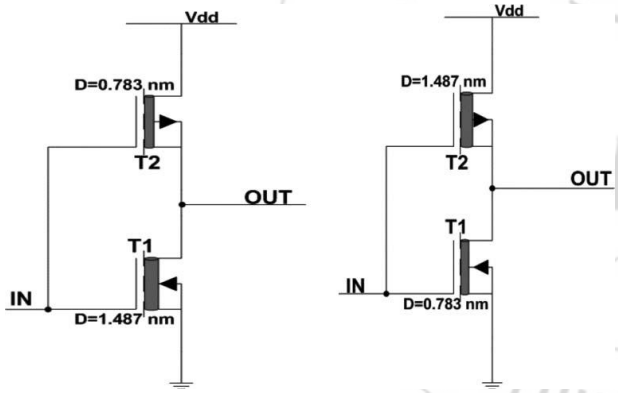
There are basically three type of invertor represented as [2]:

$$\overline{X_C} = \begin{cases} C & if\ X = 1 \\ 2 - X & if\ X \neq 1 \end{cases}$$

Where C represents logic 0 for negative ternary inverter (NTI), logic 1 for standard ternary inverter (STI) and logic 2 for positive ternary inverter (PTI) .The schematic diagram of the ternary inverter along with its truth table is shown below:

Table 2: Truth table of ternary inverter

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0



(a) (b)

Figure 2: (a) NTI (b) PTI

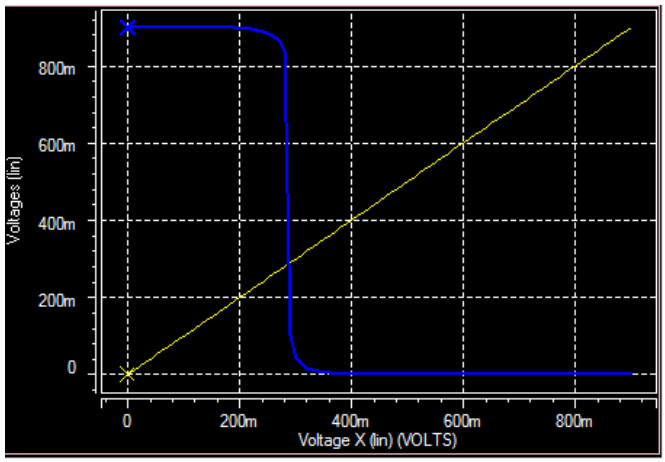


Figure 3: VTC of NTI

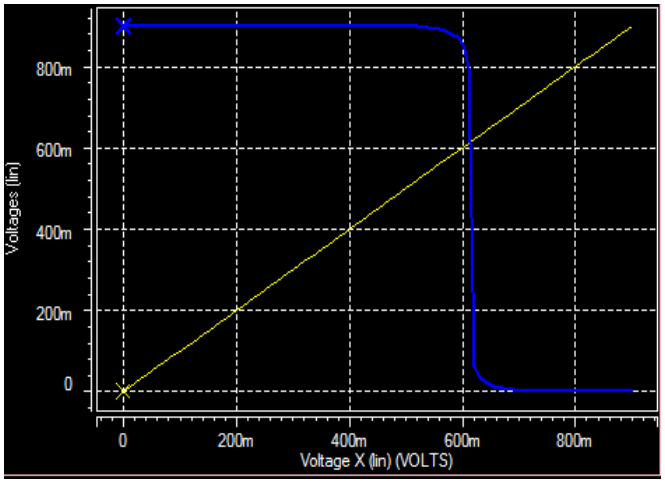


Figure 4: VTC of PTI

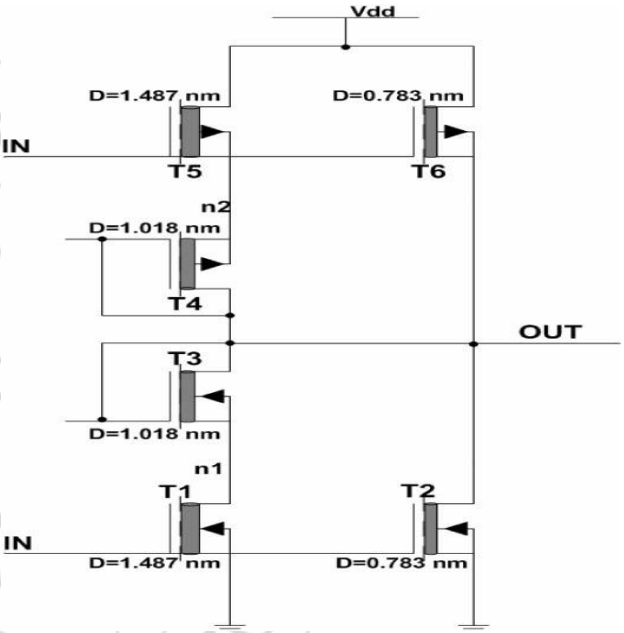


Figure 5: Schematic diagram of STI

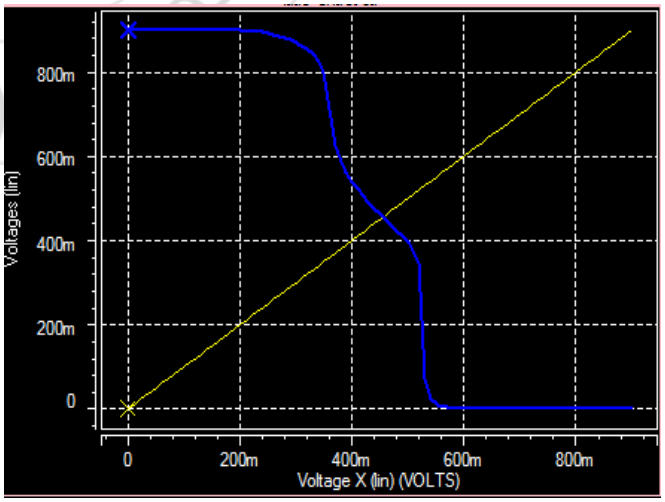


Figure 6: VTC of STI

3.2 Ternary NAND and NOR gate

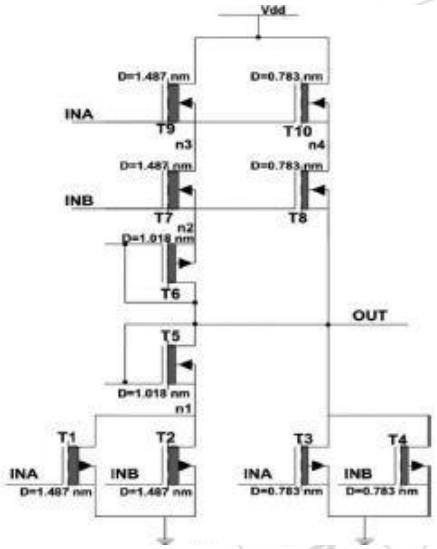
NOR and NAND gate are defined as:

$$Ynor = \overline{\max(X1, X2)}$$

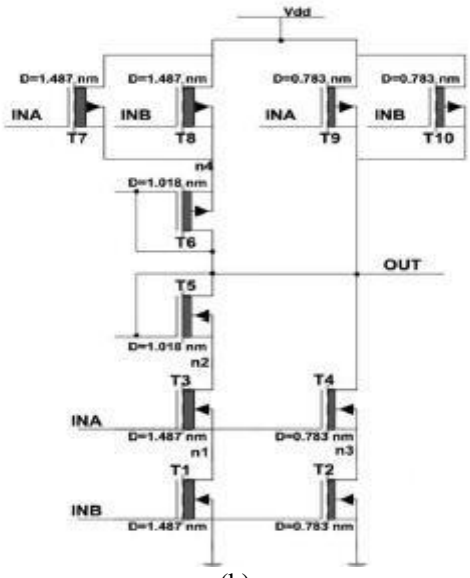
$$Ynand = \overline{min\ (X1,X2)}$$

Table 3: Truth table of NAND and NOR logic

Input X_1	Input X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0



(a)



(b)

Figure 7: Schematic diagrams (a) NOR (b) NAND

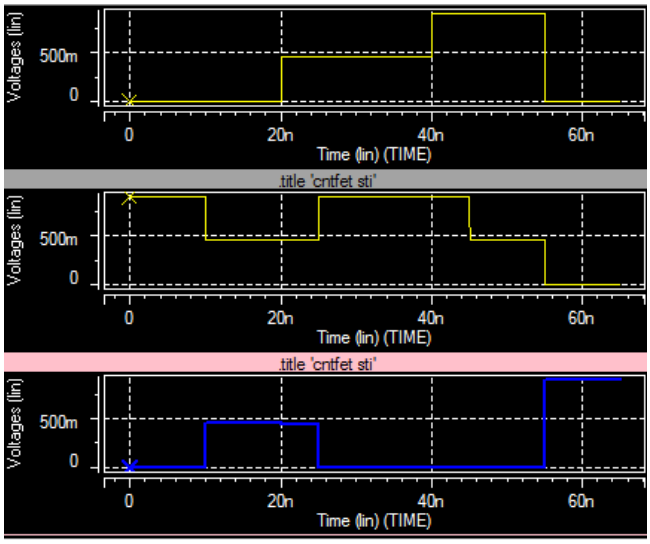


Figure 8: Simulation of Ternary NOR

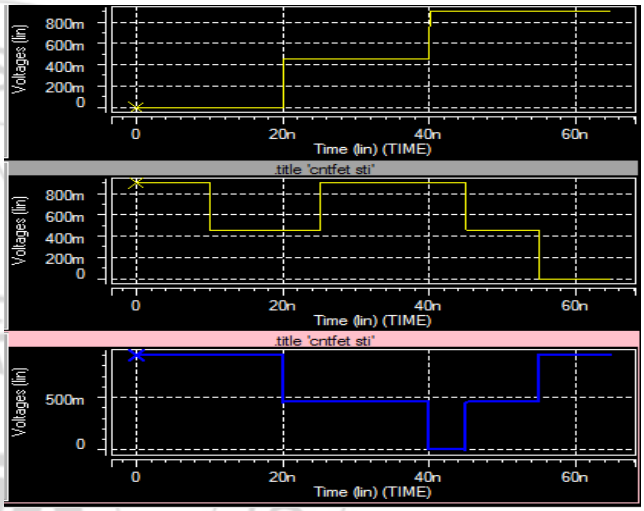


Figure 9: Simulation of Ternary NAND

4. Ternary Half adder

In order to design arithmetic circuit it is better to design decoder first. The three output of ternary decoder (xo, x1, x2) are either at logic 0 or else at logic 2. A ternary Decoder schematic and its response to input x is given below:

$$X_K = \begin{cases} 2 & if\ x = k \\ 0 & if\ x \neq k \end{cases}$$

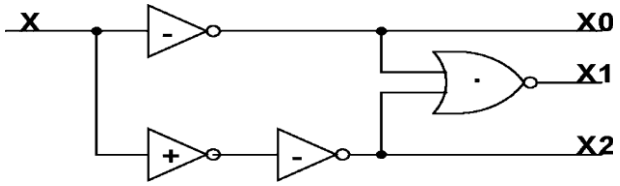


Figure 10: Ternary decoder Schematic

The buffer used in ternary adder is represented by logic as:

$$Out = \begin{cases} 1 & if\ in = 1, 2 \\ 0 & if\ in = 0 \end{cases}$$

Where in is the input at the buffer while out is the output through it. Ternary half adder [11] has two inputs A and B respectively and two outputs namely sum and carry respectively. The decoders here provide the unary output

signal for the inputs A and B. The truth table and characteristic equation obtained is given as [1]:

Table 4: Truth table of half adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	1	2	0
1	2	0	1
2	2	1	1

Sum= $A_2B_0+A_1B_1+A_0B_2+ 1.(A_1B_0+A_0B_1+A_2B_2)$
Carry= $1.(A_2B_1+A_1B_2+A_2B_2)$

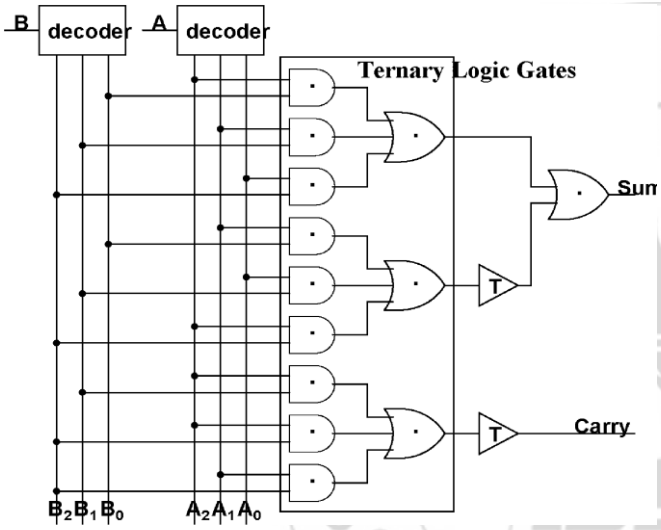


Figure 11: Ternary half adder

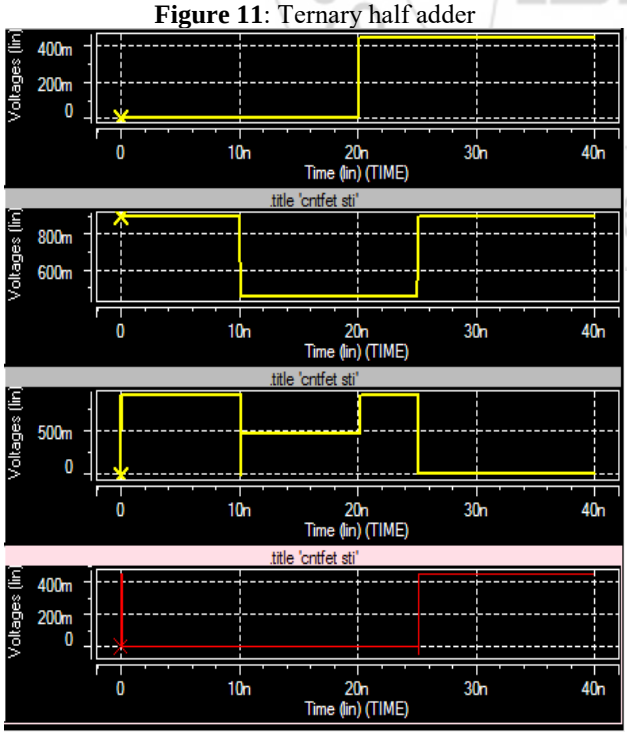


Figure 12: Simulation of HA

5. Future Work

From the study it was found that CNTFET is the promising alternative to counter the scaling down problem in conventional Si-MOSFET. Moreover it has good transport property and high on-off current ratio thereby making it suitable for low-power and high performance designs. In future, we will design full adder, SRAM etc using ternary logic based CNTFET.

6. Conclusion

The ternary inverters, NAND, NOR and Half adder design simulation is performed using Hspice. The simulation shows high performance at low power voltage supply. The power dissipation across ternary half adder is 0.32µW and the delay across sum and carry are 66.64psec and 47.92psec respectively.

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