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# A Novel Design of Low Power 4:2 Compressor using Adiabatic Logic

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**Abstract:** ***The purpose of the project is to design an adiabatic logic based low power 4:2 Compressor on the application of "Two Phase Clocked Adiabatic Static Logic (2PASCL) technique", which shows the lowest power dissipation between different adiabatic logic families. It works on the principle of charge reversible logic. The present technique has smallest power dissipation relative to the standard CMOS design style by using different design specification such as different input signal switching frequency and supply voltage. The simulation is performed on S-edit of Tanner tool at 90nm BSIM4 technology.***

**Keywords:** Adiabatic logic, Sinusoidal power supply, two phase power clock, energy recovery logic, 2PASCL technique, S-edit, Odd detector, compressor

## 1. Introduction

Now days, the movable devices are increasingly used by the everyday life. There is a continuous increase in these portable equipments, such as laptops, cell phones etc. With the gradual increase in complexity and functionality of these portable devices, the power dissipation will also increase. There are various sources of power dissipation in digital CMOS circuits such as switching power, leakage power and short circuit power dissipation. This power dissipation can be reduced by reducing the supply voltage, power gating and multi-threshold libraries. But this technique is not sufficient to fulfill today's power needs, hence another approach can be used to reduce power dissipation that is called as Adiabatic Logic. In this technique, oscillating power supplies may be utilized instead of constant supply voltage and charge stored in an output capacitor is reused instead of charge expending as in a conventional CMOS circuit. Hence, the total energy can be conserved.

## 2. Adiabatic 2PASCL Technique

The word "Adiabatic" is used in thermodynamics system that does not transfer energy to the environment, so that charge transfer out of the module is comparable to zero. But in everyday growth of computing, such optimal process cannot be possible because of the existence of dissipative elements like resistances in a circuit. Therefore, the Adiabatic logic is used in ultra low power purpose for which conventional energy is confined and speed is not critical such as bio-medical, robotics, space, deep sea, etc [1].

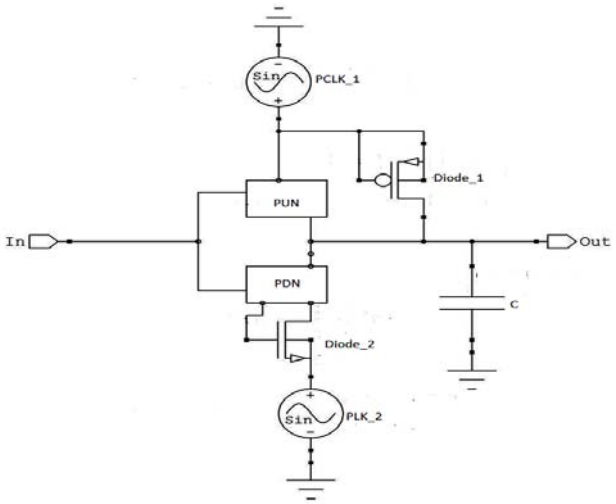


**Figure 1:** basic 2PASCL adiabatic circuits

From Fig. 1 the construction of 2PASCL logic based circuits consists of two powers clock PCLK_1 and PCLK_2 respectively and there is one eighteen degree phase reversal among consecutive power clocks. The above circuit also contains two diodes in its construction where Diode_1 is connected with PCLK_1 and output terminal and Diode_2 is connected with PDN and PCLK_2, so that both diodes enhance the discharging velocity of internal signal nodes. The operation of adiabatic 2PASCL circuits can be divided into two phases. In charging phase, when the intake voltage is low then PUN is in ON state and PDN is in OFF state which results in charging the output load capacitor equal to the supply voltage. The charging phase is illustrated in Fig. 2.

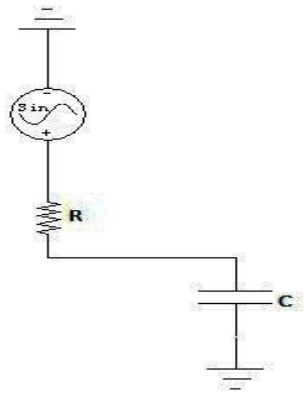


**Figure 2:** Charging in 2PASCL adiabatic logic

During discharging phase, when the input signal is high then PDN is ON and PUN is in OFF state which result in charge reserved in the output load capacitor can be retrieve instead of dissipated, in the conventional CMOS technique. The discharging phase is illustrated in Fig. 3.

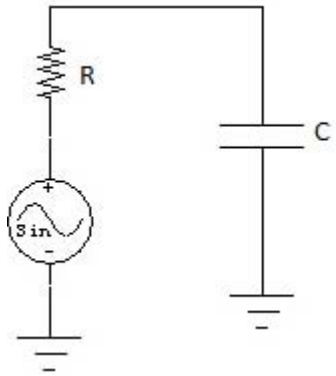


**Figure 3:** Discharging in 2PASCL adiabatic logic

## 3. Multiplexer

A multiplexer is also abbreviated as "MUX". It is a combinational logic circuit that consists of several input lines, select lines and a single output line. A single input line can be routed to the output line by choosing a proper combination of select lines. Multiplexers are similar to a speedily moving multiple position rotary switch which controls multiple input lines one at a time to the output.

### 3.1 2 to 1 line Multiplexer:

A 2 to 1 line multiplexer has two inputs but a single output. Under control of single selection line, one of the input signals is passed to the output. Fig. 4 shows the schematic symbol of 2 to 1 line multiplexer. The truth table of 2 to 1 line multiplexer is given in Table 1

**Table 1:** Table of 2 To 1 Line Multiplexer

| Select line | Data output |
|---|---|
| $S_0$ | $I_0$ |
| $S_1$ | $I_1$ |

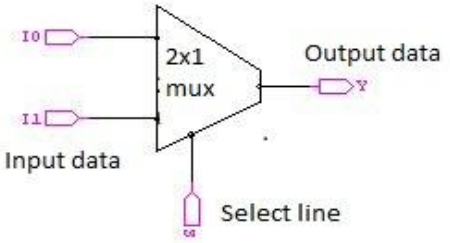


**Figure 4:** Symbol of 2 to 1 line multiplexer

From the propositional function, the output logic can be expressed as min-terms and are given below in Eq. 1.

$$Y = \bar{S}_0 I_{0+} S_1 I_1 \quad (1)$$

Where I and S are data input and select line respectively.

## 4. Exclusive – Or (EX-OR) Gate

The logical operation of a two-input EX-OR gate is that its output is at logic high, only when one of its inputs is high. Under the conditions, when both the inputs have the logic 0 state, or when both the inputs have the logic 1 state, the output has a logic 0 state. It is called an Anti-coincidence or Inequality Detector.

The input variables are represented by A and B and the output variable is represented by X. The output expression of this gate is written as given in Eq. (2).

$$X = A\bar{B} + .\ B = A \oplus B \quad (2)$$

The schematic symbol of EX-OR gate is illustrated in Fig. 5. And the truth table of EX-OR gate is given in Table II.

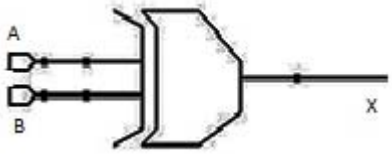


**Figure 5:** Symbol of EX-OR gate

**Table 2:** Truth Table Two Input ex-or gate

| Inputs | | Output |
|---|---|---|
| A | B | $X = A\bar{B} + .B$ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## 5. Compressor

Compressors are the basic building blocks of high accuracy and high speed multipliers, arithmetic and digital signal processing (DSP) applications. A 4:2 compressor consists of five inputs namely $X1$, $X_2$, $X_3$, $X_4$ and $C_{IN}$. It produces a sum bit (S), a carry bit (C), and a carry propagate bit (Cout). The Carry bit from position to right is denoted as $C_{IN}$, while the carry bit into higher position is denoted as Cout. To avoid carry propagation the value of $C_{OUT}$ depends only on $X_1$, $X_2$,

$X_3$ and $X_4$. It is independent of $C_{IN}$ the block diagram is shown in Fig. 6 [2].

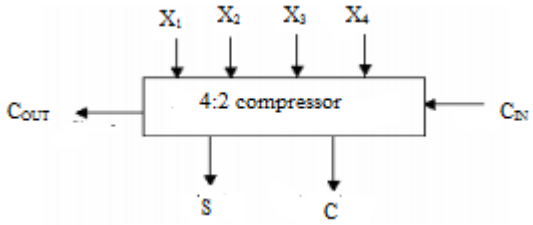


**Figure 6:** Symbol of 4:2 Compressor

The 4:2 compressor could be realized by different combinations of EX-OR gates and multiplexers. It is composed of six modules: four 2-input EX-OR gates and two 2 to 1 line multiplexers. The logic level decomposition is shown in Fig. 7.

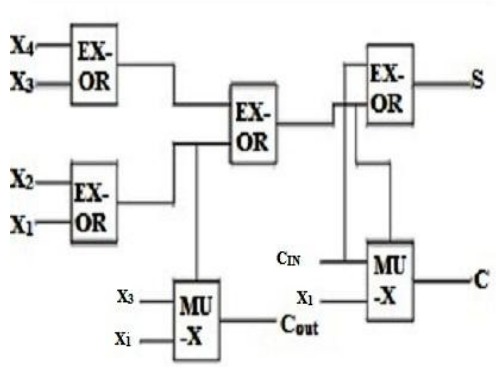


**Figure 7:** Logic level decomposition of 4:2 compressors

The output expression of 4:2 compressor are given by the following equations.

$$S = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{IN} \quad (3)$$

$$C = (X_1 \oplus X_2)\, X_3 + (X_1 \oplus X_2)\, X_1 \quad (4)$$

$$C_{OUT} = (X_1 \oplus X_2 \oplus X_3 \oplus X_4)\, C_{IN} + (X_1 \oplus X_2 \oplus X_3 \oplus X_4)\, X_4 \quad (5)$$

**Table 3:** Truth Table of 4:2 Compressors

| inputs | | | | $C_{IN}=0$ | | $C_{IN}=1$ | | $C_{OUT}$ |
|---|---|---|---|---|---|---|---|---|
| $X_1$ | $X_2$ | $X_3$ | $X_4$ | C | S | C | S | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | | | | | |
| 0 | 1 | 0 | 0 | | | | | |
| 1 | 0 | 0 | 0 | | | | | |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | | | | | |
| 1 | 1 | 0 | 0 | | | | | |
| 0 | 1 | 0 | 1 | | | | | |
| 1 | 0 | 1 | 0 | | | | | |
| 1 | 0 | 0 | 1 | | | | | |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | | | | | |
| 1 | 1 | 0 | 1 | | | | | |
| 1 | 1 | 1 | 0 | | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

## 6. Design of 4:2 Compressor

The 4:2 compressor can be designed by using 2 to 1 line multiplexer and two input EX-OR gate by the application of CMOS and 2PASCL logic technique given in below figures.

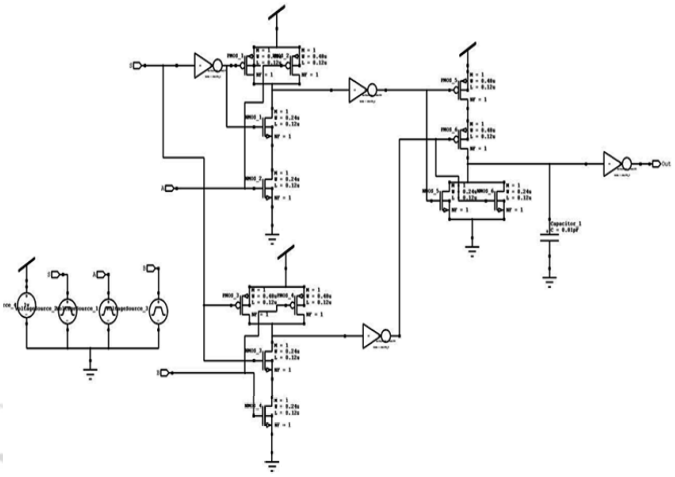

**Figure 8:** Schematic of 2 to1 line multiplexer using CMOS logic

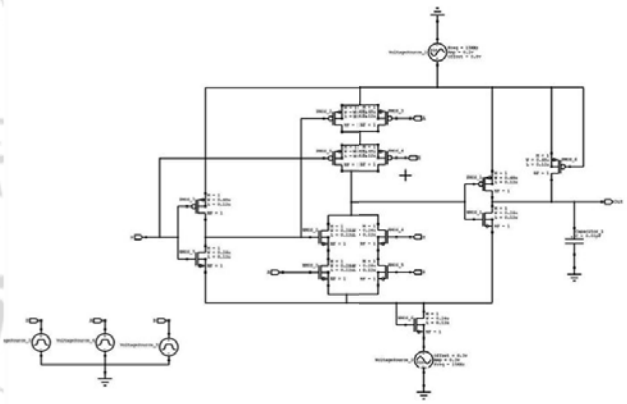

**Figure 9:** Schematic of 2PASCL logic based 2 to 1 line multiplexer

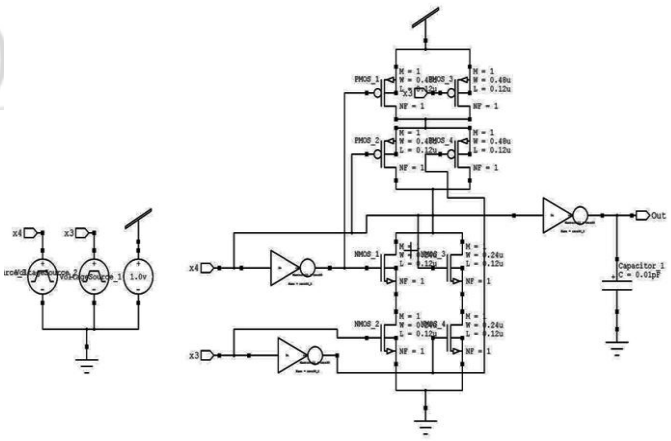

**Figure 10:** Schematic of EX-OR gate using CMOS logic

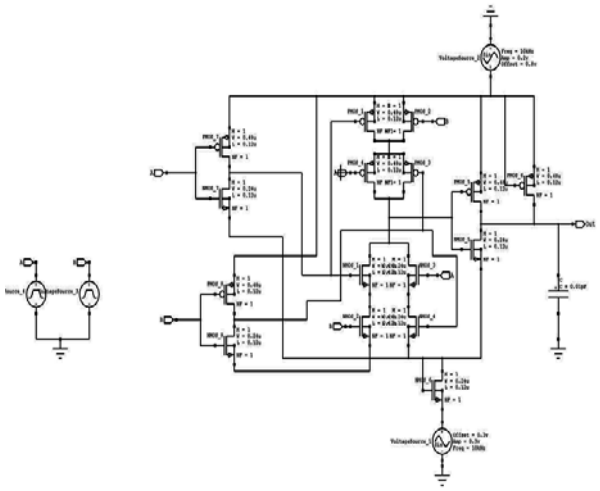

**Figure 11:** Schematic of 2PASCL logic based EX-OR gate

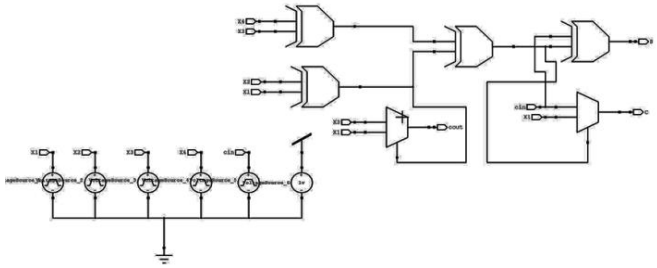

**Figure 12:** 4:2 Compressor by using CMOS logic

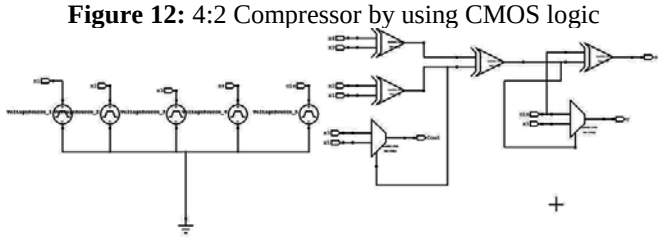

**Figure 13:** Adiabatic 2PASCL logic based 4:2 Compressors

## 7. Simulation Results

The simulation is performed on Tanner EDA tool using 90nm technology. The Tanner tool consists of S-edit, T-spice, W-edit tools. S-edit is a schematic entry tool that is used to verify the circuits, T-Spice provides the simulation of the circuits and W-edit provides the real time waveform viewing. Below figures show the simulated waveform of 2 to 1 line multiplexer, EX–OR gate and 4:2 compressor using conventional CMOS and 2PASCL logic respectively.

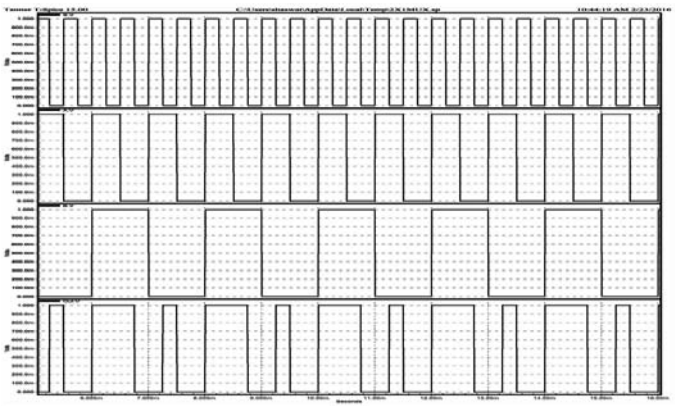

**Figure 14:** Simulation waveform of 2 to 1 line multiplexer using CMOS logic

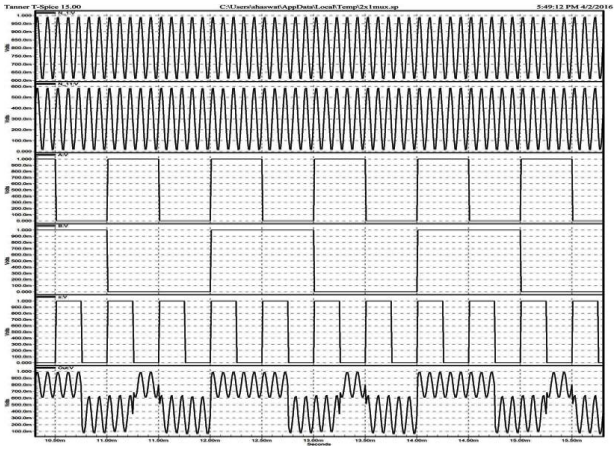

**Figure 15:** Simulation output waveform of 2 to 1 line multiplexer using 2PASCL logic

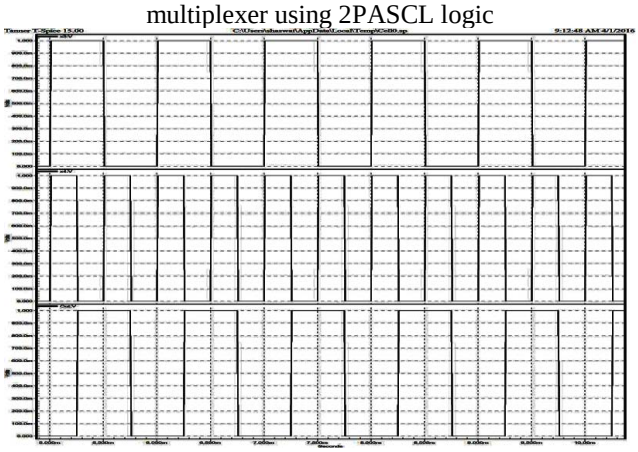

**Figure 16:** Simulated waveform of EX – OR gate using CMOS logic

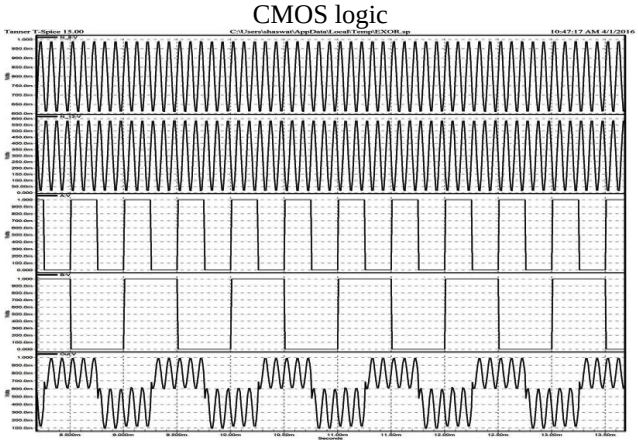

**Figure 17:** Simulated waveform of EX-OR gate using 2PASCL logic

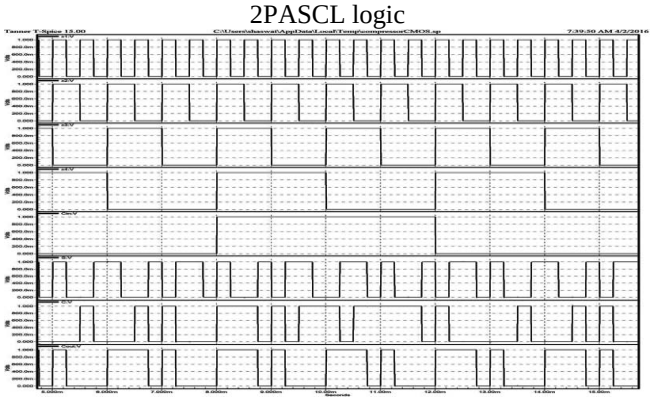

**Figure 18:** Simulated waveform of 4:2 compressor using CMOS logic

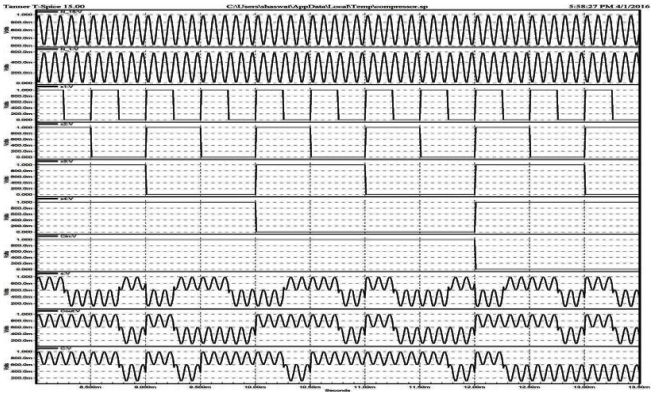

**Figure 19:** Simulated waveform of 4:2 compressors using 2PASCL logic

## 8. Comparison of Results

**Table 4:** Comparison of Proposed and CMOS Logic Based 2 To 1 Line Multiplexer

| Logic families | Change in supply voltage | Average power dissipation | Change in input frequency | Average power dissipation |
|---|---|---|---|---|
| CMOS | 1.2V | 3.24µW | 2KHz | 0.523 µW |
| | 1.4V | 14.4 µW | 5KHz | 0.544 µW |
| | 1.6V | 57.9 µW | | |
| | 1.8V | 130.6 µW | 10KHz | 1.19 µW |
| | 2.0V | 201.8 µW | | |
| 2PASCL | 1.2V | 3.22 nW | 2KHz | 0.76 nW |
| | 1.4V | 8.71 nW | 5KHz | 0.86 nW |
| | 1.6V | 78.3 nW | | |
| | 1.8V | 953.06 nW | 10KHz | 0.94 nW |
| | 2.0V | 2377.5 nW | | |

In Table 4, the proposed logic based multiplexer can save 99.92% And 98.82% of power with respect to CMOS logic based multiplexer at 10KHz input frequency and 2.0V supply voltage respectively.

**Table 5:** Comparison of Proposed And CMOS Logic Based EX-OR Gate

| Logic families | Change in supply voltage | Average power dissipation | Change in input frequency | Average power dissipation |
|---|---|---|---|---|
| CMOS | 1.2V | 4.41 µW | 2KHz | 0.3 µw |
| | 1.4V | 18 µW | 5KHz | 0.76 µw |
| | 1.6V | 69.2 µW | | |
| | 1.8V | 160 µW | 10KHz | 1.50 µw |
| | 2.0V | 288 µW | | |
| 2PASCL | 1.2V | 40 nW | 2KHz | 1.64 nw |
| | 1.4V | 2109.2 nW | 5KHz | 2.33 nw |
| | 1.6V | 8909.6 nW | | |
| | 1.8V | 9322 nw | 10KHZ | 3.60 nw |
| | 2.0V | 10191.4 nw | | |

In Table 5, the proposed logic based EX-OR gate can save 99.76 % and 96.46% of power with respect to CMOS logic based EX-OR gate at 10KHZ input frequency and 2.0V supply voltage respectively.

**Table 6:** Result of 4:2 Compressor Using CMOS And 2PASCL Logic

| *Logic families* | *Change in supply voltage* | *Average power dissipation* | *Change in input frequency* | *Average power dissipation* |
|---|---|---|---|---|
| CMOS | 1.2V | 7.19 µW | 2KHz | 0.422 µW |
| | 1.4V | 45.1 µW | 5KHz | 1.02 µW |
| | 1.6V | 206.4 µW | | |
| | 1.8V | 491.9 µW | 10KHz | 2.01 µW |
| | 2.0V | 895.3 µW | | |
| 2PASCL | 1.2V | 128 nW | 2KHz | 8.16nW |
| | 1.4V | 6065.0 nW | 5KHz | 10.01 nW |
| | 1.6V | 30224.4 nW | | |
| | 1.8V | 31866.5 nW | 10KHz | 12.4 nW |
| | 2.0V | 35082.0 nW | | |

In Table 6, the proposed logic based 4:2 compressor can save 99.38% And 96.08% of power with respect to CMOS logic based 4:2 compressor at 10KHz input frequency and 2.0V supply voltage respectively.

## 9. Conclusion

From the results, it is concluded that the 2PASCL logic based 4:2 compressor is more energy efficient as compared to CMOS logic based compressor. The proposed compressor has power saving of 99.38% and 96.08% respectively as compared to static CMOS logic based 4:2 compressor at 10 KHz input signal frequency and 2.0V supply voltage.

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