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Review of Fully Reused VLSI Architecture of Channel Encoding Using SOLS Technique for DSRC Applications

Supriya S. Garade[1], P. R. Badadapure[2]

[1]Pune University, Department of ENTC ICOER, Wagholi Pune, Maharashtra India

[2]Professor, Pune University, Department of ENTC ICOER, Wagholi Pune, Maharashtra India

Abstract: ***Dedicated short-range communications are one-way or two-way short-range to medium-range wireless communication channels specifically designed to push the intelligent transportation system into our daily life. So I am processing the fully reused VLSI architecture of FM0 and Manchester encoding using SOLS technique for DSRC application. The DSRC standards generally use FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both encodings. The similarity-oriented logic simplification (SOLS) technique is implemented to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both encodings. In this we also compare our method with other techniques This experiment also exhibits an efficient performance compared with the existing works.***

Keywords: Dedicated short-range communication, FM0, Manchester

1. Introduction

DSRC communication implemented fundamentally on standards based interoperability among devices from different manufacturers. The dedicated short-range communication is a technique for one- or two-way medium range communication especially for intelligent transportation systems. The DSRC can be briefly divided into two categories: vehicle-to-vehicle and vehicle-to- roadside. The primary aim for deploying DSRC is to enable collision prevention applications. These applications depend on frequent data exchanges among vehicles, or between vehicle and roadside infrastructure. The U.S.Department of Transportation (DOT) has conclude that vehicle-to-vehicle (V2V) communication based on DSRC can address up to 82% of all crashes in the United States involving unimpaired drivers, potentially saving thousands of lives and billions of dollars. The National Highway Traffic Safety Administration (NHTSA) within the U.S. DOT plans to decide in 2013 whether to use rules to require or encourage deployment of DSRC equipment in new vehicles in the U.S.

In vehicle-to-vehicle, the DSRC activated the message sending and broadcasting among vehicle for safety issues and public information announcement. The Safety issues consist of blind-spot, intersection warning, intercars distance, and collision-alarm. The vehicle-to-roadside focuses on the intelligent transportation service, such as automatic electronic toll collection (ETC) system. With ETC, the toll collecting is electrically or automatically accomplished with the contactless IC-card platform. Moreover, the ETC has application such as payment for parking-service, and gas-refueling. Thus, the DSRC plays an important role in automobile industry.

The DSRC standards have been implemented by several organizations in different countries. These DSRC standards are shown in Table I.

Table 1: DSRC Standards

	Europe	America	Japan
Organization	CEN[1]	ASTM[2]	ARIB[3]
Data Rate	500 kbps	27 Mbps	4 Mbps
Carrier Frequency	5.8GHZ	5.9GHZ	5.8GHZ
Modulation	ASK,PSK	OFDM	ASK
Encoding(Downlink)	FMO	Manchester	Manchester

[1] European Committee for Standardization.
[2]American society for Testing and Materials.
[3]Association of Radio Industries and Businesses.

The data rate individually targets at 500 kbps, 27 Mbps, and 27 Mbps with carrier frequency of 5.8 and 5.9 GHz. The modulation methods includes such as amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the Waveform of transmitted signal is expected to have zero mean for robustness noise, and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, (1 or 0) which is difficult to obtain dc-balance. The goal of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely designated in encoding for downlink.

The encoding techniques used in communication convert information into a suitable form for transmission. Encoding techniques can also be used for security purposes. In general, different types of encoding techniques can be used for serial communication application. There are several types to encode the data such as Miller encoding, Manchester encoding, FM0, NRZ, FM1, RZ, etc. This type of encoding techniques is used on the transistor level, so it can be used

with optical communication as well as minimizing the critical path, area, delay, and buffer size by adding a minimum number of buffers. A baseband processor consist of a UHF RFID Reader, PIE encoder, FM0 decoder, or Miller decoder are used for encoding and decoding purposes application, achieving higher efficiency and accuracy. But in order to do this, it needs to have a high frequency clock. The system architecture of DSRC transceiver is shown in Fig 1.

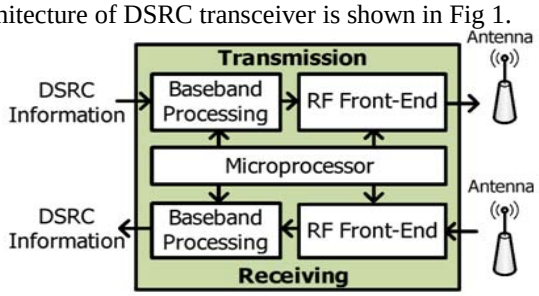

Figure 1: DSRC Transceiver

The upper and bottom parts are designed for transmission and receiving, respectively. This transceiver is partitioned into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor takes and manipulate the instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is dedicated for modulation, error correction, clock synchronization, and encoding. The RF front-end transmits and receives the wireless signal through the antenna for communication.

2. Literature Survey

In last few years VLSI architecture of Manchester encoder is used for optical communications [1]. A new Manchester code generator designed at transistor level is represented. This Manchester code generator uses 32 transistors and has the same complexity as a standard D flip-flop. It is intended to be used in a complex optical communication. The main advantage of this design is to use a clock signal running at the same frequency as the data. Output changes on the rising edge and falling edge of the clock signal. This design is realized with full-custom. This design consist of the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by 0.35-μm CMOS technology and it‟s operated on 1 GHz frequency.

Optical Technology is now widely used in telecommunications, providing bandwidth far beyond the physical limits of electronics and paying the way for the explosive growth of the internet application. As bandwidth demands in institutional intranets have increased to the disadvantage of electronic, interconnection & optical systems (Gigabit Ethernet, Fiberchannel) have also found their way into local area networks (LANs). The research effort on optoelectronic interconnections has increased to a significant progress on component level including the tight integration of opto-electronic I0s and silicon chips, novel micro optical devices and advances in opto-mechanical integration. These interconnections are a better substitute to electrical ones which are limited by chip IO restrictions, interconnection complexity restrictions, fanout and fan-in limits of high performance electronic links. Conflict detection is one of the major problem in systems using optical fan-in, especially when unmodulated signals are used such as NRZ signals. Modulation codes are widely used in data transmission communication systems, magnetic recording, and fiber optic data links. The Manchester code is a very popular code as it is level insensitive, self clocking, and it provides signal absence detection as the coded signal has always at least one transition per bit.Hence, we propose a new design of such an encoder, running at almost the same frequency as a standard D flip-flop, but without the need of resetting the initial state. The encoder is designed at transistor level and uses transfer gates, inverters, and gated inverters. As a result, on the rising edge of the clock signal, the input is transmitted to the output, while on the falling edge of the clock signal, the output is inverted .The delay between the edge of the clock and the output change is the propagation time through inverters. The difference between these two delays can be reduced by adjusting correctly the transistor size. When the inverters delays are much smaller than the clock period, this difference can be neglected or ignored. The transistor size of each inverter has to be optimized in order to ensure correct behavior of encoder. If the transistors size is decreased would lead to an increase in the propagation time of the inverters while increasing their sizes would enlarge the capacitance load of preceding ones and so increase their propagation times. The maximum clock frequency for this circuit is 1 GHz as the output duty cycle is influenced by the gates propagation delays. At the 1GHz frequency, using a 50% duty cycle clock signal lead to a generated output duty cycle of 38% for the worst case process corner and 48% for the best case .A Manchester decoder has also been designed but it is not presented. This decoder is compatible with the worst case duty cycle, which validated the design of the Manchester encoder.

The VLSI architecture of Manchester encoder [2] further replaces the architecture of switch in [1] by the NMOS device. It is realized in 90-nm CMOS technology, and the maximum clock frequency is as high as 5 GHz. A Manchester code generator designed at transistor level uses NMOS switches. This Manchester generator uses 26 transistors and has the same complexity as a standard D flip-flop. It is implemented to be used in a complex optical communication system. The main advantage of this design is the use of a clock signal running at the same frequency as the data. Output changes on the rising edge and falling edge of the clock signal. The circuit has been designed in a 90 nm UMC CMOS technology to increase the efficiency. The CMOS wideband switches are designed primarily to statisfy the requirements of devices transmitting at ISM (industrial, scientific, and medical) band frequencies. The low insertion loss, the high isolation between ports, the low distortion and the low current consumption of these devices make them an excellent solution for many high frequency applications that requires low power consumption and the ability to handle transmitted power up to 16 dBm, such as car radios, antenna switching, wireless metering, high speed filtering and data routing, home networking, power amplifiers and PLL switching. To improve their bandwidth, CMOS wideband switches uses only N-channel MOSFETs in the signal path. An NMOS only switch has to be twice the bandwidth

performance of a standard switch with NMOS and PMOS FETs in parallel. Due to removal of the P-channel MOSFET resulting in smaller switch size and greatly reduced parasitic capacitance. N-channel MOSFETs act as voltage controlled resistors. The Performance evaluation shows a correct behaviour up to 5 Gbit/s data rate is achieved showing the right operation of the switches and the high wideband function of the specific encoder. At typical case in 2.4GHz frequency, a 66ps propagation time and a 45.7% duty cycle are reached. Without changing the size of transistors, a 138ps propagation time and a 42% duty cycle are reached at typical case in 5GHz. These results are quite good but not the best. The proper identification of transistors‟ dimensions to obtain best propagation time and duty cycle above 5 GHz, is under investigation.

The high-speed VLSI architecture almost fully reused with Manchester and Miller encodings [3] for radio frequency identification (RFID) applications is implemented. This design is realized in 0.35-μm CMOS technology and has the maximum operation frequency is 200 MHz. This design uses concept of parallel operation to improve data throughput. In addition, the technique of hardware sharing is improved in this design to reduce the number of transistors. This design uses TSMC CMOS 0.35-µm 2P4M technology. The average power consumption of this circuit under room temperature is 549 µW. The total core area of circuit is 70.7 µm × 72.2µm. This circuit can be easily integrated into Radio Frequency Identification (RFID) application. Based on the previous proposed architecture, this design adopted the concept of parallel operation to improve data throughput. Due to the convenience and economic benefits, radio frequency identification (RFID) applications have been greatly utilized in recent years. RFID is not a new technique. The earliest invention was applied to identify military aircrafts during the Second World War. Along with technical growth and continuous improvement, RFID appears in new fields and derives more new applications, such as in human tracking or biomedicine (with a sensor). In RFID system, the data communication through modulation is transmitted between the tag and reader. In order to reduce error rate, gaining DC balance and improve efficiency, the data is encoded before being modulated. In general, the Manchester and Miller codes can be applied to telecommunication and then used in the RFID system. The Miller code itself carries „timing‟ information, which can be extracted the clock signal information in other site, that is, the code with a self-timing property. Therefore, the Miller code has better improvement against delay error and noise interference.

A Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator [4] is designed. This hardware architecture is constructed from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum clock frequency of this design is about 256 MHz. In this encoding design presented RTL design of Manchester encoder. FSM based Manchester encoder schematic occupies very less number of hardware thus minimizing the area on the FPGA .RTL based Manchester encoder design uses more number of gates and FFs, which in turn maximize the area on the FPGA device. FSM approach is efficient in design Manchester encoder as compared to RTL. FSM based design operates at higher frequency thus maximizing the speed of the encoder. The complete circuit has been designed using Verilog Hardware Description Language. The similar design methodology is further used to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator.

3. Conclusions

Here I have given the paper on literature survey of VLSI architecture encoding techniques for various applications. In proposed system we use VLSI architecture of FMO/ Manchester encoding using SOLS technique and also compare this technique with other techniques.

However, the coding-diversity between both encoding seriously limits the potential to design a VLSI architecture that can be fully reused with each other. In this paper we proposes a VLSI architecture design using similarity-oriented logic simplification (SOLS) technique. The SOLS technique reduces the limitation on hardware utilization by two core techniques. The SOLS consists of two core methods such as area-compact retiming and balance logic-operation sharing. The area-compact retiming technique relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing technique efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture. With SOLS technique, we constructs a fully reused VLSI architecture of Manchester and FM0 encodings for DSRC applications. This paper not only implement a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing techniques.

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Author Profile

Miss. S. S. Garade has Completed B.E in Electronics And Tele-Communication in Gharda College of Engineering Khed and pursuing ME in ICOER JSPM Wagholi, Pune.

Prof. P. R. Badadapure, Head of Department in ICOER JSPM Wagholi, Pune.