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Adiabatic Logic Circuits for Low Power VLSI Applications

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Abstract: ***The power dissipation has become a major design issue in VLSI circuits. As the system size is shrinking gradually it has become one of the prime concerns for the designers. The power dissipation can be reduced by introducing different design techniques. In this paper a new adiabatic approach 2PASCL has been introduced. The power dissipation in adiabatic circuits can be minimized more than 90% as compared to conventional CMOS logic. In adiabatic circuit the charge stored in load capacitor is recovered while in conventional CMOS it is transferred to ground which causes wastage of energy.***

Keywords: static CMOS, adiabatic logic, energy dissipation, 2PASCL, energy recovery.

1. Introduction

The design of low power circuits is one of the important concerns in VLSI design. Initially it was not a major issue but as the system size is reducing from last few years it has become important for designers. The growing demand for portable electronic devices like mobiles, computers require energy efficient power sources with small size. Although CMOS devices are very Power friendly but minimization of dynamic power dissipation is a big challenge. During charging transfer of charge occurs between V_{dd} and the load capacitance C_L i.e. an energy of $E = C_L V_{dd}^2$ is transferred from V_{dd} to C_L. Energy stored in load capacitor:

$$E_{stored} = \frac{1}{2} C_L V_{dd}^2.$$

$$E_{charge} = E_{discharge} = \frac{1}{2} C_L V_{dd}^2$$

Adiabatic technique is one of the energy efficient technologies for low power VLSI designs. Adiabatic logic works on the charge recovery principle by which energy is recycled instead of dissipation.

2. Operation of Adiabatic Logic

The term ADIABATIC is originated from Greek word that is used to describe the thermodynamic process in which no exchange of energy occurs between the system and the external environment. But in practical computing such ideal condition can not be achieved due to the presence of dissipative elements like resistances. However one can achieve very low power dissipation by reducing the speed of operation and only switching transistors under certain conditions. The adiabatic logic is also known as ENERGY RECOVERY CMOS [1]. In literature, there are two types of adiabatic circuits presented one is full adiabatic and other is quasi-adiabatic or partial adiabatic circuits. In most practical cases two type of dissipation occurs in adiabatic circuit adiabatic loss and non adiabatic loss. Adiabatic loss occurs by switching resistances of transistor when a current flow through the transistor and the non adiabatic loss occurs due to threshold voltage.

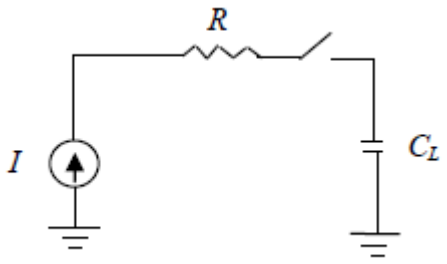


Figure 1: Adiabatic Logic Circuit [1]

Here the load capacitance is charged by the constant current source while in conventional CMOS constant voltage source is used. Here R is the resistance PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume the capacitor voltage is initially zero.

The Voltage across the switch= IR

P(t) in the switch=I^2R ..... (1)

Energy during charge $E = (I^2R)$T ..... (2)

Also $Q = C_L V_{dd}$, $I = \frac{C_L V_{dd}}{T}$

E = (I^2R) T = $\left(\frac{RC_L}{T}\right) C_L V_{dd}^2$ ..... (3)

Where E is the energy dissipated during charging time,
Q is the charge transferred to the load,
C is the value of the load capacitance,
R is the on-resistance of the PMOS switch,
V is the final value of the voltage at the load,
T is the charging time.

Theoretically the energy dissipation is nearly zero when the switching time of the driving voltage is long. When $V_\emptyset$ goes from HIGH to LOW discharging process takes place through the NMOS. The energy dissipation can be minimized by increasing the switching time. The energy dissipation is proportional to R. Thus by decreasing the on-resistance of PMOS network will decrease the energy dissipation.

3. Adiabatic Logic Families

The adiabatic logic family can be divided in partial adiabatic and full adiabatic. Some charge is transferred to the ground in partial adiabatic circuit while in full adiabatic circuits all the charges are recovered. Adiabatic logic family consist of many design techniques like efficient charge recovery logic (ECRL), 2N- 2N2P adiabatic logic, Positive feedback adiabatic logic (PFAL), NMOS energy recovery logic(NERL), Clocked adiabatic logic(CAL), True single phase adiabatic logic(TSEL), Source coupled adiabatic logic(SCAL), Two phase adiabatic static clocked logic(2PASCL) and fully adiabatic logic families are Pass transistor adiabatic logic(PAL), Split Rail charge recovery logic(SCRL). But in this paper we are going through ECRL, PFAL, 2PASCL, 2N-2P, 2N-2N2P and CAL. By using these techniques inverter circuit has been designed. These designs show good improvement as compared to conventional CMOS in power dissipation.

A. ECRL

Efficient charge recovery logic (ECRL) [13] proposed by Moon and Jeong is shown in figure 2. Cross-coupled PMOS transistors are used in this design. An AC power supply pwr is used for energy recovery purpose. With the help of out and $\overline{out}$ a constant load capacitance is drived by the power clock. Due to the use of cross-coupled PMOS full output swing is found in both precharge recover phase. When the voltage on the supply clock reaches to |Vtp| the PMOS gets off and due to this the recovery path is disconnected which results in incomplete recovery. The ECRL circuits work on the principle of pipelining with four phase power clock.

The main disadvantage of ECRL is the occurrence of coupling effect, because two outputs are connected by the PMOS latch and two complementary outputs can interface each other.

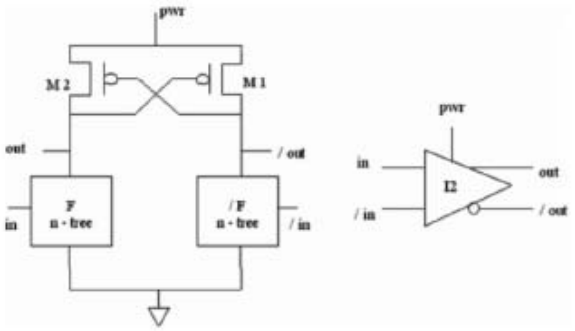


Figure 2: Efficient charge recovery logic proposed by Moon and Jeong

B. PFAL

The positive feedback adiabatic logic (PFAL) [15] works with lower energy consumption compared to others. The schematic of PFAL inverter [1] gate is shown in figure 2. It this design two cross coupled inverters are used in which NMOS connection is made between the output and the power clock. For the purpose of adiabatic charging a time varying source is used that is known as power clock which have four phases. Let us consider the case when input is high. Then transistors m5 and m1 are in on state when the value of power clock increases. Due to this out is connected to ground and $\overline{out}$ will follow the changes of power clock. When the power clock comes to V_{dd} , out will be zero and $\overline{out}$ will be V_{dd} which will act as input for the next stage. When power clock varies from V_{dd} to 0 then the energy will be recovered through the m1.

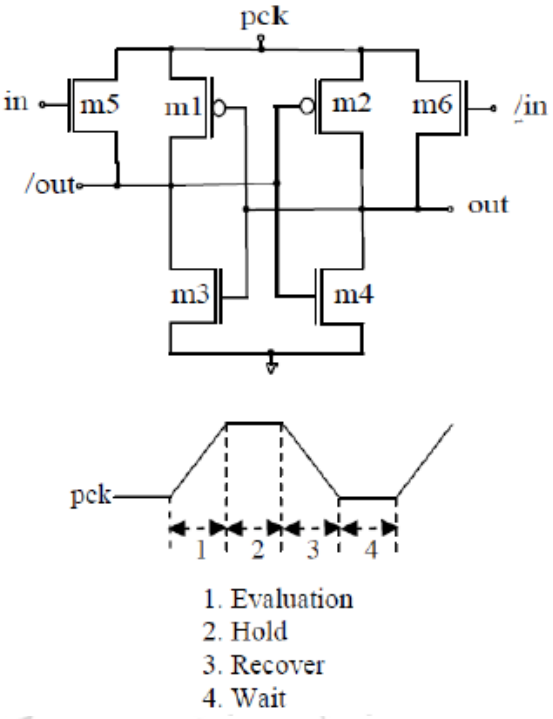


Figure 3: PFAL logic circuit

C. 2PASCL

The schematic of two phase adiabatic static clocked logic [6] is shown in figure 4. This circuit consists of two diodes for the energy recovery purpose and to improve the discharging speed of internal signal nodes. In which one is connected between output node and power clock and other is connected between the NMOS and the other power source. It works in two phases: Evaluation and Hold. In evaluation phase $V_{\emptyset}$ swings up and $\overline{V_{\emptyset}}$ swings down and in hold phase reverse process occurs. It is not necessary to occur the charging /discharging process after every clock cycle which results in minimum number of dynamic switching. It will suppress the node switching activities.

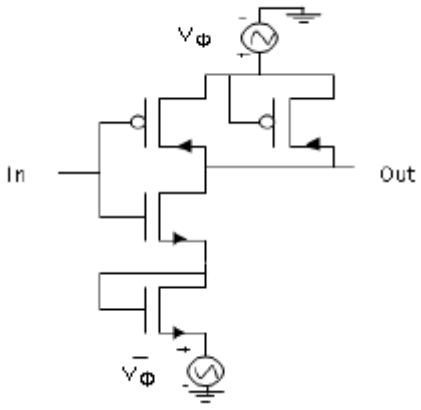


Figure 4: 2PASCL logic circuit

D. 2N-2P

The schematic of 2N-2P [1] is shown in figure 5. Initially input IN is high and $\overline{IN}$ is low. When power clock rises from 0 to V_{dd} the output _out' remains ground level and $\overline{out}$ will follow the changes of power clock. When the value of power clock comes to V_{dd} out and $\overline{out}$ are 0 and V_{dd} respectively and this is used as input for next stage. When the power clock goes from V_{dd} to 0 the output $\overline{out}$ will return the stored energy to power clock.

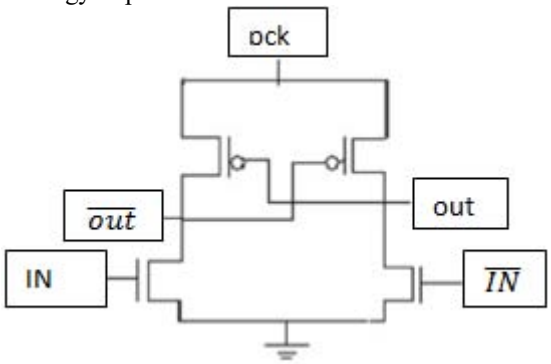


Figure 5: Schematic of 2N-2P inverter

E. 2N-2N2P

To reduce the coupling effect in 2N-2P a new technique 2N-2N2P [1] was introduced. In 2N-2P the latch is designed by only two PMOSFETs while in 2N-2N2P technique two PMOSFETs and two NMOSFETs are used. The additional cross coupled NMOSFET switches results in a non floating output for a large part of the recovery phase. The schematic of 2N-2N2P inverter [1] is shown in figure 6. In this technique four phase clocking is used i.e. _evaluation', _hold', _recover' and _wait'.

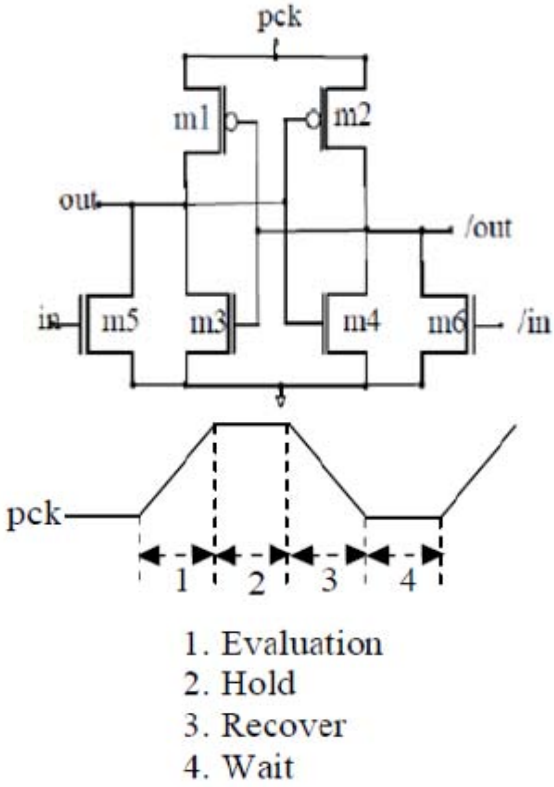


Figure 6: Schematic of 2N-2N2P inverter and power clock

F. CAL

Clocked Adiabatic Logic is a dual rail logic which is operated from a single phase AC power clock supply [17]. The on chip switching and a small external inductor are used to generate the power clock supply waveform in adiabatic mode. The schematic of basic CAL gate inverter is shown in figure 7. It consists of cross coupled inverters to provide memory function. An auxiliary timing control clock signal CX has been used. This has been introduced to control the transistors that are in series with the logic trees represented by the functional blocks F and /F. The clocked enable devices allow operation with a single power clock.

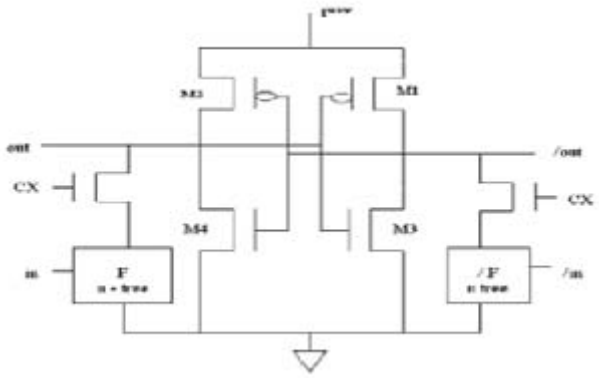


Figure 7: The basic CAL gate- the inverter

4. 2PASCL based basic logic gates

The partial adiabatic 2PASCL NAND gate [9] schematic and energy dissipation compared to conventional NAND gate are shown in figure 8. Power dissipation in this design is reduced upto 97% compared to conventional NAND gate.

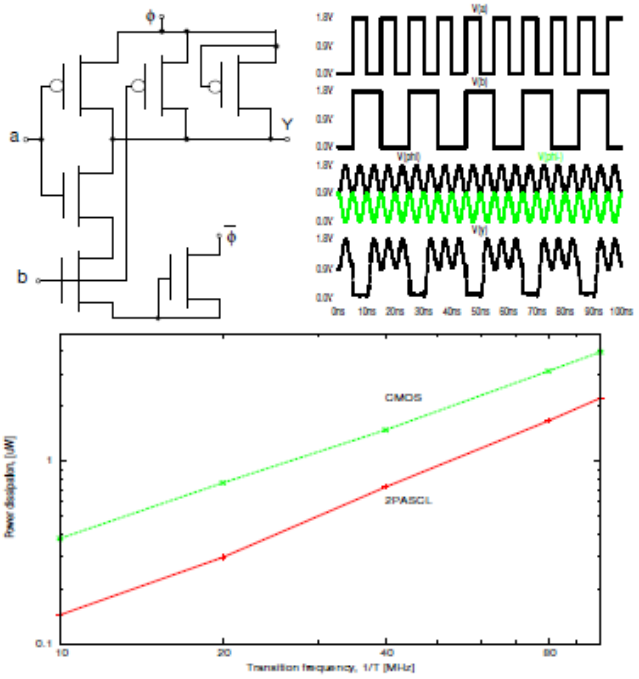


Figure 8: 2PASCL- based NAND logic and waveform from simulation at 100MHz

The schematic of 2PASCL NOR gate and energy dissipation comparison is shown in figure 9. It show reduced power dissipation as compared to conventional NOR gate.

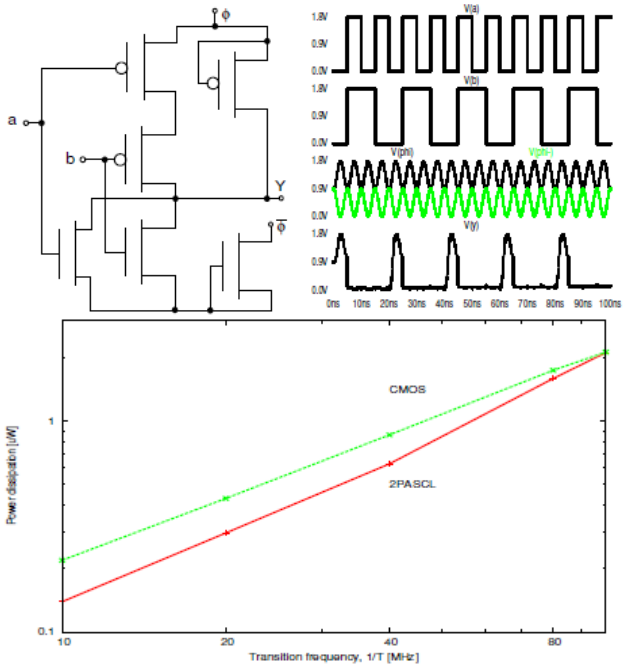


Figure 9: 2PASCL based NOR logic and waveform from simulation at 100MHz

An adiabatic 2PASCL XOR gate schematic and energy dissipation comparison with conventional NOR gate are shown in figure 10.

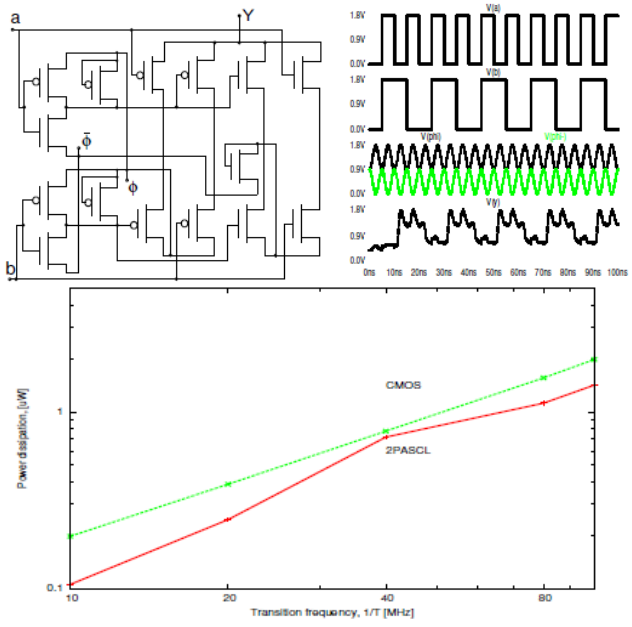


Figure 10: 2PASCL based XOR logic and waveform from simulation at 100MHz

The schematic of 2PASCL inverter circuit is shown in figure 11. It show power dissipation reduction compared to conventional design.

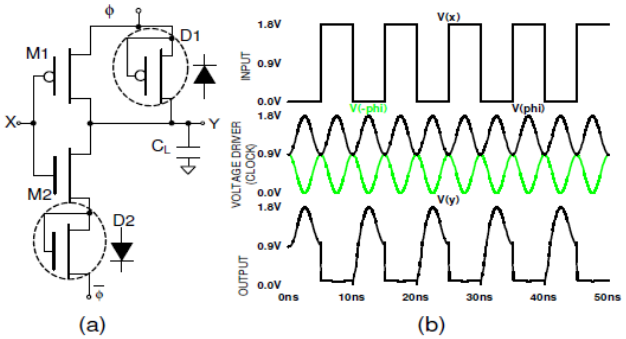
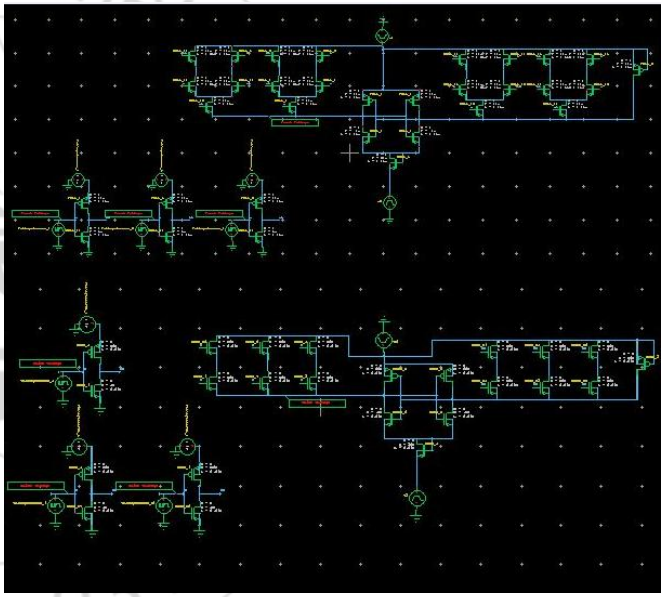
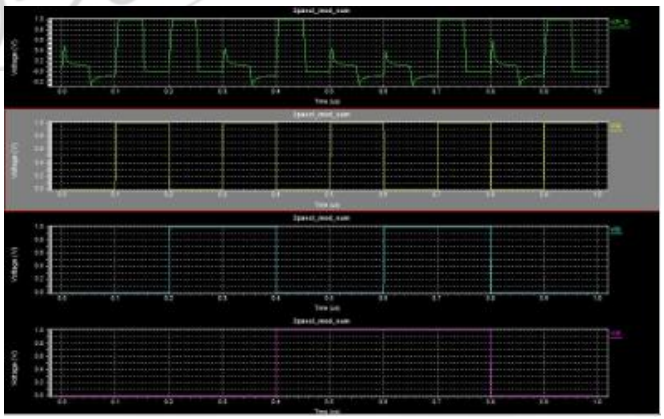


Figure 11: (a) 2PASCL inverter. (b) waveform from simulation at 100MHz

5. Adiabatic 2PASCL ADDER circuit design

An adder circuit is designed using 2PASCL logic. The schematic is shown in figure 12. The full adder designed using 2PASCL logic will show power reduction as compared to conventional CMOS devices.





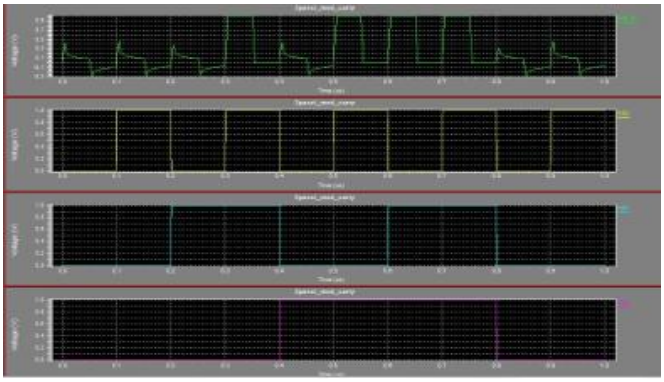


Figure 12: 2PASCL ADDER schematic and waveform from simulation

6. Future Work

From the study it was found that the adiabatic logic circuits can play a significant role in designing applications where power conservation is one of prime importance such as in high performance, hand held and portable digital systems running on batteries. The above circuits shows power reduction compared to CMOS. In future, we will design circuits using 2N-2N2P, ECRL, PFAL, 2PASCL, CAL etc adiabatic logic so that we can get minimum power dissipation.

7. Conclusion

We have studied about different type of adiabatic logic and found that the adiabatic 2PASCL offers significant power reduction and better performance. The NAND, NOR, EXOR logic using 2PASCL topology has offered more energy saving compared to conventional CMOS. As it dissipates less energy than other adiabatic inverter circuits, 2PASCL is a promising candidate for low power circuits.

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