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Design of Switched Resistor ΔΣ ADC Using VHDL-AMS Tool

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Abstract: ***This paper presents design and simulation of switched resistor (SR) ΔΣ ADC in analog mixed signal (AMS) environment. The proposed design consists of 1st order single bit SR ΔΣ modulator with dissipated power of 0.935mW and 2nd order digital decimation filter. Such modulator offers high-performance due to small delay which is achieved by simple circuitry. SR technique is chosen to achieve reduction of element and components, low power dissipated in hardware realization, and ability of tunable. The proposed decimation filter design consists of a second order Cascaded integrator Comb filter (CIC). Such structure no need multipliers in order to save silicon area. The proposed design and simulation are carried out using Mentor Graphics SystemVision tools. The switched resistor (SR) ADC offers resolution of 10-Bit using 64 Oversampling ratio.***

Keywords: Switched resistor, Delta Sigma modulator, Cascaded integrator Comb filter.

1. Introduction

Now, Analog-to-digital converters (ADCs) are the backbone for building signal processing and communication systems blocks. That is because most of the signals in their natural form are analog hence signal in digital format can be easily stored and recall. ADC is preferred to be designed in low power and high speed in order to achieve long battery life for portable system. Also minimum number of battery cells reduces the volume and weight of the system [1].

There are many types of ADCs such as flash ADC, successive approximation, and ΔΣ ADC. These types are different in features as shown in table 1. Also, each one has its own advantage and dis advantage. Flash ADC is the fastest but requires large number of comparator, then a large silicon area and also power dissipated. Successive approximation has high speed with medium resolution [1].

ΔΣ ADC is an over sampling converters. The benefit of ΔΣ ADC is using signal processing techniques in place of complex and precise analog components, which achieve high resolution. It involves only 15 percent of analog components , thus making it a good choice to realize embedded ADC interfaces in modern systems-on-chip (SoCs) [2].

Table 1: ADCs features

Type	*Speed*	*Resolution*	*Hardware complexity*
`Flash	Very high	Low	High
SAR	High	Medium	low
ΔΣ	Slow-medium	High	Medium

This work is organized as follows: Section 2 describes analog mixed signal using VHDL-AMS. In section 3 describes SR ΔΣ modulator and digital decimation filter. Experimental results are discussed in Section 4.Conclusion is presented in Section 5.

2. Analog Mixed Signal and VHDL-AMS

VHDL-AMS is a hardware description language for mixed signal models. “Very High Speed Integrated Circuit /VHSIC/ Hardware Description Language for Analog and Mixed-Signal Systems”. It contains not only the simultaneous representation of digital and analogue electrical signals, but also nonelectrical quantities can be described with that. It is an addition to the classic VHDL (IEEE 1076-1993) which only enables description of time-, and value-discrete models. At first VHDL was developed to define a uniform description language for digital systems and to simplify the simulation and synthesis of digital circuits. Because of the rapid development in computer technology and more efficient mathematical algorithms it has become possible to simulate time-continuous analogue systems too. Therefore a description standard was fixed with the AMS expansion to VHDL (IEEE 1076.1-1999) for mixed signal models in 1999. VHDLAMS language depends on the concept of “Quantity” represents the equation variables [7].

The System Vision environment integrates simulation models from multiple design and engineering domains including mixed analog/digital circuits; thermal, mechanical and hydraulic systems; and continuous and sampled-data control systems [8]. For example a VHDL code of an Op-Amp included in SystemVision library is shown in Fig.1.

```
library IEEE;
use IEEE.math_real.all;
-- Use IEEE natures and packages
use IEEE.electrical_systems.all;

entity OpAmp_3p is
-- Initialize parameters
  generic (rin   : resistance := 1.0e6;     -- Input resistance [Ohm]
           rout  : resistance := 100.0;     -- Output resistance [Ohm]
           avol  : real       := 100.0e3;   -- Open loop gain [No Units]
           f_0dB : real       := 1.0e6      -- Unity Gain Frequency [Hz]
           );
-- Define ports as electrical terminals
  port (
    terminal in_pos, in_neg, output : electrical);

end entity OpAmp_3p;

-------------------------------------------------------------------------------
-- Basic Architecture
-- Characteristics modeled:
--      1. Open loop gain
--      2. Frequency characteristics (single pole response)
--      3. Input and output resistance
-- Uses Q'Ltf function to create open loop gain and roll off
-------------------------------------------------------------------------------
architecture basic of OpAmp_3p is
  -- Declare constants
  constant f_3db : real        := f_0db / avol;     -- -3dB frequency
  constant w_3dB : real        := math_2_pi*f_3dB;  -- -3dB freq in radians
  -- Numerator and denominator for Q'LTF function
  constant num   : real_vector := (0 => avol);
  constant den   : real_vector := (1.0, 1.0/w_3dB);
  -- Declare input and output quantities
  quantity v_in across i_in through in_pos to in_neg;
  quantity v_out across i_out through output;

begin

  i_in  == v_in / rin;                    -- input current
  v_out == v_in'ltf(num, den) + i_out*rout;  -- output voltage

end architecture basic;
```

Figure 1: VHDL-AMS code of an OP-AMP

3. ΔΣ ADC

Fig.2 shows the block diagram of a ΔΣ ADC. It consists of a ΔΣ ADC modulator and a digital decimation filter. The modulator is realized in analog technique to produce a single bit stream and a digital Decimation filter to achieve a multi bit digital output [3].

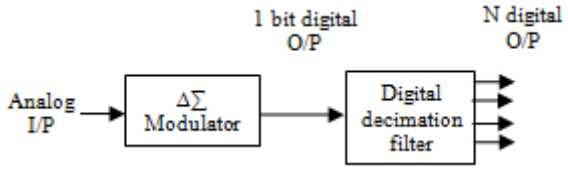

Figure 2: ΔΣ ADC block diagram

3.1 1st order SR ΔΣ Modulator

The ΔΣ Modulator is established from known delta modulator. The name (sigma) comes from the summing integrator in front of delta modulator. Fig.3 shows a block diagram of 1st orderΔΣ Modulator [4].

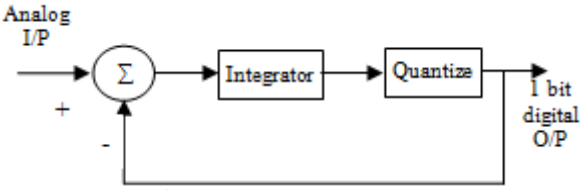

Figure 3: 1st order ΔΣ modulator block diagram

Analog filters are key building blocks in many systems. Like many other analog circuits, traditional filters are adversely affected by a low supply voltage. One of the most fundamental low-voltage issues in analog design is the reduction in available signal swing. To achieve the same dynamic range as their high-voltage counterparts, low-voltage circuits must achieve better noise and distortion performance. This is difficult because low-voltage operation will increase the nonlinearity, leading to more distortion. Conventional switched-capacitor (SC) filters have difficulty working at low supply voltages because of the floating switch in the signal path.

Continuous-time (CT) filters are also strongly affected by a low supply voltage. One of the most critical issues in integrated CT filters is the corner frequency deviation caused by variations in process, voltage and temperature.

To suppress this time-constant variation, a SR filter (integrator) is often used.

The tuning range will be changed by varying duty cycle of the clock as stated in eq. (1) [5].

$$R_{eq} = \frac{R_{on}}{D} \tag{8}$$

The order of modulator is determined by the order of used integrator.

Then, the using SR technique, circuit complexity is reduced, and no need to change the topology. Moreover the nonlinearity is reduced [13]. Fig.4 Shows a simple SR integrator used for proposed ΔΣ Modulator and Fig.5 shows its simulation result.

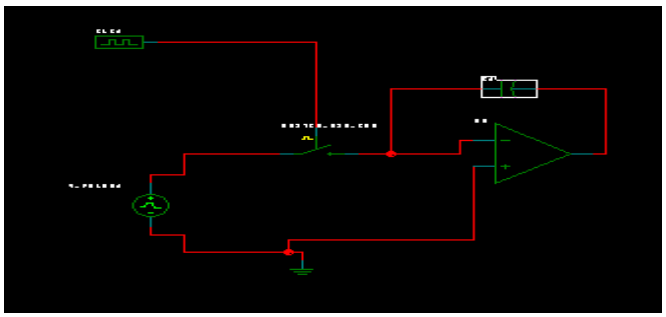

Figure 4: SR integrator circuit

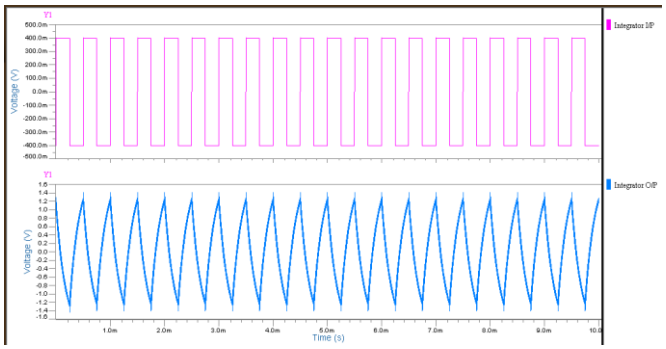

Figure 5: SR integrator simulation results

The quantizer in Fig.3 is actually a comparator if single bit modulator is used. The comparator is also coded in Spice and then the code is imported to SystemVision. Both the differential node and integrator is mapped in this work as a SR summing integrator as shown in Fig.6.

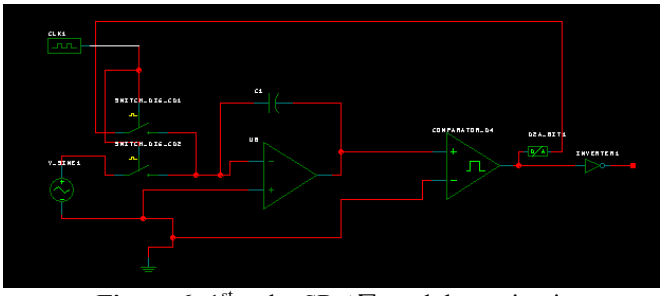

Figure 6: 1st order SR ΔΣ modulator circuit

By applying sine wave as input to the modulator, the output is 1-bit digital data. As the input increases, the positive digital data width will increase. At the peak of the sine wave the positive pulse width has the maximum width. As the input decreases, the positive digital data width will decrease. When the input reaches zero the positive digital data width becomes equal to the negative digital data width. As the sine wave decreases below zero, the negative pulse width of the output will increase. The average value of the output follows the analog input [6]. Fig.7 shows the output of 1st order single bit SR ΔΣ modulator with OSR of 64 at 2 kHz sine wave input. The power dissipation of modulator is 0.935 mW by SystemVision

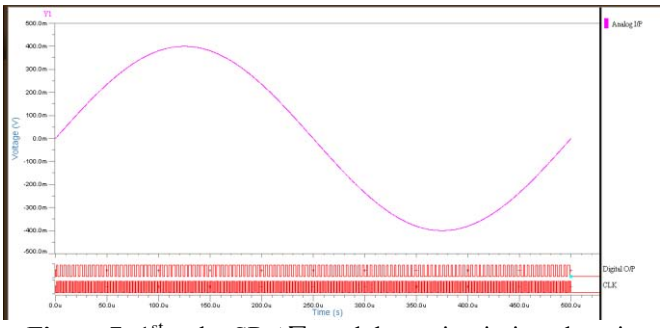

Figure 7: 1st order SR ΔΣ modulator circuit time domain simulation results

3.2 Digital Decimation filter

The main objective of digital decimation filter is to remove out of band quantization noise, increase resolution bits, and down sampling. The 1-bit modulator stream is digitally filtered to obtain an N-bit representation of the analog input. In simplified terms the 1-bit modulator stream is accumulated over (K) sampling cycles and divided by (K), where (K) is the oversampling ratio. This yields a decimated value which is the average value of bit stream from the modulator.

A preferred decimation filter can be realized using cascaded integrator comb filter (CIC) with transfer function given by eq. (9).

$$H(z) = \left(\frac{1 - z^{-K}}{1 - z^{-1}}\right)^{L} \qquad (9)$$

Where L is the filter order, in this work L=2 for 1st order modulator. There is much architecture for implementing CIC filter such as polyphase structure, non-recursive structure, and IIR-FIR structure.

The IIR-FIR structure provides the lowest area by increasing oversampling ratio compared with others [9]. So in this paper the IIR-FIR is chosen.

From eq. (9), the numerator represents the transfer function of a differentiator and dominator represents transfer function of integrator.

A simple block diagram of CIC that follows eq. (9) is shown if Fig.8.

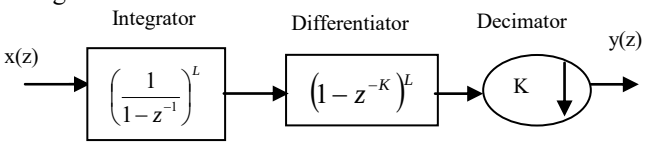

Figure 8: Direct CIC block diagram

The differentiator circuit needs K (oversampling ratio) delay elements, which are implemented using registers. The number of delay elements increases as oversampling ratio will increase, and as well the number of registers bits that are used to store the data. This type of implementation becomes Complex and requires more area as we go for higher order and higher sampling rates. This problem can be overcome by implementing a decimation stage between the integrator and Differentiator stages as shown in Fig.9 [10].

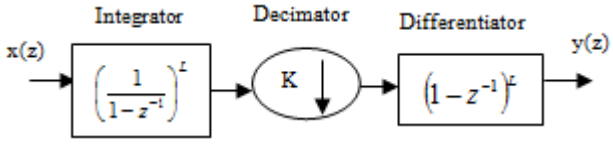

Figure 9: Modified CIC block diagram

The one bit digital integrator and differentiator is a combination of delay element and a simple full adder, as shown in Fig.10 a&b respectively [11].

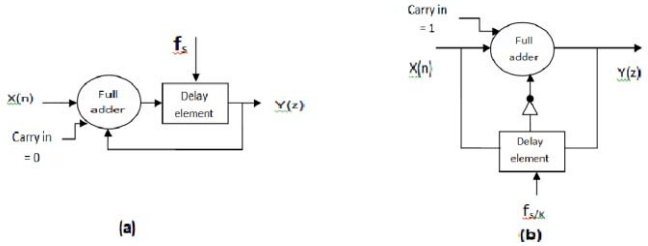

Figure 10: One bit digital integrator (a) and differentiator (b)

A clock divider is needed for both down sampling and differentiator. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved.

To generate the required clock output for the differentiator of the CIC filter. As 64 =26, N=6, we need 6-stage T-flip flops to achieve a frequency division by 64. Whenever the input and output of a T-flip flop are given as inputs to an AND gate, only the ON time of the input clock is transmitted to the output. The output of the AND gate remains at logic „1" during this ON time only [10].

T-flip flop is not included in SystemVision library; it's only JK- flip flop. T- flip flop is created from JK- flip flop By inverting K by J and connecting Q' to J. Fig.11 Shows the

clock divider circuit and its simulation wave forms are shown in Fig.12.

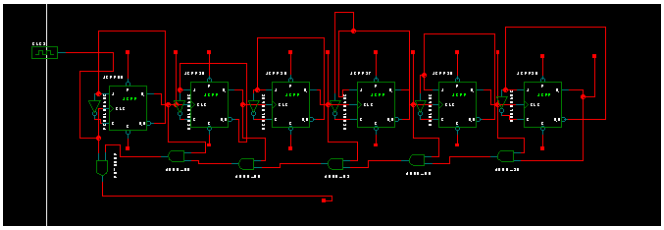

Figure 11: clock divider by 64 circuit

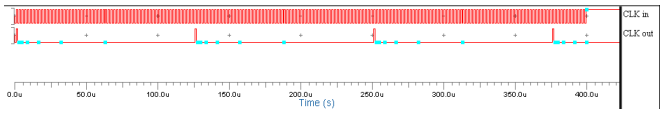

Figure 12: clock divider by 64 circuit wave forms

A single integrator is unstable due to the single pole at z=1. There is a chance of register overflow and data may be lost. To avoid this problem of register overflow, 2's complement coding scheme is used. By using the 2"s complement number representation, the data will not be lost due to register overflow as long as the register used to store the data is long enough to store the largest word given by Kx2N. Here N is the number of input bits to that particular integrator stage. Internal word width (W) needed to ensure not run time overflow is estimated from eq. (2) [10].

$$W = (1\sin bit) + (\text{Number of input bits}) + (\text{Number of stages "filter order L "}) + \log_2(\text{Decimator factor}) \quad (2)$$

In our case W=14. Then a coder 2's complement circuit is needed to convert a single bit of modulator output to 14 2's complement bits as illustrated in table 2.

Table 2: ADCs features

I/P single bit	*O/P 14 bits 2's complement*
0	00000000000001
1	11111111111111

The circuit that responsible for existing above table is shown In Fig.13.

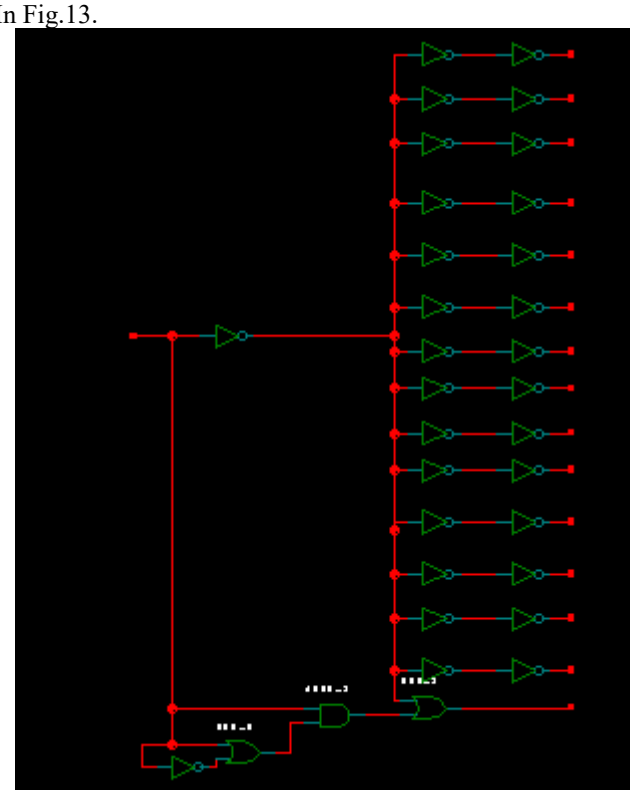

Figure 13*:* 14 bit 2's complement coder

The overall digital filter was implemented as in Fig.14. Note that down samplers were realized using D flip-flops clocked at the lower frequency [12].

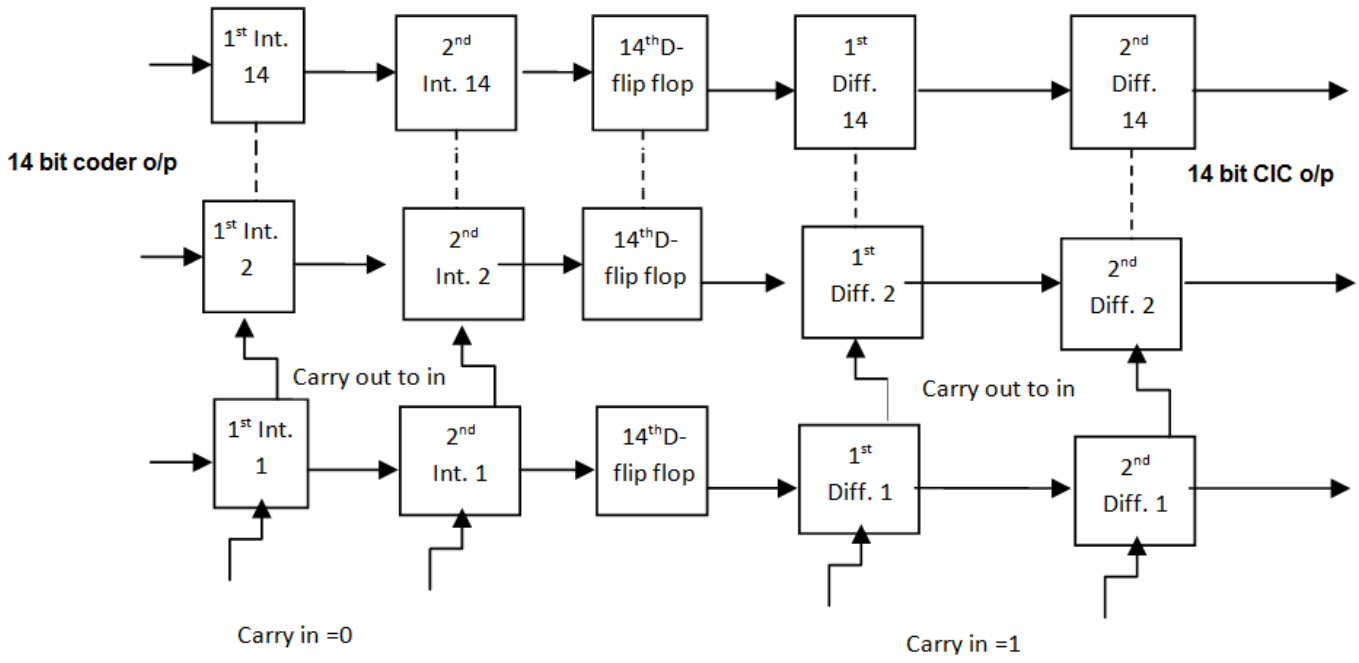

Figure 14*:* Over all CIC filter

4. Experimental results

The output of the CIC is a two"s complement 14-bit data. This data has to be converted into binary form and also the least significant bits should be dropped in order to achieve the required resolution as given in eq. (3)&(4).

$$N_{final} = N_{i/p} + N_{inc} \quad (3)$$

$$N_{inc} = \frac{30\log K - 5.17}{6.02} \quad (4)$$

In equation (3)&(4), N_{inc} is the increase in resolution and K is the oversampling ratio. So, for K=64, the output resolution achieved is 10 bits. Hence, we select 11-Bits (1-sign bit +10 resolution bits) from the 14-bit output of the differentiator and drop the lower 3 bits [11].

The applied sine wave input to the ADC is .8Vp-p, 2 kHz with a bandwidth of 4 kHz and the applied oversampling clock frequency is 512 kHz.

In the first case, since the output frequency is at 8 kHz and the input signal is at 2 kHz, there exist four output data words in one clock cycle of the input signal. Fig.15 shows Experimental results showing the four waveforms for digital output codes.

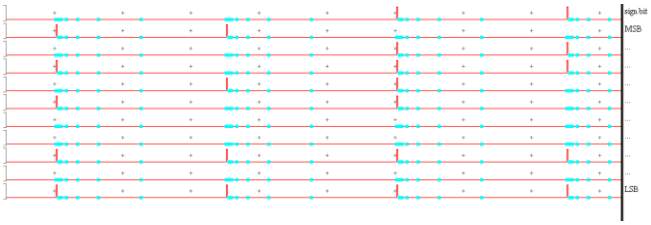

Figure 15: ADC O/P

For an ADC 1 LSB is defined as eq. (5).

$$1LSB = \frac{V_{FSR}}{2^N} \quad (5)$$

Substituting the previous value in equation (5) the resulted value is 0.00039. The output of the CIC filter is in 2's complement form. The desired 11-Bits output is converted from 2"s complement to equivalent binary form and actual analog voltage (by multiplying 1 LSB with decimal value). Table 3, which shows the 11-Bit 2's complement output, binary output, its decimal equivalent, and the actual analog voltage.

Table 3: O/P results

2's complement	*Binary form*	*Decimal value*	*Analog equivalent*
01010100101	01010100101	677	.264
01001000101	01001000101	581	.227
10111100101	01000011011	-539	-.211
10110000101	01001111011	-635	-.248

It can be observed that alternative outputs have approximately same magnitude.

5. Conclusion

A SR 1st order ΔΣ modulator and 2nd order CIC decimation filter have been designed using VHDL_AMS Mentor Graphics tools. The SR ADC has been obtained resolution 10-Bit using 64 Oversampling ratio. The SR integrator used in ΔΣ modulator offers component reduction and tunable ability. The power dissipated of 1st order SR ΔΣ modulator is 0.935mW.

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