4. Experimental results

The output of the CIC is a two's complement 14-bit data. This data has to be converted into binary form and also the least significant bits should be dropped in order to achieve the required resolution as given in eq. (3)&(4).

$$N_{final} = N_{i/p} + N_{inc} \quad (3)$$

$$N_{inc} = \frac{30\log K - 5.17}{6.02} \quad (4)$$

In equation (3)&(4), N_{inc} is the increase in resolution and K is the oversampling ratio. So, for K=64, the output resolution achieved is 10 bits. Hence, we select 11-Bits (1-sign bit +10 resolution bits) from the 14-bit output of the differentiator and drop the lower 3 bits [11].

The applied sine wave input to the ADC is .8Vp-p, 2 kHz with a bandwidth of 4 kHz and the applied oversampling clock frequency is 512 kHz.

In the first case, since the output frequency is at 8 kHz and the input signal is at 2 kHz, there exist four output data words in one clock cycle of the input signal. Fig.15 shows Experimental results showing the four waveforms for digital output codes.

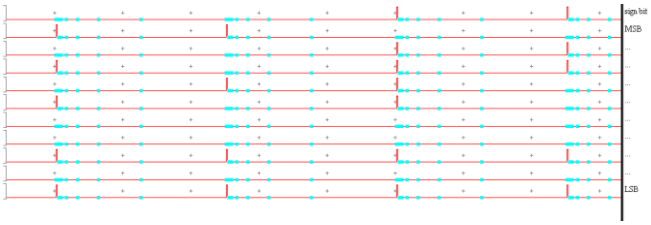

Figure 15: ADC O/P

For an ADC 1 LSB is defined as eq. (5).

$$1LSB = \frac{V_{FSR}}{2^N} \quad (5)$$

Substituting the previous value in equation (5) the resulted value is 0.00039. The output of the CIC filter is in 2's complement form. The desired 11-Bits output is converted from 2's complement to equivalent binary form and actual analog voltage (by multiplying 1 LSB with decimal value). Table 3, which shows the 11-Bit 2's complement output, binary output, its decimal equivalent, and the actual analog voltage.

Table 3: O/P results

2's complement	*Binary form*	*Decimal value*	*Analog equivalent*
01010100101	01010100101	677	.264
01001000101	01001000101	581	.227
10111100101	01000011011	-539	-.211
10110000101	01001111011	-635	-.248

It can be observed that alternative outputs have approximately same magnitude.

5. Conclusion

A SR 1st order ΔΣ modulator and 2nd order CIC decimation filter have been designed using VHDL_AMS Mentor Graphics tools. The SR ADC has been obtained resolution 10-Bit using 64 Oversampling ratio. The SR integrator used in ΔΣ modulator offers component reduction and tunable ability. The power dissipated of 1st order SR ΔΣ modulator is 0.935mW.

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