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Selective Harmonic Elimination Technique Based Cascaded Multilevel Inverter with Reduced Number of Switches

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Abstract: ***This paper presents a topology with a reduced number of switches, which is used to reduce the total harmonic distortion (THD%) using MCPWM technique, MCPWM with trapezoidal reference wave and also SHE technique such as PSO technique and Newton-Raphson (NR) technique. SHE technique is used to eliminate a particular harmonic in a multilevel inverter (MLI);the MCPWM and Trapezoidal reference wave techniques are also used to reduce the harmonics present in the MLI with a triangular wave which acts as a carrier wave .This topology is also used to improve the multilevel performance .The performance evaluation of the proposed PWM, Trapezoidal reference wave and SHE techniques for a MLI is done by using MATLAB/Simulink and THD is analysed. It is observed that PSO technique produces a better fundamental voltage output and less THD.***

Keywords: Multicarrier Pulse Width Modulation (MCPWM), Selective Harmonic Elimination (SHE), Particle Swarm Optimization (PSO), Newton-Raphson (NR) and Total Harmonic Distortion (THD).

1. Introduction

Inverter converts the power from DC to AC. The multilevel inverters concept has been introduced since 1975. Multilevel inverters have been emerged as powerful devices in the power industries. Initially the inverters scope was limited up to two-level inverters but nowadays multilevel inverters such as three levels, five levels and higher levels have been designed depending upon the various topologies. In 1960s, with series connected H bridge multilevel inverter technology came into existence . These inverter were called as cascaded H-bridge inverters. In the same year another type of topology came into existence i.e. flying capacitor. However the real multilevel power converter came in the late 1970s. This topology is called as diode clamped or NPC configuration.[6]. Conventional two-level inverters are used to generate an AC voltage from a DC voltage. It can only produce two levels of output voltage, +Vdc or –Vdc. Two-level inverter are only used in low-voltage electrical equipment's up to 1kv. Multilevel inverter is an attractive solution for high power drives especially on medium voltage and it also offers some salient features regarding modularity, power quality power applications. For medium and high voltage equipment over 1KV, a multilevel inverter can be applied. Generally there are three different types of multilevel inverter available; diode-clamed MLI reduces the harmonic contents by adding zero level in the output voltage. With increase in the switching devices, clamping diodes and capacitors further extension to any level is possible. There are three different possible switching states in a 3-level diode-clamped MLI, which produce a stair case type of output voltage. Flying capacitor MLI is similar to the diode clamped MLI, but instead of clamping diode the flying capacitor MLI uses clamping capacitance. Each capacitor voltage is different. The clamped capacitor C1 is starts charging when the switch S1' and S2' is ON and starts discharging when the switch S1 and S2 are ON.CHB multilevel inverter, with its modularity and flexibility, shows superiority by comparing with other types of MLI. The hybrid multilevel inverter topology has two parts; one part is known as high frequency and another part is known as Low frequency. The high frequency is also known as level-generation part; this part consists of three power semiconductor switches, diodes, dc voltage source. It is responsible of generating the levels in the positive polarity. The next part is known as polarity generation. This part is used to generate the polarity of the output voltage.

2. Modes of Operation

This topology has four modes of operation to generate seven levels. The various switching combinations for different levels are explained below and is given in Fig.3.6 and Table.3.1 gives the switching states of the hybrid multilevel inverter. The generation of the PWM signal for the DC link switches can be explained as follows:

a) Level 0: During this mode of operation the switches 2, 3 and 4 are turned ON. The source is disconnected from load. So the output voltage across the load will be zero.

b) Level 1: During this mode of operation the switches 2, 3 and 5 are conducting. So V_{dc} of the supply is connected across the load. Therefore the voltage across the load will be V_{dc}. This mode of operation can be achieved by the switching combination 2,4and 6.

c) Level 2: During this mode of operation the switches 2, 6 and 5 are turned ON. Two times of V_{dc} is connected with load. So the output voltage is $2*V_{dc}$. This mode can also be obtained by turning on the switches 1 and 4.

d) **Level 3:** During this mode of operation the switches 1 and 5 are turned ON. So all the three voltage sources are connected with the load. The output voltage across the load will be equal to $3*V_{dc}$

3. Selective Harmonic Elimination (SHE) Technique

The multilevel inverter generates a staircase output voltage waveform by switching ON and OFF the switches for one fundamental cycle. There are two ways to eliminate low frequency harmonics,

1) By increasing the switching frequency in SPWM and SVM in case of two-level inverters or in multicarrier based phase shift modulation for multilevel inverters.
2) By computing the switching angles using SHE techniques.

The SHE techniques includes the mathematical modeling of output waveform and solving them for switching angles, the amplitude of the fundamental output voltage and number of the eliminated harmonics. Thus, in SHE, the lower order harmonics are either eliminated or minimized while the higher order harmonics are filtered out.

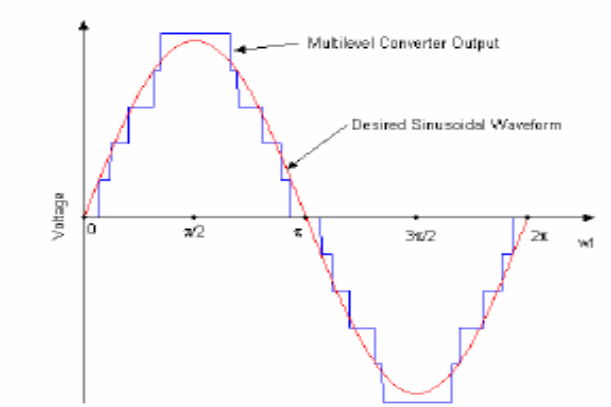

Figure 3: Staircase Sinusoidal Waveform Generated By H-Bridge Cascaded Multilevel Voltages

As shown in Fig.3, a multilevel converter can produce a quarter-wave symmetric stepped voltage waveform synthesized by several DC voltages. By applying fourier series analysis, the output voltage can be obtained.

$$\rightarrow (1)$$

Where,
n=integer multiple

φ_n = initial phase for nth harmonic

a o and c $_n$ = fourier co-efficient.

The output voltage equation derived for different voltage sources is given below,

$$\rightarrow (2)$$

Where,
S=number .of dc sources connected per phase

$V_1, V_2 V_3$ level od dc voltages..

The relation between the fundamental voltage and maximum voltage is given b the modulation index. It is given by m1, is the ratio of fundamental voltage v1 to the maximum voltage. The maximum voltage is given by

$$V_{1max} = \frac{4}{\pi} S V_{dc}$$

$$m = \frac{\pi V_1}{4 S V_{dc}} \rightarrow (3)$$

For an 7- level inverter, there are 4 H-bridges per phase so, s=4 i.e., five degrees are available; one degree is used to control the magnitude of fundamental voltage and remaining degrees are used to eliminate 5th, 7th, 11th, and 13th order harmonic components. The above statements are given by,

$$\text{Cos}(\theta_1) + \cos(\theta_2) + \ldots\ldots + \cos(\theta_s) = 4m_1 \rightarrow (4)$$

$$\text{Cos}(5\theta_1) + \cos(5\theta_2) + \ldots\ldots + \cos(5\theta_s) = 0 \rightarrow (5)$$

$$\text{Cos}(7\theta_1) + \cos(7\theta_2) + \ldots\ldots + \cos(7\theta_s) = 0 \rightarrow (6)$$

$$\text{Cos}(11\theta_1) + \cos(11\theta_2) + \ldots\ldots + \cos(11\theta_s) = 0 \rightarrow (7)$$

$$\text{Cos}(13\theta_1) + \cos(13\theta_2) + \ldots\ldots + \cos(13\theta_s) = 0 \rightarrow (8)$$

A. Particle Swarm Optimization (PSO) technique

The PSO technique which works under some rules. The PSO algorithm is effective in reducing the THD corresponding to the range of modulation index. After that the objective function is also evaluated for the particles to rank their present location. The new search points are then been updated regarding the pbest and gbest solution.

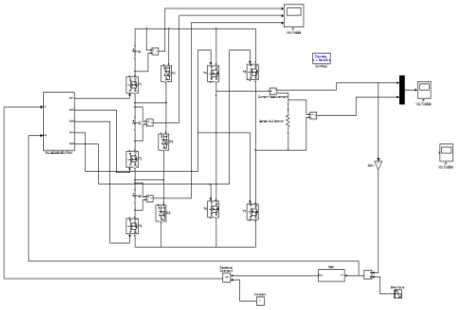

Figure 4: Simulation schematic of 7-level inverter for PSO technique

Algorithm

The PSO algorithm is given as follows:

Step1: Randomly the initial population sizes of switching angles are chosen and which should be between 0 toπ/2.

Step2: The Pbest, Gbest and velocity values are initialized and the iteration count for calculating the switching angles are also initialized.

Step3: The iteration counts are been updated.

Step4:update the velocity and position for moving of particles in search space

Step5: evaluate the fitness (i.e., objective function).

Step6: The Pbest and Gbest values are also updated.

Step7: If the criterion is achieved then go to next step otherwise repeat the step3 to step6 for the best solution.

Step8:The best solution of fitness value is selected.

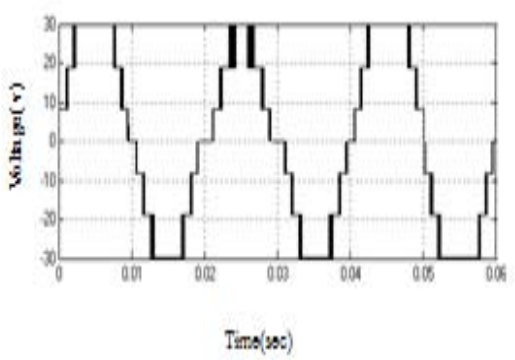

Figure 5: Output waveform

The THD (total harmonic distortion) which is the measure of the entire harmonics present in the circuit is calculated for the 7–level output of PSO technique using the fast Fourier analysis. The THD analysis for the above circuit is found to be 8.86%.

Table 1: Switching and Voltage Levels of the 7-Level Chb Inverter

S1	S2	S3	V_{OUT}
OFF	OFF	OFF	0
ON	OFF	OFF	1
ON	ON	OFF	2
ON	ON	ON	3

B. Newton-Raphson (N-R) technique

These nonlinear polynomial equations can be solved by the Newton-Raphson technique by iterations to determine the switching angles. The initial switching angles lie in between 0 and π/2.Newton-Raphson (NR) technique is also an iterative method. This method starts with an iteration and with an initial approximation.. However, the NR method is used to compute the switching angles for the system of SHE equations using the best solutions. The Switching angles produce the desire fundamental voltage along with elimination of 5th, 7th, 11th, and 13th order harmonics components are computed with respect to the range of modulation index. To reduce the harmonics in the multilevel inverter, the firing angles can be selected accordingly. For a 7-level inverter, three firing angles α1, α2 and α3 can be selected at different values in order to reduce the lower order harmonics.

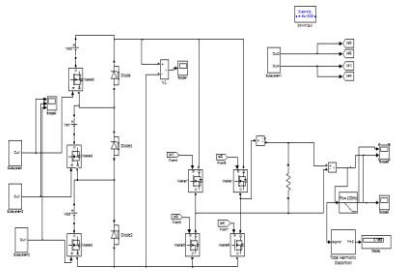

Figure 6: Simulation schematic of 7-level inverter for Newton-Raphson technique

The conditions to select the firing angles are given by the following

$$\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}$$

$$(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) = (m-1) \times M \rightarrow (9)$$

Where MI is the modulation index is the number of separate dc sources. The instantaneous phase voltage is,

$$\frac{4V_{dc}}{n\pi}\left[\sum_{j=1}^{\frac{(m-1)}{2}} \cos(n\alpha_j)\right]\sin(n\omega t) \rightarrow (10)$$

And the modulaton i

$$MI \rightarrow (11)$$

V_{cr}–Peak Carrier Voltage, m–Number of output levels For the given 7-level inverter, we have chosen the M value as 0.8 for effective harmonic elimination. Hence, equation can be rewritten as,

$$\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 = 3 * 0.8 = 2.4$$

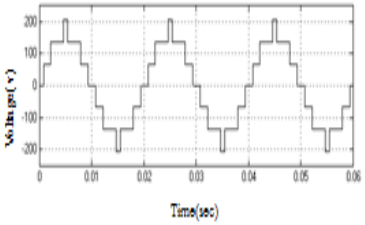

Figure 7: Output voltage

The THD (total harmonic distortion) which is the measure of the entire harmonics present in the circuit is calculated for the 7–level output of Newton-Raphson technique using the fast Fourier analysis. The THD analysis for the above circuit is found to be 12.38%.

4. Hardware Results

The proposed inverter is digitally implemented in *Universal VLSI Moon1* board. The board has X*C3S400PQ208* FPGA device as the main feature consists of 400k system gates, 8,064 logic cells, 896 CLBs,264 maximum user I/Os. Other features used on the *Universal VLSI Moon1* board are a 4 MHz oscillator for clock source, one pushbutton switch for system reset and toggle switches for the selection of modulation index values. For the generation of PWM it is required to compare the sinusoidal modulating signal and the triangular carrier signal. A simple logic which I have used is the "COUNTER". The pulse width depends on the counter speed. The count is nothing but the input data which will be variable. If the counter speed is slow then the width of the pulse is more and if it counts fast the short width pulse will be generated. The speed of the counter depends on the clock. This clock is nothing but the system clock which I will use as sinusoidal modulating signal. The system clock is high frequency near about 4 MHz to 6 MHz. By using "divide by" network required modulating signal can be obtained.

The following figure shows the flow how the seven PWM pulses are generated.

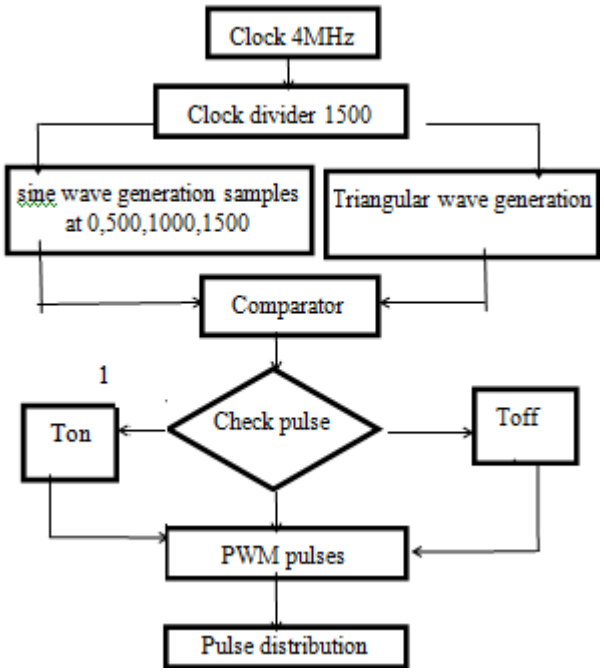

Figure 8: Flow chart for PWM generator

The model of the proposed multilevel PWM single phase inverter is simulated by using Xilinx simulation tool. The PWM pattern is derived and simulated at different modulation indexes (Ma) as a control signals; the system is tested and simulated by resistive.

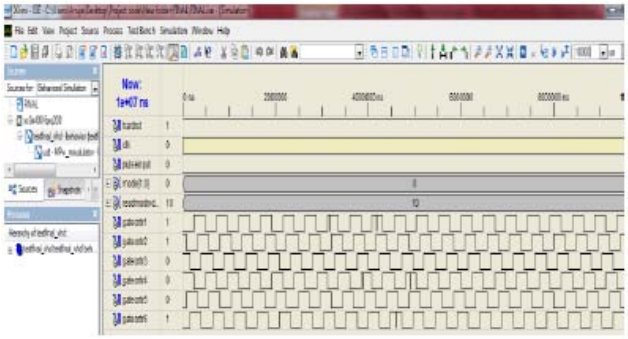

Figure 9: Multilevel PWM single phase simulation results using XILINX FPGA

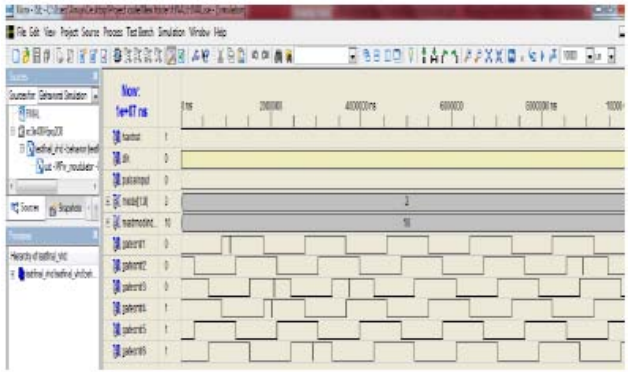

Figure 10: Multilevel PWM single phase simulation results using XILINX FPGA

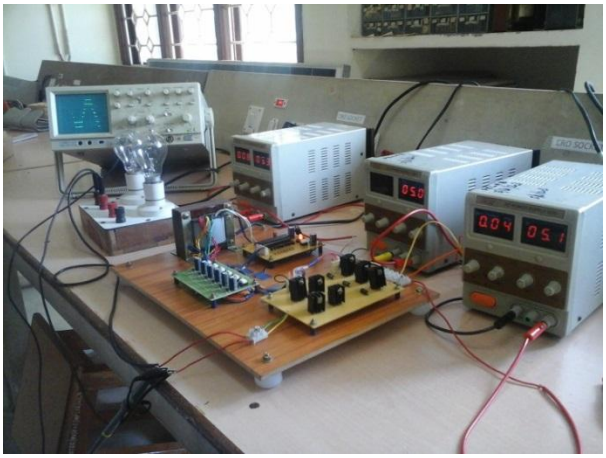

Figure 11: Overall Hardware setup

5. Conclusion

The simulation results of the multilevel inverter for various levels using PD, POD, APOD methods are simulated using MATLAB/Simulink software and got lower THD in PD method than other techniques in MCPWM and the results are tabulated. The MCPWM with trapezoidal technique is implemented in the 7^{th}, 9^{th}, 11^{th} and 13^{th} levels and has reduced the lower order harmonics like 3^{rd}, 5^{th} and 7^{th} and it is found that thirteen-level inverter has lower THD among the levels. The selective harmonic elimination (SHE) technique is implemented for 7-level by using Newton Raphson got 12.38% of THD and by using PSO got 8.86% of THD. Thus, the hardware implementation is carried out for seven-level inverter with particle swarm optimization technique using Field Programmable Gate Array (FPGA) and the output results are observed.

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