

Design Parameter Analysis of Simulink and System Generator Module for Real Time Image Splitting and Enlarging

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Abstract: The paper presents the design parameter analysis of simulink module and system generator module for a real time image splitting and enlargement. Image splitting and enlargement is done. The various design parameter used for the image splitting and enlargement and the output difference between the two module simulink and the system generator is discussed in this paper.

Keywords: Image, Splitting, System generator, Video, Simulink

1. Introduction

Image can be defined in several ways. One way of defining an image can be a two dimensional function $f(x,y)$. We can define X and Y as spatial coordinates and the function can also be pair of (x,y) called to be grey level of an image. Splitting of the image is done through manual splitting by rows and column wise. Splitting of image is done in to four equal parts. The proposed block diagram for image splitting is shown in Fig.1.

Designing the system development tool for any design is by considering the starting point. We need to follow the disciplined methodology for designed process in order to guarantee the development of such system. Designing a system in such a way that it must help us to handle complex design in very efficient manner, time design should be minimize, it must eliminate many error and also the reduced man power finally it should be the optimal design solution. We consider system generator is one of the presently cutting edge technology where to implement the DSP application into FPGA platform would be beneficial.

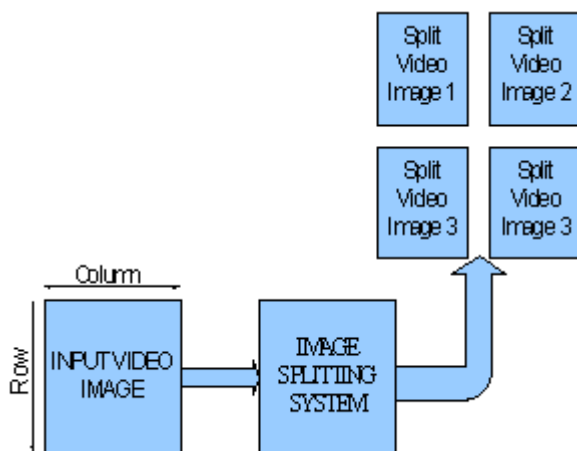


Figure 1: Proposed Image splitting Diagram

The paper is organized as follows. Proposed Block Diagram Of Image/Video Splitting is presented in section 2. Section 3 presents the Simulink Design for real time video Image

Splitting. Section 4 gives the design of system generator result for real time Image/video Splitting. Simulink and System generator results are presented in Section 5. Section 6 presents the Conclusion and future work.

2. Proposed Block Diagram of Image / Video Splitting

The design task for the image splitting is carried out using the various simulink parameters. By using image processing blockset in matlab simulink R2007b version parameter has been designed.

A. Block Set Resize

One of the simulink parameter namely block resize enlarges or shrinks the image by resizing the image in one dimension. Later it resizes image in other dimension.



Here we need to specify the data type of the input signal. If the data type is floating point the output must contain the same data type. We can also select the output size as a percentage of the input size. The aspect ratio of output column and the aspect ratio of output row depend on input parameter. In dialog box the appearance of resize factor in percentage parameter occurs.

B. Block Set Color Space Conversion:



The below mentioned equation used to convert the RGB to YCbCr and YCbCr to RGB conversion.

$$\begin{bmatrix} Y' \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} + A \times \begin{bmatrix} R' \\ G' \\ B' \end{bmatrix}$$

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = B \times \left(\begin{bmatrix} Y' \\ Cb \\ Cr \end{bmatrix} - \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} \right)$$

The A and B values can be decided by the user choice for the conversion process and for some of the standard scanning parameters. The input RGB formats converts to YCbCr format by the color space conversion. YCbCr mean to state the intensity in lumia blue component (Cb) and intensity in chroma red component (Cr). The main purpose of converting color image to grey level image is the processing time can be increased in case of grey level images. But finally we need to convert the grey level image back to RGB image by using the resize block set.

The other parameter of simulink includes matrix concatenation. This block also operates in vector or the multidimensional array concatenate mode. Sub Matrix selection, UDP send, UDP receive, Video to display are some of the simulink parameter which helps in building the simulink design. Once the suitable parameters are designed for designing the simulink model it has to be integrated in such a way that the output should be in the 256 X 256. The purpose of designing the simulink model is to verify the design before implementing it on the hardware. After the splitting is done it has to be enlarged by using the various interpolation techniques. Here we are going to use the bilinear interpolation techniques. After the interpolation image is going to be displayed on the big screen. The interpolation techniques is going to explain using the system generator model.

3. Design of Simulink Model for Real Time Video Image Splitting

Splitting the image in to four equal parts by using the simulink model is shown in the fig 2. By using the simulink parameter briefed above the final integrated design for

image splitting model has been developed. The input image size is of 256 X 256. The output image is going to original format by the YCbCr format and the each four splitted image size is of 256 X 256.

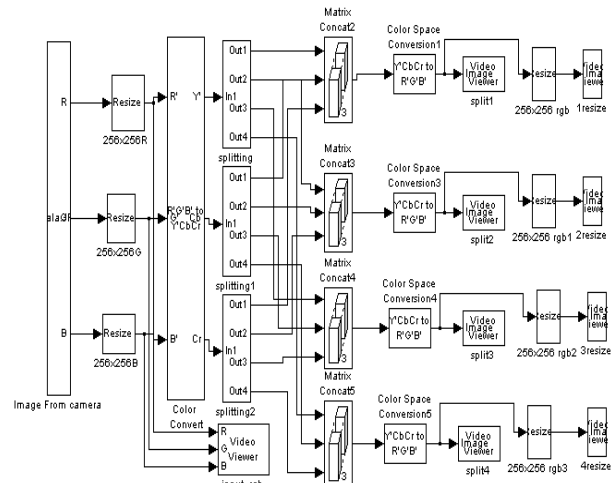


Figure 2: Design of Simulink Model for video/image splitting

4. System Generator Design for Real Time Video Image Splitting

1. Image Splitting

Image splitting block receive the serial data through gateway In. Single port RAM is used to store the image data by using counter. In single port RAM stored 65536 image data. Then 65536 image data split into equal half image data by using delay and counter. Two equal 32767 image data stored in two separate single port RAM. Each 32767 image data split into 16383 image data by using clock and store in four single port RAM. Then each output is connecting to interpolation data block and interpolation block. This procedure is used for other two color components. The system model for image splitting shown in Fig.3.

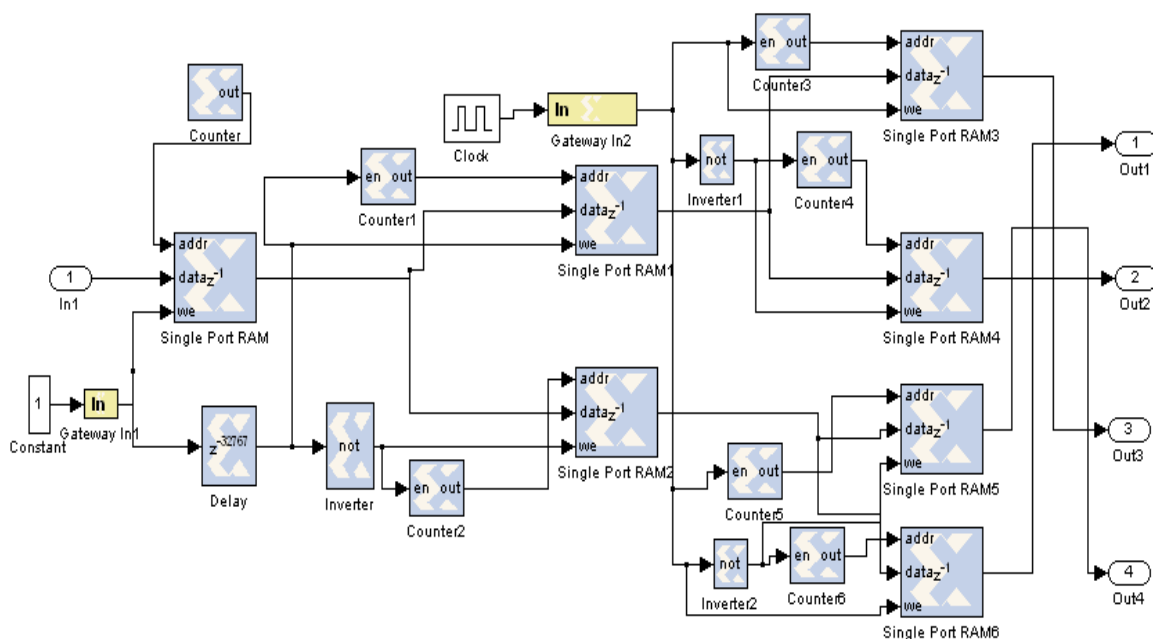


Figure 3: Design of System Image Splitting

2. Interpolation Data

The system model for interpolation data shown in Fig.4. Splitted output is connected to interpolation data block input. Here two delay blocks are used and clock is used to select image data. In positive edge select, first delay and in negative edge, select next delay [7]. Then both delay block output is connect to addition block. Shift block divides the output of addition output. The same procedure is used for all interpolation data block.

3. Interpolation

The system model for interpolation is shown in Fig.5. This interpolation subsystem, receives data from splitting part and interpolation data. Image data is connected to FIFO and FIFO1. By using clock signal resize the image into original size by horizontally and by using FIFO2 and FIFO3 resize vertically and mux is used to combine the output and produce the interpolated image [10]. Same procedure is used for all other splitted image.

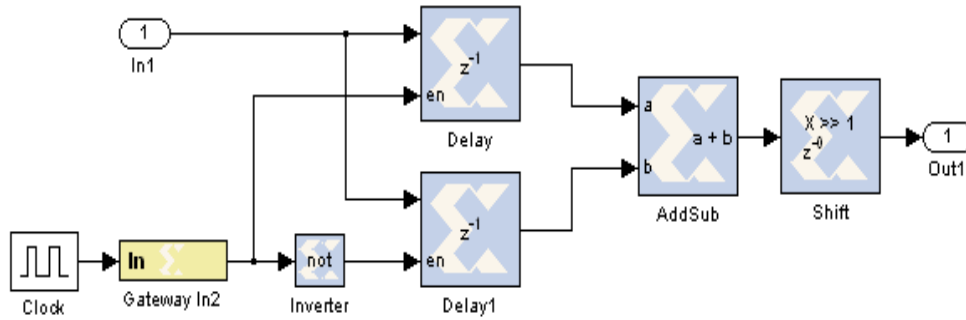


Figure 4: Design of System Interpolation Data: $(x+y)/2$

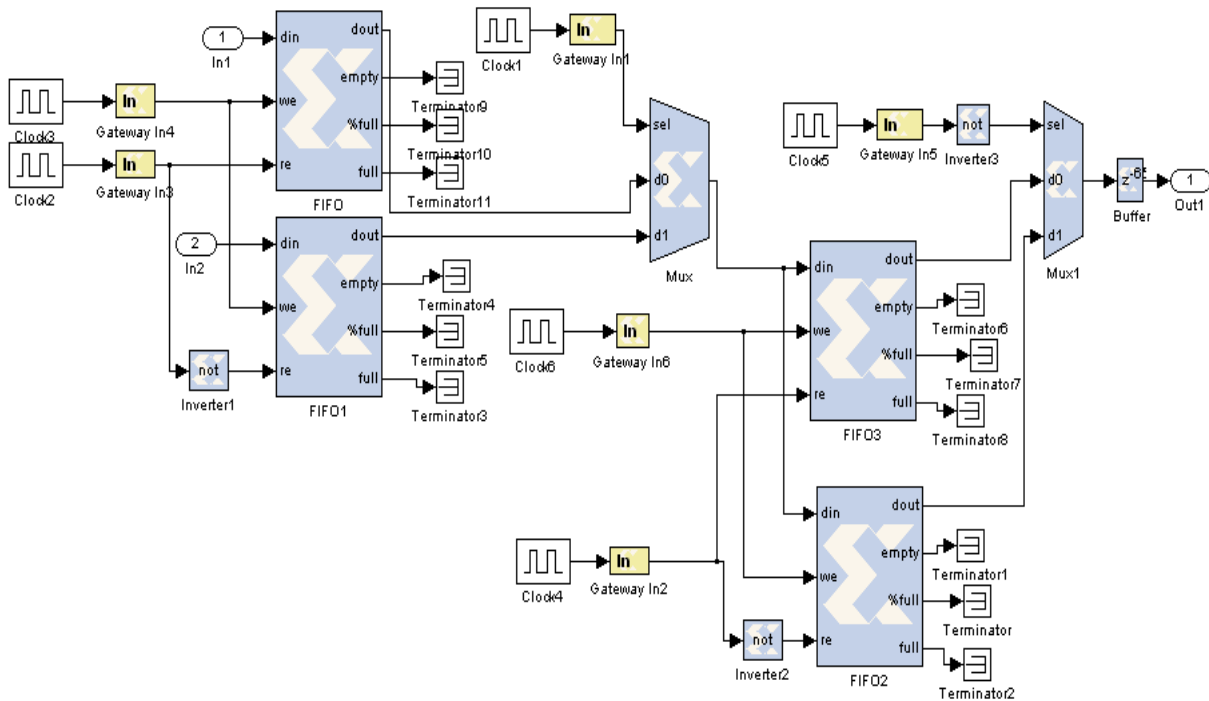


Figure 5: System Design of Interpolation

5. Simulink and System Generator Model Results

The image provided as input is in the form of RGB format. The input image size is 256 x 256 shown in below fig 6. The Final resulted image in RGB format and having size 512 x 512 shown in below fig 7 for Both simulink and system generator Models.



Figure 6: Input Image(256 x 256)

For achieving these results, first step was to split the image then performing bilinear interpolation and then merging of the original part of the image with the interpolation part. Finally the generated matrix was verified for the output image which is of very good quality in terms of resolution and appearance.

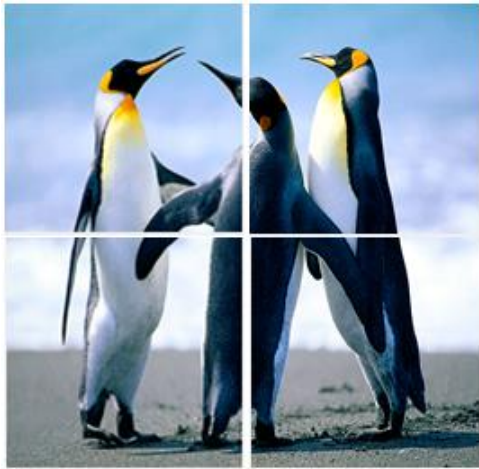


Figure 7: output image (Both simulink and system generator)

6. Conclusion and Future Work

The paper presents Video or image splitting and enlargement. The design was implemented using simulink and system generator blocks. In this paper the splitted and enlarged image output is same for both the model but the time taken by the system generator model is faster than the simulink model. In order to implement in system generator, image matrix is converted into single dimensional data. These single dimensional data are stored in memory. Then stored data was split from counter and splitted data stored in memory. Then interpolation using shift register and FIFO. These interpolated single dimensional data converted into image matrix. Then finally splitted image shown in screen. In future the design image splitting can be implemented on fpga in which output result can be faster than the system generator module. The proposed design can also be splitted in to eight equal parts with same resolution for the future work.

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