

Based on Multi-FPGA Neuron Simulation Hardware Platform

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Abstract: *The nervous system is constituted a complex network of a large number of neurons coupled. Network information transmission between neurons through synaptic currents and changes in membrane voltage implemented. Due to ethical issues, animal experiments have been unable to carry out large-scale, thus computational neuroscience increasingly favored by researchers. But the traditional software simulation method has lower computational performance limitations of the study efficiency. Specific integrated circuit chip is a hardware category, with parallel computing capabilities, with its built circuit model neuron system can significantly computational efficiency pricey neural network. Currently, there are many domestic and foreign researchers of Applied Physiology characteristics of the neural circuit model of signal transduction in the nervous system. In this paper, we use multi-chip field-programmable gate array (FPGA) chip to build a model of neural information transmission circuit, and through the neurons and neural network analysis to prove the validity of the model.*

Keywords: Neural Network, FPGA, Simulation, Control, Identification, LabVIEW

1. Introduction

Computational Neuroscience is the use of mathematical analysis and computer simulation method to simulate and study the nervous system of a subject [1]. From real biophysical model neuron theory to quantify the type of brain tissue and nerve calculation, learning their dynamics and interactions between neural networks, calculated from the point of view to understand how the brain, brain research style, adaptability the nature of information processing, information processing explore new mechanisms and pathways, thereby creating brain [2]. Its development will major impact on information science, intelligence science, neuroscience.

In recent years, a field programmable gate array (FPGA) technology has been used for high-speed digital computing platform. FPGA programmable logic flexibility combined with its ability to make high-speed parallel computing has the potential to be applied to dynamic real nervous system. In addition, FPGA can be used by the rapid acceleration of the brain process model simulation hardware prototype, build a simulation platform, the main advantage is that the model can be made in a shorter design cycles, studies the functional behavior of the brain. Currently, the limit of its development is mainly due to hardware resources, mainly before researchers build neuron simulation level by a single FPGA chip. This paper discusses the use of multi-chip FPGA simulation hardware platform to build neural network for the study of large nerve planning networks and brain simulation as a foundation.

2. Multi-FPGA development platforms neural network technology to explore

Multi-platform FPGA neural network system is to include multi-chip FPGA chip in the system, system development difficulty is in multi-chip FPGA chip with each other to calculate how neuroscience inquiry, technical difficulties exist is a connection between multi-chip FPGA topology, data

transmission clock synchronization and configuration of multiple FPGA. The following three main issues we have to research and development of multi-FPGA neural network simulation platform.

2.1 Topology Research

Multi-FPGA topology between multiple FPGA refers to connections according to how it affects the utilization of FPGA resources. Common structures include linear structure, grid type, cross-connect and mixed interconnect type, as follows Figure 1:

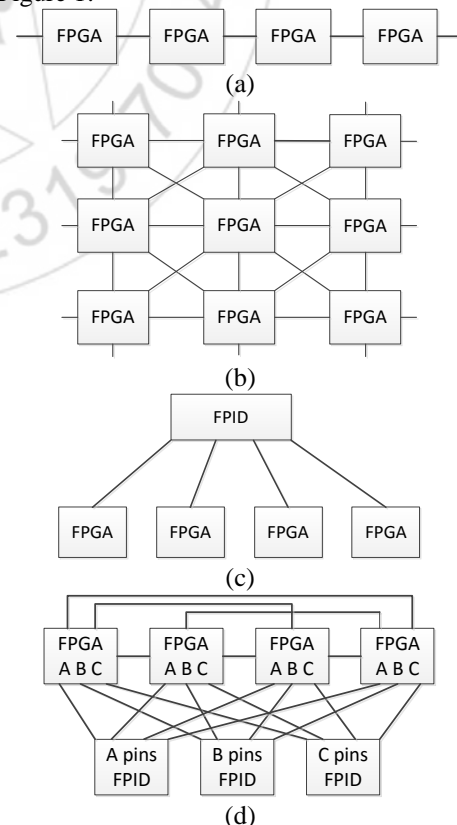


Figure 1: Multi-chip FPGA topology

The biggest characteristic linear structure is simple, low cost, easy placement and routing, mainly in the early stage of some multi-FPGA systems, such as the literature [3, 4], suitable for special applications, such as in [5] Use 32 Xilinx 3090FPGA composed of multi-FPGA systems to run pulsating algorithms. Each piece in the grid structure are its neighbors FPGA 8 FPGA connected directly communicate with the FPGA 8, without passing other FPGA, in communication efficiency and utilization pin has a great advantage.

Cross interconnect structure is the use of specialized field programmable interconnect device (FPID: Field Programmable Interconnect Devices) Programmable FPGA interconnects between, according to the number used FPID can be divided into fully cross-connect and partial crossbar interconnect of two types. The number of cross-system use fully interconnect structure contains only a FPID, using cross interconnection structure part of the system contains multiple pieces FPID, each piece of FPGA pins are divided into N subsets, N is FPID per piece FPGA first i subsets pin is connected to the i-th FPID.

FPID selection can either use a dedicated programmable interconnect devices [6], may be using a common FPGA devices. When using the FPGA to make FPID, if this time the FPGA is connected only assume the task does not implement other logic functions, obviously wasted logic resources, so the actual application, a portion of the pin is zoned interconnection use, other pin is used as an internal logic function module for external connection. FPID dedicated application saves FPGA pin resources, and are conducive to the PCB board layout and wiring, but also increases the cost of the system components.

2.2 Clock synchronization

Clock synchronization is a data signal transmission between the multi-chip FPGA, to ensure that the sender and receiver data synchronization clock. Clock synchronization is to determine whether the validity of the data transfer rate and data dissemination.

The method commonly used in clock synchronization using hardware methods clock buffer (CLOCK BUFFER) to a clock into multiple clock are supplied multi-chip FPGA use, complete transmit and receive data signals. 1, a schematic diagram of the clock required for data transmission between chips in FIG. FIG crystal oscillator circuit generates the oscillation signal CLK, is input to the PI49FCT3803 Clock Distribution chip, after PI49FCT3803 clock divider to generate the same clock signal multiplexer, the way in which the supply of the main chip A for transmitting data, all the way from the chip 2 is used for Data sent from the main chip samples stored. Clock CLKB clock divider issued after the PCB path delay time (T_{flt_CLKB}) reach the main chip, the master chip with data from the CLKB clock latch output port when T_{CO_DATA} arrive on the chip, the data output path of the PCB and then after a delay time (T_{flt_DATA}) reach the input port from the chip B; clock divider to generate a clock CLKA path through the PCB (T_{flt_CLKA}) delay time to the clock input from the chip B port, complete data is sent to the master chip A latched. This is the use of synchronous clock for

data transmission between chips the whole process. Therefore, the availability of data transmission between the two chips to meet two requirements. First, the main chip A input data valid time earlier than the effective time clock, that meet established time chip (T_{setup}); second, to ensure that data can be successfully latched into chip, the chip receiving data of the received data must be maintained for some time at the chip input port to ensure proper latch isochronous data into the device, i.e., satisfies the hold time (T_{hold}).

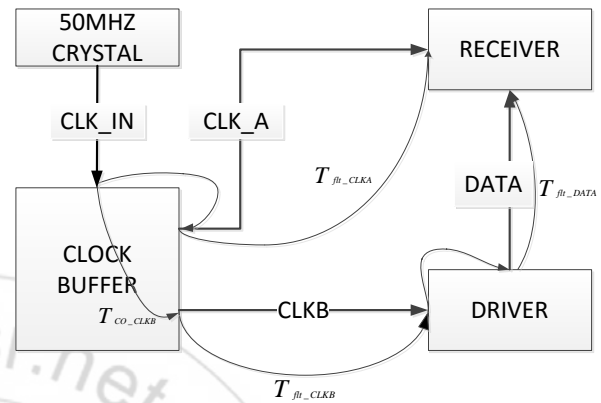


Figure2: Each component of the Lab model

2.3 Configuration Methods

2.3.1 Multi-chip FPGA active configuration

Multi-FPGA active configuration, when the first piece of chip configuration, its potential nCEO pin low, enabling the next device in the chain one device, until the last piece of chip configuration. Finally, a chip nCEO may not be connected or for user input and output pins. The multi-chip nCONFIG, nSTATUS, CONF_DONE, DCLK, and DATA [0] pin is connected together were received.

The first piece in the device chain as the main chip controls the entire configuration data chain configuration, other devices using passive configuration as the configuration chain from chip.

All FPGA chip nSTATUS and CONF_DONE pins are connected to an external pull-up resistor together, after receiving 3.3V supply, as shown below:

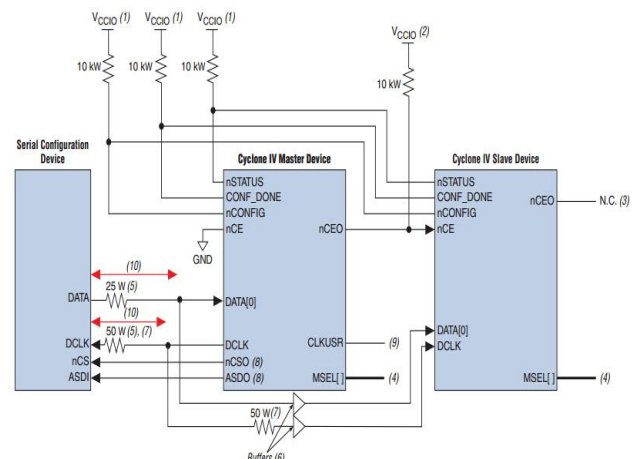


Figure3: Multi-chip FPGA active configuration

2.3.2 Multi-chip FPGA JTAG daisy chain configuration

FPGA on a multi-chip hardware experimental platform system using JTAG daisy chain configuration, shown in Figure 2.2, the first piece of the FPGA TDI (test data input port) and horns ninth pin socket connected to the last piece of the FPGA TDO (test data output port) and third pin socket horns connected between the chip TDO sequentially and connected on a TDI, TCK (test clock input port) on the entire chip, TMS (test mode select port) are connected together is connected to horns socket first leg and fifth foot; horns socket sixth foot VIO is Master-Blaster output reference voltage, the fourth pin VCCA is a voltage USB-Blaster, the second, ten feet grounded, seventh, eight-foot vacant . JTAG daisy chain configuration according to the actual needs of 4 FPGA configured with four different SOF file can also be individually configured to any piece of chip design in favor of a more flexible model neurons.

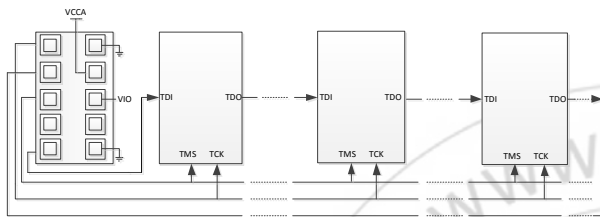


Figure4: Multi-chip FPGA JTAG daisy chain configuration

3. Multi-FPGA communication structure of neurons Experimental Platform:

3.1 Configuration Methods

3.1.1 DAC newsletter

A/D will introduce an external signal, for example in the study of neural feedback or synchronization, resonance, etc., should be introduced into the corresponding signal to the outside. Because the FPGA mainly deal with digital signals, it should be external analog signal is converted to the corresponding data signal, adding with a FPGA internal functioning of neuronal networks. We generally use a signal generator which generates a corresponding digital signal, after A/D conversion, added to the FPGA. Similarly, we use D/A to FPGA emulation signal, is connected to the oscilloscope to observe signals corresponding neuron discharge.

3.1.2 Real-time data communications design

Cypress (Cypress) of CY7C68013A classic USB2.0 protocol chip used with enhanced 8051 microcontroller, clock frequency 48Mhz. CYPRESS framework provides a very good program, eliminating the need for users to have written some of the relatively strong common mode of the program. On the basis of the framework, the user need only write the appropriate code in the appropriate place to complete USB work. General framework can be divided into three parts.

- 1)Descriptor file. For example dscr.a51 document, which defines the time to enumerate the device to use a variety of descriptor information, this part of the user according to the actual situation need to write your own.
- 2)The firmware file, for example FW.C file, which is a function of the hardware import program.
- 3)Functional document processing various interrupt. For example PERIPH.C file. 8051 general default only four

interrupt, which is obviously not enough to use USB, so CYPRESS introduced the concept of automatic vector, the equivalent of the soft interrupt, which greatly extends the existing number of interrupts.

4. Neural Network Platform PC

LabVIEW (Laboratory Virtual Instrument Engineering Workbench) as a graphics-based programming language, a standard data acquisition and control software. LabVIEW software, measuring instruments along with computer hardware to integrate, and then create a virtual instrument development system, the user can customize based on this programming design, while the LabVIEW graphical interface development environment allows programming man-machine interface of the PC more intuitive and simple programs written modularity also helps to understand and modify the program, and thus suitable for data acquisition and processing system display and analysis, is widely used in academic research, industrial areas . LabVIEW offers a variety of similar appearance and actual instrument control, very easy to establish in the design of man-machine interface. LabVIEW interface is shown in Figure 2-3, the main features include common configuration, real-time data display and feature analysis.

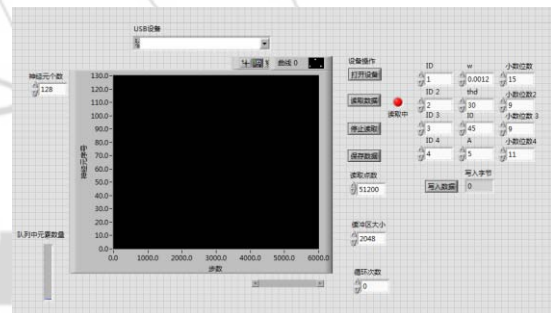


Figure5: Neural Network Platform PC

5. Neural Network Platform and Verification

Through the above analysis of the multi-FPGA systems, we use four hurricanes fourth generation of Altera's FPGA chip EP4CGX150DF27C8N as the core, preliminary exploration designed a neural network simulation platform, as shown. The topology of the platform in accordance with the form of a grid connection is connected, each one chip has 96 GPIO pin is connected to be able to meet most of the neuron model set up data communication with another three-piece chip; neuron simulation of multi-FPGA on the platform, using analog Devices (ADI) of AD9248, AD9767AST digital to analog and analog to digital conversion chip; with Cypress's experimental platform CY68031A USB chip hardware emulation platform data communication with the host computer in real time; In addition, experimental platform DM9000A chip using FPGA internal collect data; at the same time, the hardware simulation platform reserved for a large number of external ports, allows researchers hardware testing and functional expansion more convenient. We use Leaky integer-and fire (LIF) validity of the model test platform, the results shown: meet the rules FHN model discharges.

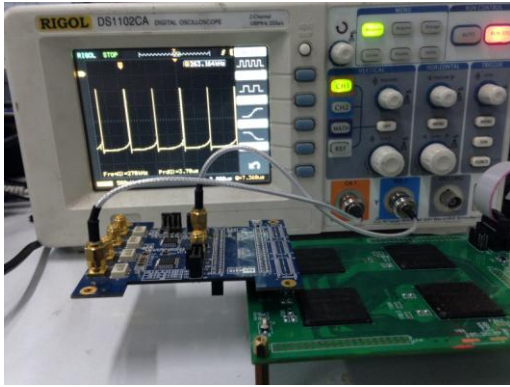


Figure 6: Multi-chip FPGA neural network simulation platform

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6. Conclusion

This paper describes the design of the design of multi-FPGA Platform explored. It describes the topology between multi-chip FPGA chip, including wired array structure, grid type, cross-connect and mixed interconnect type. And analyze the advantages and disadvantages of each method, through a comprehensive judging the final choice meshed topology. Then, the analysis of multi-chip FPGA chip clock synchronization using hardware method, using the clock buffer (CLOCK BUFFER) to a clock into multiple clock are supplied multi-chip FPGA used in conjunction sending and receiving chip timing analysis, solve the multi-FPGA chip data transfer clock synchronization problems. Finally, the multi-FPGA chip communication problems, describes three means of communication with the digital-analog converter chip inside the FPGA results displayed by the oscilloscope; the form of an Ethernet packet capture FPGA internal calculation result is stored, In the computer for data analysis and processing; transfer with USB chip inside the FPGA on LABVIEW written information to the host computer, to analyze real-time data. Finally, oscilloscope Leaky integer-and fire (LIF) neurons discharge model, conforming LIF neuron discharge characteristics. Demonstrate the effectiveness of the experimental platform.

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