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Design of the Add Multiply Operator Using Modified Booth Recorder

Sruthikeerthana V.M[1], Pavithra.S[2]

[1]PG Student, Department of ECE, Velalar College of Engg. & Tech., Thindal, Erode

[2]Assistant Professor, Department of ECE, Velalar College of Engg. & Tech., Thindal, Erode

Abstract: ***Add –Multiply operation it perform addition and result will be added to the input of multiplier. In proposed method s-mb recorder is used to the sum of two number in modified booth form. This technique implement the sum of two number in modified booth form. The sum to modified booth recoding it improve the performance of a different scheme of FAM unit. In existing method, Coventional design of the AM operator is implemented by using S-MB algorithm. The area, power dissipation and delay is increased by the use of adders. In proposed method, compressor adder is to be used instead of Carry select adder. The design is coded in VHDL and simulated in ModelSim and Synthesized in EDA tool Xilinx ISE9.2i . The power and delay will be reduced compare with existing methods.***

Keywords: Booth multiplication, fused add multiply operator, add-multiply operator,radix-4, radix-8

1. Introduction

The multiplier has different speed and area constraint is designed fully with parallel. The fastest type of multiplier is a parallel multiplier. The type of parallel multipliers are booth multiplier and parallel multipler. Wallace tree circuit is a irregular structure .The multiplication of Wallace tree is faster. Wallace tree circuit is not used in low power application because excess wiring is used so it increase the power consumption in multiplier Booth multiplier is the parallel multiplier. Booth multiplier has a signed operand it operate the two's complement form. Booth multipler is a high performance and low power consumption. Booth multiplier is used to different modes such as Radix-2, Radix-4, Radix-8 etc. The Radix-4 and Radix-8 is used to designing the FIR filter. The number of partial product will be reduce the Radix-4 and Radix-8.The disadvantage is generate the more multiples of multiplicand. Booth algorithm is a signed number multiplication. It uniformally treat both positive and negative number.Radix-8 multiplier it perform more than one multiplier in each cycle. The high speed multiplier decrease the subsequent calculation stage. The booth multipler has two drawback. The add and subtraction operation number is variable and inconvenient to designing the parallel multipliers. The algorithm is inefficient to isolated 1s.

The radix-4 modified booth algorithm overcome the limitation of radix-2 algorithm. The modified Radix-4 booth algorithm is used to equal to or greater than 16 bit. The encoding of a two's complement multiplier is reduce the number of partial Product. The Radix-8 booth recoding is apply the same algorithm in Radix-4. The quartet is codified in sign digit. Radix-8 algorithm is reduce the partial partial product in n/3,the n is the number of multiplier bit. Addition is used in arithmetic operation of microprocessor, digital signal processor and digital computer. The efficient implementation of arithmetic operation and binary ader is a very critical hardware unit. The electronics, adder is a digital circuit which perform addition operation. The modern computer adder in the arithmetic logic unit and other operation is also performed. The adder can be constructed from the many numerical representation, such as binary coded decimal and excess-3, the most common adder operate in binary number. The 2's complement is used to represent the binary number in trival to modify the adder. The carry select adder multiple level have small requirement and shortened computation time. The carry look ahead is a parallel prefix adder and represent the fastest addition scheme in large area complexity . The single bit adder has three general type. The half adder is a logic circuit and perform the addition in two binary digit. The half adder produce the sum and carry value in two binary digit. A full adder is a logic circuit and perform the addition in three binary digit.. The full adder produce sum and carry and both are in binary digit. And combine the other full adder .The multiplication accumulation computation is one of the fundamental operation in digital signal processing. The operation is applicable in digital signal processing, speech processing, video coding and communication etc. The MAC unit is a basic component of a digital signal processing and application specific integrated circuit. The increasing demand in protable electronic component and electronic component have low power consumption it leads to market trend. The algorithm used in MAC is

1) Radix-4 booth algorithm
2) Bough wooley algorithm
3) Booth algorithm
4) Modified booth algorithm

MAC addition is merged in to pps. The carry save addition perform in a Z datum and partial product in the multiplication, carry and sum value is generated.

2. Existing Method

The AM operator consist of input A and B is driven by the adder. The input X and Y=A+B is driven by the multiplier to get the output Z. The drawback is insert the delay in path of AM unit .The MB encoding technique is used in AM operator. An conventional AM operator is implemented using S-MB algorithm , and also the impact of power

consumption, hardware complexity and delay has been analyzed. The use of adder in existing method to increase area, delay and hardware complexity. To overcome these drawbacks, compressor adder is proposed and simulated. The signed half adder and full adder has three alternative scheme of S-MB recoding technique by radix-8 booth encoding

1) Smb1 recoding scheme.
2) Smb2 recoding scheme
3) Smb3 recoding scheme

The signed or unsigned number can easily apply the three scheme. It consist of odd and even number of bit. The input A and B consider the 2's complement form the 2k bits of even and 2k+1 of odd number of bit . The sum of A and B is transform in to MB form. .

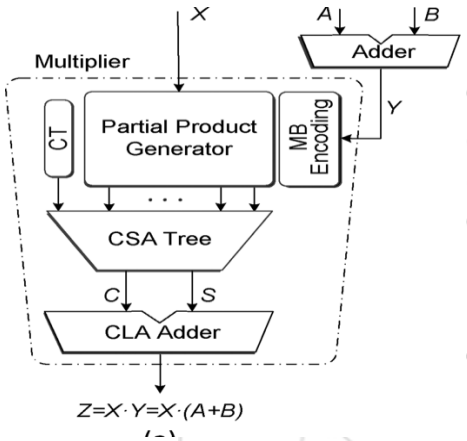

Figure 1: Coventional design of AM operator

3. Proposed Method

In proposed modification carry select adder instead of using compressor adder to reduce power, area and delay. The add-multiply input is x, a, b and while the output is z work, we propose modification to the carry select adder instead of using compressor adder to considerably reduce its power, delay and area. The design add-multiply consider the length of input is x, a and b while the output is z. The fus

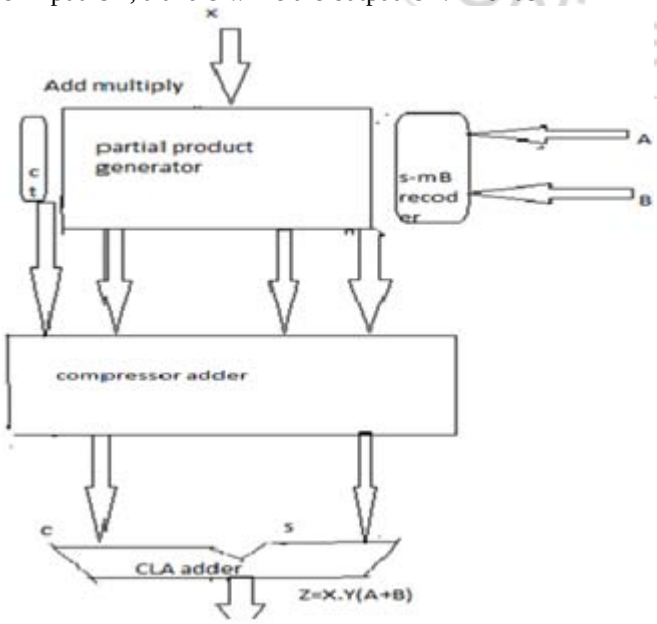

Figure 2: Fused design of the direct recoding

The design of AM operator is optimized by proposed system and introducing the fusion technique is based on the direct recoding of sum of two number in modified booth form. The sum of two number in modified booth form is a efficient implementation in the fused add multiply and will be compare to the existing one. The Smb technique is efficient implementation in sum of two number in modified booth form. The proposed technique yielding a considerable reduction in critical delay ,hardware complexity and power consumption in FAM unit.

FAM design having sum to modified booth algorithm technique is reduce the partial product and increase the speed of calculation. The delay, area and power consumption is decrease by the FAM technique. The proposed S-mb algorithm is a simple and easily modified in the signed and unsigned numbers it comprise the odd and even number of bits.

Partial product generator

The multiplier product is obtained by the multiplicand and multiplier process the more than one digit and calculating a large product use partial product in intermediate step .Partial product generator is generally produce the multiplicand in multiplication by 0,-1,1,4,-4.

1) 1.The product generator is multiplying the zero it is a multiplicand is multiply by zero. Multiply by 1 is a product remain same in multiplicand value.
2) 2.Multiply -1 is a product of two's complement form and multiply -2 is a shift the two's complement form

Carry Look Ahead Adder

Carry Look ahead the carry is faster and generate the additional circuit in parallel when input is change. In this technique carry bypass logic is used to speed the carry propogation. The ai and bi is the adudend input The carry output is a si and c_{i+1} . The pi and gi is the auxillary function and it is called propagate and generate signal.The carry look ahead adder is shown in fig 3.2

$P_i = a_i + b_i$
$g_i = a_i b_i$
$s_i = a_i$ xor b_i xor c_i
$c_{i+1} = g_i + p_i c_i$

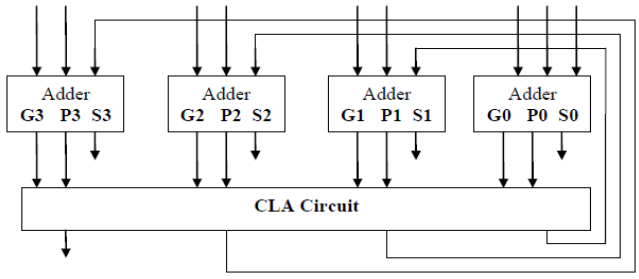

Figure 3: Four bit carry look ahead adder

4:2 Compressor Adder

The 4:2 compressor adder consist of 5 input has A,B.C,D and c_{in} produce the three output sum,C_{in} and C_{out} . The input and output has the same height. The input C_{in} is the output of previous compressor and Sth C_{out} is the output of next stage

compressor. This approach is implement the 4:2 compressor is shown in fig 3.3

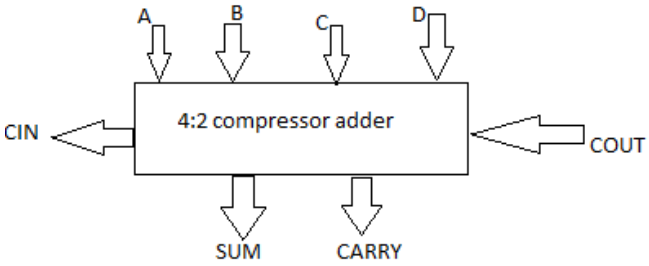

Figure 4 4:2 Compressor adder

4. Result Analysis

Table 1: Comparison of existing method

Parameter	Even bit	Odd bit
Delay	6.236ns	6.236ns
Area	260	175
Power	50nw	49nw

The fused-add multiply is a direct recoding the sum of two number in modified booth form. The fused add multiply consist of odd and even number of bit. The result obtained in odd and even number bit .VHDL coding of odd and even number bit is generated in modelsim and implemented in xilinxISE9.2i software in project navigator of FPGA

5. Conclusion

An conventional operator is implemented using S-MB algorithm and also impact of power consumption, hardware complexity, delay is increase. To overcome this drawback compressor adder is used in proposed method

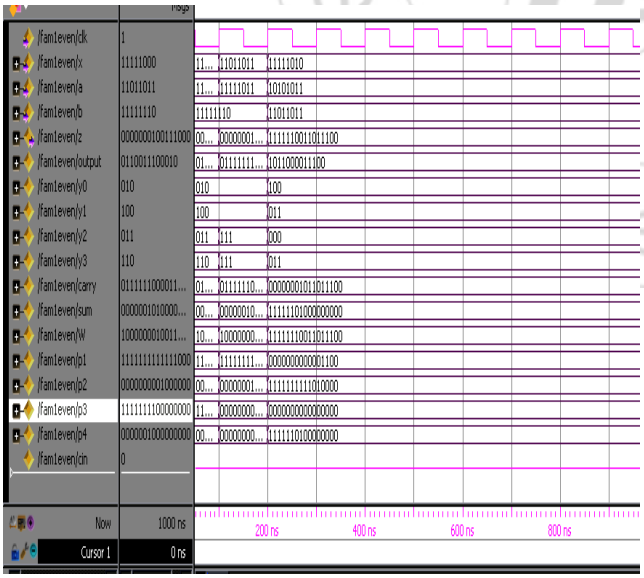

Figure 5: Waveform of even number of bit

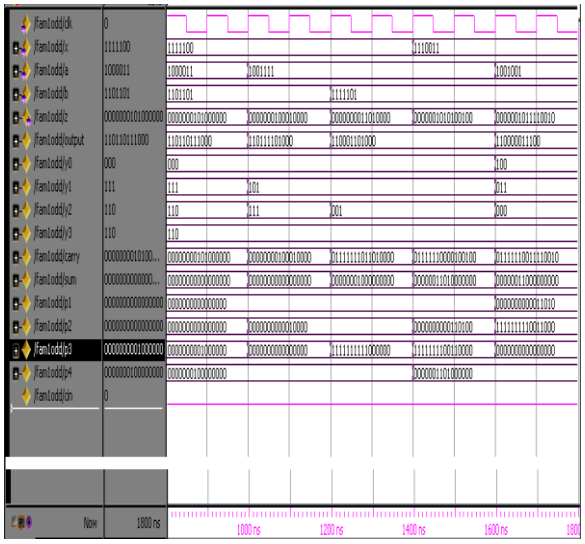

Figure 6: Waveform of odd number of bit

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