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Design and Analysis of BEC and GDI Technique Using Carry Select Adder

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Abstract: ***The overture of the work is focused on Carry Select Adder (CSLA), one of the fastest adders used to perform arithmetic functions. The logic operations involved in conventional carry select adder (CSLA) and Binary to Excess-1 Converter (BEC)-based CSLA are analyzed to review the data dependence and to identify redundant logic operations. All the redundant logic operations found in the conventional CSLA are removed and a new logic formulation for CSLA has been proposed. Because of complex digital signal processing (DSP) system involves several adders, an efficient adder design essentially improves the performance of a complex DSP system and FCSA does this work. Modified GDI logic architecture concentrates on the area level & fast carry selections. The fixed Carry Selections of different stage parallel adder i.e. (Cin=0, 1) is directly based on the GDI technique. This concept provides less area and low delay than previous SQRT-BEC CSLA.***

Keywords: DSP, SQRT, BEC, FCSA, CSLA

1. Introduction

The integrated circuits production capability, dependability, and building-block approach to circuit design ensured the fast adoption of standardized ICs in situ of designs using discrete transistors. Here the hot spot is combinational circuit, that the basic portion of the combinational circuit is Adder. A complex digital signal processing (DSP) system involves many adders. A ripple carry adder (RCA) uses a simple design, however carry propagation delay (CPD) is the main worry in this adder. Carry look-ahead and carry select (CS) methods have been suggested to reduce the CPD of adders [1],[2].Low power, area-efficient, and high-performance VLSI systems are progressively employed in compact and mobile equipments, wireless receivers, and bio medical instrumentation [2][3]. A conventional CSLA has less CPD than RCA, however the design is not appealing because it uses a dual RCA. Few tries have been made to avoid dual use of RCA in CSLA design. A conventional carry select adder (CSLA) is a dual RCA arrangement that generates a duo of sum words and output carry bits analogous to the anticipated input-carry (C_{in} =0 and 1) and chooses one out of each duo for final-sum and final output carry. Within the previous strategies of adder designs, logic is optimized while not giving any consideration to the data dependence [1]. In this proposal, we made an analysis on logic operations involved in conventional and BEC-based CSLAs with GDI.

The carry selections in the GDI technique are taken into account to study the data dependence and to identify redundant logic operations. As well as on the basis of this analysis, we have proposed a logic formulation for the GDI CSLA. The main contribution is the logic formulation based on data dependence and optimized carry generator (CG) and CS design. On the basis of the proposed logic formulation, we have derived a productive logic design for CSLA. Due to optimized logic units, the proposed CSLA involves significantly reduced ADP than the existing BEC-CSLAs. We have shown that the GDI based SQRT-CSLA using the proposed CSLA design involves nearly 45% less ADP and consumes 40% less energy than that of the corresponding SQRT-CSLA.

Carry Select Adder

A conventional carry select adder (CSLA) is an RCA–RCA configuration that produces a pair of sum words and output carry bits analogous to the anticipated input-carry (Cin =0 and 1) and chooses one out of each duo for final-sum and final output-carry. A conventional CSLA has less CPD than an RCA, but the design is not attractive because it uses a dual RCA. Few tries have been made to avoid dual use of RCA in CSLA design. Layout of area and power adeptive high speed data path logic systems is one of the major substantial areas of research to perform arithmetic calculations in VLSI design. There is a scope for reducing area and delay in digital adders, the speed of addition is restricted by the time required to propagate through the adder. The sum for each bit position in an elementary adder is generated gradually only after the preceding bit position has been summed and a carry propagated into the later position. The CSLA is used in many computational systems design to moderate the problem of carry propagation delay by separately producing multiple carries and then select a carry to produce the sum. It uses independent ripple carry adders (for C_{in}=0 and C_{in}=1) to produce the sum. But, the regular CSLA is not area and speed efficient as a result of it uses multiple pairs Ripple Carry Adders (RCA) to produce partial sum and carry by considering carry input. The final sum and carry are selected by the multiplexers (MUX). Due to the use of two independent RCAs the area will increase which leads to an increase in delay. To overcome the above problem, the basic idea of the proposed work is to use n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be replaced in RCA for Cin=1 to further improves the speed and thus reduces the delay. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA will achieve lower area, delay which speeds up the addition operation.

The Carry select adders are classified as Linear Carry select adder and Square root Carry select adder. The linear carry select adder is constructed by chaining a number of equal length adder stages. For an n-bit adder, it could be implemented with equal length of carry select adder and is called as linear carry select adder. The square-root carry select adder is constructed by equalizing the delay through two carry chains and the block multiplexer signal from previous stage. It is also called as non-linear carry select adder. The existing modified SQRT CSLA uses Binary to Excess-1Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower delay with slightly increase in area.

The basic idea of the proposed architecture is that which replaces the BEC logic by Common Boolean Logic. The proposed architecture generates a duplicate sum and carry-out signal by using NOT and OR gate and select value with the help of multiplexer. From the structure of regular SQRT CSLA, there is scope for reducing delay and area utilization. The carry out is calculated from the last stage. Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structure becomes a very critical hardware unit. In digital adders, the sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The Carry Select Adder is used in many computational systems to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

A carry-select adder is divided into sectors, each of which except for the least-significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. A four bit carry select adder generally consists of two ripple carry adders and a multiplexer. The carry-select adder is simple but rather fast, having a gate level depth of $O(\sqrt{n})$. Adding two n-bit numbers with a carry select adder is done with two adders (two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

Next we move on to the functional formulation where we describe the existing and the proposed methods.

2. Functional Formulation

In this section we concentrate the overall functional logic formulations method. The GDI concept is taken from the Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit [4] by Partha Bhattacharyya.

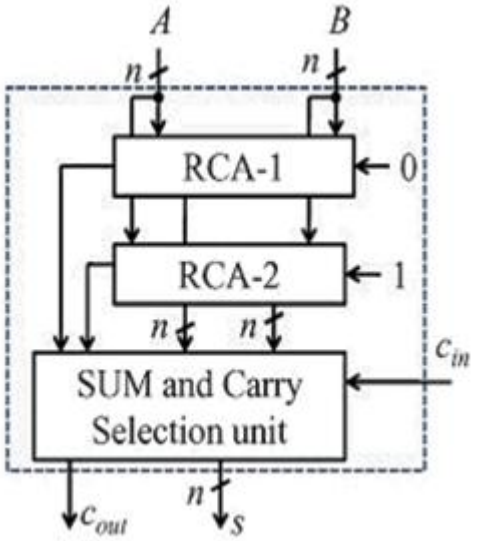

Figure 1: Basic structure of CSLA

The CSLA is originally started in RCA [5]. The main objective of this study is to identify redundant logic operations and data dependence. A conventional carry select adder (CSLA) is an RCA–RCA configuration that generates a pair of sum words and output carry bits corresponding the anticipated input-carry (Cin =0 and 1) and selects one out of each pair for final-sum and final-output-carry. A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA. Few attempts have been made to avoid dual use of RCA in CSLA design. A carry select adder is divided into sectors, each of which, except for the least significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one within the sector, there are two 4-bit Ripple Carry Adders receiving the same data inputs but different Cin.

There are two 4-bit Ripple Carry Adders receiving the same data inputs but different Cin. The upper adder has a C_{in} =1. The actual C_{in} from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carry-out of the upper adder are selected. If the carry-in is one, the sum and carry-out of the lower adder are selected. Logically, the result is not different if a single ripple carry adder were used. First the coding for full adder and different multiplexers was done. Then ripple carry adder was done by calling the full adder. As shown in Figure 1.1, the SCG unit of the conventional CSLA is composed of two n-bit RCAs where n is the adder bit-width. The logic operation of the n-bit RCA is performed in four stages: 1) half-sum generation (HSG); 2) Half-Carry Generation (HCG); 3) Full-Sum Generation (FSG); and 4) Full Carry Generation (FCG).

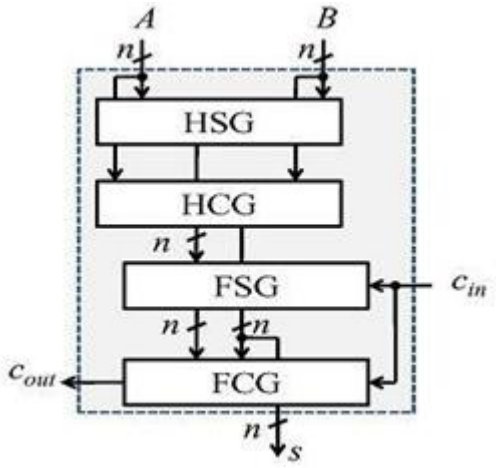

Figure 1.1: the logic operations of RCA

Suppose two n-bit operands are added in the conventional CSLA, then RCA-1 and RCA-2 generate n-bit sum (s0 and s1) and output-carry (c0out and c1out) corresponding to input-carry (Cin = 0 and Cin = 1), respectively. Logic expressions of RCA-1 and RCA-2 of the SCG unit of the n-bit CSLA are given

$$s_0^0(i)=A(i)\oplus B(i)\ c_0^0(i)=A(i).B(i) \quad (1)$$
$$s_1^0(i)=s_0^0(i)\oplus c_1^0(i\text{-}1) \quad (2)$$
$$c_1^0(i)=c_0^0(i)\oplus s_0^0(i).c_1^0(i\text{-}1)\ cout_0=c_1^0(n\text{-}1) \quad (3)$$
$$s_0^1(i)=A(i)\oplus B(i)\ c_0^1(i)=A(i).B(i) \quad (4)$$
$$s_1^1(i)=s_0^1(i)\oplus c_1^1(i\text{-}1) \quad (5)$$
$$c_0^1(i)=c_0^1(i)\oplus s_0^1(i).c_1^1(i\text{-}1)\ cout_1=c_1^1(n\text{-}1) \quad (6)$$

Where $c^0 1(-1) = 0$, $c^1 1(-1) = 1$, and $0 \le i \le n-1$.

As shown in (1)–(6) and (4)–(6), the logic expression of{ $s_0^0(i)$,$C_0^0(i)$}is identical to that of {$s^1{}_0(i)$, $c^1{}_0(i)$}.These redundant logic operations can be removed to have an optimized design for RCA-2, in which the HSG and HCG of RCA-1 is shared to construct RCA-2. Based on this, an add-one circuit instead of RCA-2 in the CSLA, in which a BEC circuit is used in for the same purpose. Since the BEC-based CSLA offers the best area–delay–power efficiency among the existing CSLAs, we discuss here the logic expressions of the SCG unit of the BEC-based CSLA as well. In a SQRT CSLA, CSLAs with increasing size are connected in a cascading structure. The main objective of SQRT-CSLA design is to provide a parallel path for carry propagation that helps to reduce the overall adder delay.

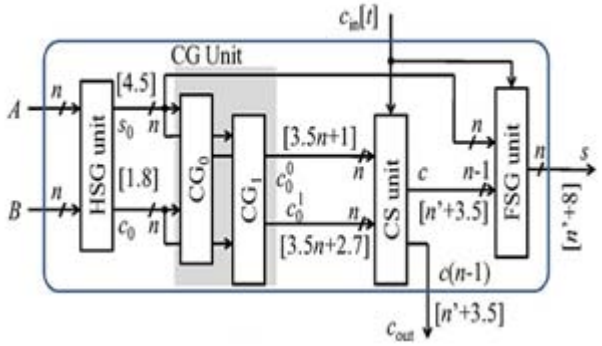

Figure 2: BEC-SQRT structure CSLA

The figure 2 intimate the final sturcutre of SQRT-BEC CSLA[1].which provide less delay (apprx 33%)than previous convolutions based CSLA.The carry selection formula is based on the below eqn due to get low propagations delay.

$$S1[0]=\sim s[0] \quad (7)$$
$$C1[0]=s[0] \quad (8)$$
$$S1[i]=s[i\text{-}2]\hat{}c[i\text{-}1] \quad (9)$$
$$C1[i]=s[i\text{-}2]\&c[i] \quad (10)$$

The $S_1[0]=\sim s[0]$ describes the sum selcetions of 2nd stage adder. Furtherly $C_1[0]=s[0]$ shows the carry selections of second stage carry selections unit.$S_1[i]$,$C_1[i]$ vice versa;where i is the number of digits in the adder design.

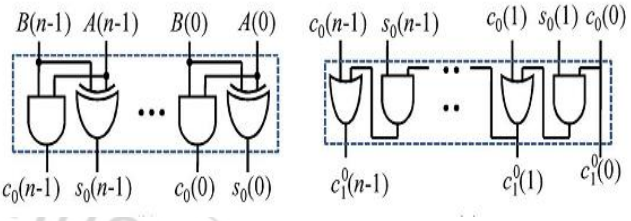

Figure 3:AND and OR gate based Adder design.

The figure 3 shows the N number of bit adder design ,this sturcture is taken from the fast CSLA adder[4].It the CG unit is composed of two CGs (CG_0 and CG_1) corresponding to input-carry „0‟ and „1‟. The HSG receives two n-bit operands (A and B) and generate half-sum word s0 and half-carry word c0 of width n bits each. Both CG0 and CG1 receive s0 and c0 from the HSG unit and generate two n-bit full carry words c_{01} and c_{11} corresponding to input-carry „0‟ and „1‟, respectively.

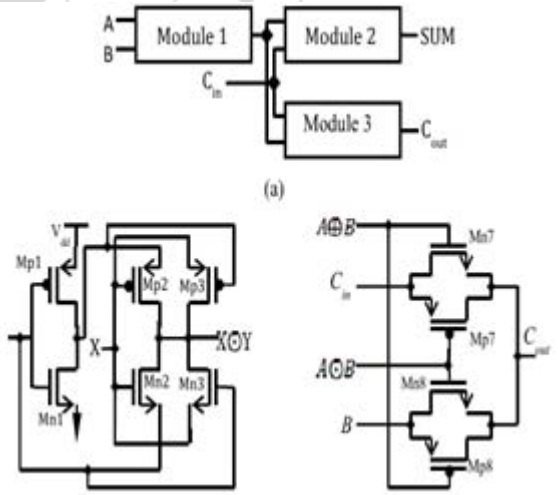

Figure 4: The single bit full adder desing module by using GDI

The figure 4 clearly explain the transitor selections of single bit full adder circuit by using GDI technique[2].from this concept we have to think how about multi bit adder circuit,how to reduce area and dely finally we proved this design is well suited for high speed multiplier design.as well as low area multi bit full adder design.For this design we had chosen Tanner 13 tool initially next xilinix.

Due to early generation of output-carry with multipath carry propagation feature, the CSLA design is more favorable than the existing CSLA designs for area–delay efficient implementation of SQRT-CSLA. To do design an efficient CSLA by using optimized logic units. The proposing CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA.

The proposed method would initiate the GDI(Gate Diffusion Input) Technique,and it will be Modify for getting suitable low power digital circuits design further to reduce the swing degradation problem. This techniques allows reduction in power consumption, carry propagation delay and transistor count of the carry select adder too.An adder is the main component of an arithmetic unit. A complex digital signal processing (DSP)system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system[7].

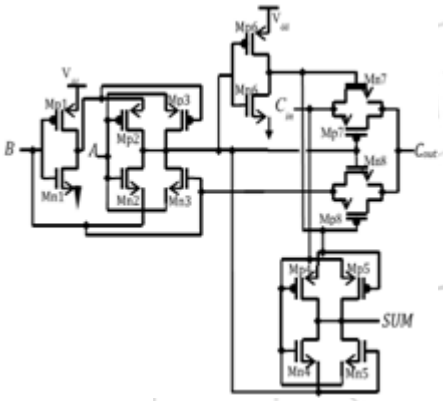

Figure 5: Full adder sum and carry selections based on modified GDI Technique

This arrangement of modified GDI cell provides reduction in both sub threshold and leakage power compared to static CMOS gate. Mod-GDI is more suitable while designing of high speed, low power circuits by using reduced number of transistors as well as improved swing degradation and static power characteristics. This logic allows simple top-down design by using a small cell library . Mod GDI logic performance is testable, so that Mod-GDI logic and logic circuit design methods is hopeful for design a low power and high performance applications. The basic Gate Diffusion Input (GDI) logic style suffers from some of the practical limitations like swing degradation, fabrication complexity and bulk connections. These limitations can be overcomed by modified gate diffusion input (Mod-GDI) logic[2]. This modified gate diffusion input (Mod-GDI) logic allows reduction in power consumption, delay and area of digital circuits.We can ensure that the Mod-GDI cell can be implemented with all current CMOS technologies. In Mod-GDI cell, the bulk node of all PMOS transistors are connected to VDD and bulk node of all NMOS transistors are connected to GND. Mod-GDI cell uses standard 4 terminal NMOS and PMOS transistors and it provides ease of implementation in all type of standard CMOS technology.

Mod-GDI is more suitable while designing of high speed, low power circuits by using reduced number of transistors as well as improved swing degradation and static power characteristics. This logic allows simple top-down design by using a small cell library [8]. Mod - GDI logic performance is testable, so that Mod-GDI logic and logic circuit design methods is hopeful for design a low power and high performance applications.

Table 1: Various logic function implementation with Mod-GDI logic

S_N	S_P	G	P	N	D	FUNCTION
0	1	A	1	0	A‟	INVERTER
A	A	B	0	A	AB	AND
0	D	B	A	1	A+B	OR
0	A	B	A	A‟	A‟B+AB‟	XOR
0	A	B	A	A	AB+A‟B‟	XNOR
0	1	A	B	C	A‟B+AC	MUX

Mod-GDI based bit selections

The logic values and the functions for each of the logic value is shown in the tabulation.Using this we have to formulate the worthfull equations for Fast Carry Selection Adder(FCSLA) which is described below:

```
if(c[0]&&c[1] )
fastcla[0]=1'b1;
else
fastcla[0]=1'b0;

if(c[1]&&c[2] )
fastcla[1]=1'b1;
else
fastcla[1]=1'b0; vice versa…..
```

The logical Equations is designed and simulated by using Xilinix 14.7v ,the synthesis and simulations result is described by below sections.

3. Synthesis and Simulations Results

The simulation and synthesis work is finally done by the xilinix and modelsim.initially the desing is done by the tanner.

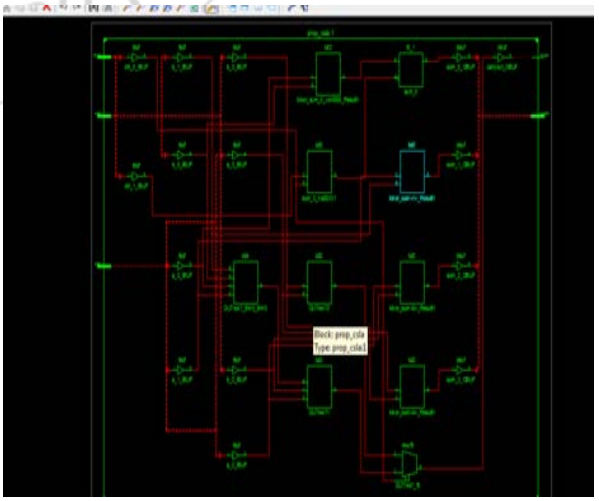

Figure 6: Synthesis results of BEC-SQRT design.

The figure intimates the BEC-SQRT proposed carry select adder,which is the combined form of conventional and binary to excess code conversion method.By this work we

confirmed the over all area of the adder is reduced by comparing previous method .The area related to delay of both logic and routing is also reduced .We got this result by analysing Look Up table:

Total delay 7.716ns (6.219ns logic, 1.497ns route)
(80.6% logic, 19.4% route)
Carry selections delay 4.368ns (3.948ns logic, 0.420ns route)
(90.4% logic, 9.6% route)
From the SAED 90nm technology Cell library data sheet the area,delay of the OR,NOT,AND gates[1] are is below:

The use of less number of transistors in this GDI concept also improved the speed. Because of reduction in average power consumption and propagation delay, the PDP of the proposed hybrid FCSLA is significantly improved in comparison with the earlier hybrid adders.

Table 2: Area of AND, OR, AND NOT gates are given in the 90nm standard cell library datasheet.

	AND-gate	*OR-gate*	*NOT-gate*
Area (µm^2)	7.37	7.37	6.45
Delay (ps)	180	170	100

Figure 7: Synthesis diagram of FCSLA

The figure 7 is designed by using verilog language with xilinix synthesis tool.for this design we had to use 16 bit carry select adder.with GDI Concept.

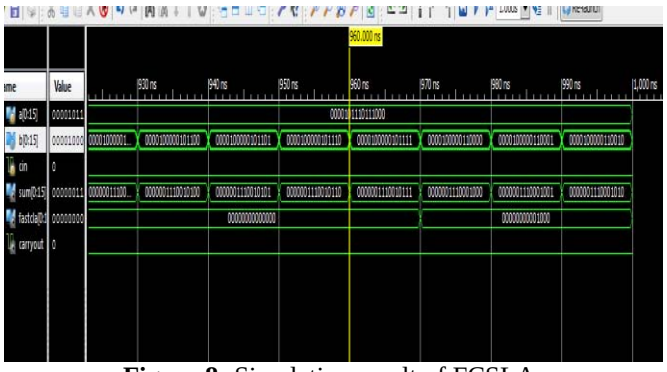

Figure 8: Simulation result of FCSLA

The figure 8 shows the simulation result of the FCSLA,which is checked by the random test bench code in xilinix tool.Here we have to reduce almost best case redundancy minimizations.The wave form indicates the flag register to intimate the final bit(0,1)of every sum,because of Ex-OR gate is enable if odd number of one is there.The final delay and area of the FCSLA is below:

```
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: 2.852ns
   Maximum output required time after clock: 4.368ns
   Maximum combinational path delay: 6.320ns
```

Figure 9: Snap of compinational path delay from the xilinix

The wired delay also reduced by perfect RTL coding,here we never allowed the latch forming that‟s why we achieved less combinational delay i.e 6.320ns.

Conclusion

From the analysis of various CSLA finally we had chosen the BEC-CSLA with SQRT technology for high speed Carry selections and modified this concept with GDI technology. we had achieved less area and low delay compared to BEC-CSLA,but we could not solve the power reductions.i.e we have same amount of power consumption as that in SQRT-BEC CSLA.The originality of the simulations and synthesis are designed and analysed.The reudundancy bit is reduced almost 100%.We had analyzed logic formulations involved in SQRT-BEC CSLA for the indivitual carry selcetions and the GDI based design is used.

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Author Profile

Mohitha.I.K received the B.E degree in Electronics and Communication Engineering from JCT College of Engineering and Technology in the year 2014. Her research areas include testing of VLSI, Advanced Signal Integrity for high speed digital designs, CAD for VLSI, Imaging and signaling analysis for multimedia, biomedical, wireless communication, Analog Design,3D IC"s and DSP Processors.