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A Review: FPGA Implementation of Reconfigurable Digital FIR Filter

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Abstract: ***This brief presents, the different methods namely conversion based approaches and memory based methods for implementation of FIR filter. It also presents an efficient implementation of Finite Impulse Response Filter (FIR) using Distributed Arithmetic (DA) architecture. The distributed arithmetic is an area efficient technique of FIR filter implementation. The existing methods have used MAC units, which need more hardware, area and power. The multipliers in FIR filter are replaced with multiplier less DA based technique. The DA based technique consists of Look Up Table (LUT), shift registers and scaling accumulator. Replacing MAC with LUT-Based DA algorithm is having power, efficiency and less area usage. With the reduction of hardware in terms of multipliers, our goal is to reduce the parameters namely, hardware, area and power.***

Keywords: RAM based LUT, Distributed Arithmetic, Conversion based approach, Field Programmable Gate Array, FIR Filter.

1. Introduction

Digital Signal Processing (DSP) has been increasing in popularity due to the decreasing cost of general purpose computers and Application Specific hardware [11]. Since many telephony and data communications applications have been moving to digital, the need for digital filtering methods is growing continue. In the electronic industry, there is a device known as Digital filters which are capable of taking digital input, process them and provide digital output [12]. A digital filter is a system that performs mathematical operations on a sampled discrete-time signal to reduce or enhance certain aspects of that signal. The two major types of digital filters are finite impulse response digital filters (FIR filters) and infinite impulse response digital filters (IIR). Finite Impulse Response (FIR) filters are one of the most common components of Digital Signal Processing (DSP) systems. FIR filtering is achieved by convolving the input data samples with the desired unit response of the filter [17].
In many digital signal processing (DSP) and image processing applications finite impulse response (FIR) digital filter is widely used as a basic tool because of their absolute stability and linear phase property. The low-complexity and high speed digital finite impulse response (FIR) filters find widely use in mobile communication systems and multimedia applications such as channelization, channel equalization, matched filtering, and pulse shaping, video convolution functions, signal preconditioning and various communication applications because of less area, low cost, low power and high speed of operation. The disadvantage is that the number of computations to process a signal is more, it requires high order and because of this more hardware, area and power consumption is required. As the filter order increases the number of multiply-accumulate (MAC) operations required per filter output also increases therefore the complexity of implementation of FIR filter increases [10]. Therefore to develop dedicated and reconfigurable architectures for realization of FIR filters in Application Specific Integrated Circuits (ASIC) and Field-Programmable Gate Arrays (FPGA) platforms, several attempts have been made. FPGA offers many advantages for many applications. Multiplier-based filter implementations may become highly expensive in terms of area and speed. This problem has been partially solved with the low-cost FPGAs that have embedded DSP blocks.

In literature, various multipliers-less schemes had been proposed. These methods can be classified in two categories according to how they operate the filter coefficients for the multiply operation. The first type of multiplier-less technique is the conversion-based approach and the second type of multiplier-less method includes use of memories (RAMs, ROMs) or Look-Up Tables (LUTs) to store pre-computed values of coefficient operations.

In the next section, the literature survey of implementation of FIR filter and the methods for FIR filter design is briefly discussed.

2. Literature Survey

Over the past year, the software radio has proposed whose ultimate idea was the expansion of digital signal processing towards the antenna [2]. This technique was popular worldwide by reason of strong demand of reconfigurable communication systems. The main reason for replacing analog signal processing with digital signal processing was the possibility to softly reconfigure the system, where they defined important functionalities of digital front-end and focus on the signal characteristics of mobile communications signals and unities among different signal processing operations.

After some years the digit reconfigurable finite impulse response filter architecture has been designed with a very fine granularity which provided a flexible yet compact and low power solution to FIR filters with a wide range of accuracy and tap length [3]. The digit processing unit has designed for implementation of FIR filter. By cascading several DPUs, properly arranging the multiplexers in those DPUs, and

summing up all the output of the DPUs and then accumulated sum, they have implemented an FIR filter with variable number of CSDs in each tap. For the last digit of each tap, the multiplexer in the corresponding DPU selected the buffered data as the output.

In recent years, the distributed arithmetic algorithm based techniques has grown popularity because it is used to produce very efficient filter design. But the memory requirement for DA-based implementation of FIR filters exponentially increases with the filter order. So to overcome the problem of such large memory requirement, systolic decomposition techniques are suggested. The 1-D and 2-D fully pipelined structures has designed which gives area-power-delay efficient implementation of FIR filter [5], [6]. This scheme presented the use of address length of LUT's for computation based on DA. If the smaller address length for DA-based computing units is used, then memory size is reduced. But that leads to increase the adder complexity and latency. The FIR filter by using DA algorithm is easy to implement. The reconfigurable FIR filter whose filters coefficients dynamically change need to be implemented in future work, where the rewritable RAM based LUT would be used.

The multipliers-less schemes have explained below. These methods can be classified in two categories according to how they manipulate the filter coefficients.

2.1 Conversion based Approach

In this method, the coefficients are transformed to other numeric representations whose hardware implementation or operation is more efficient than the traditional binary representation. Example of such techniques are the Canonic Sign Digit (CSD) method, in which coefficients are represented by a combination of powers of two in such a way that multiplication can be simply implemented with adder/subtractors and shifters. And another type is the Dempster-Mcleod method, which likewise includes the representation of filter coefficients with powers of two but in this case arranging partial results in cascade to present further savings in the usage of adders [13].

2.2 Memory based Method

This type of method involves use of memories (RAMs, ROMs) or Look-Up Tables (LUTs) to store pre-computed values of coefficient operations.

These memory-based methods include Constant Coefficient Multiplier method and the very-well known Distributed Arithmetic method as examples [12].

Distributed Arithmetic (DA) algorithm seemed as a very effective solution especially suitable for LUT-based FPGA architectures. Croisier et al [14] had proposed the multiplier less architecture of DA algorithm and it is based on an effective partition of the function in partial terms using 2's complement binary representation of data. The partial terms can be computed first and stored in LUTs. Yoo et al. [15] detected that the requirement of memory/LUT capacity increases exponentially as the filter order increases, given that DA implementations need 2K words, *K* is the number of taps of the filter.

2.2.1 Distributed Arithmetic

In the case of FPGA implementation we cannot consider that much trade off in area, because the area specification of the FPGA is fixed. So we need to study the efficient implementation algorithm. Here we presented the Distributed Arithmetic algorithm to decrease the number of addition and multiplication. By using this method we can make sure that the area of the FPGA is reduced.

Distributed arithmetic is a bit level rearrangement of a multiply accumulate to hide the multiplications [12]. It is a powerful technique for reducing the size of a parallel hardware of multiply-accumulate that is well suited to FPGA designs. The DA targets the products of sums which cover all filtering application and frequency transfer functions. DA uses Look-Up Table (LUT) which stores the constant coefficients of FIR Filter. Distributed Arithmetic (DA) Algorithm can be used to replace MAC unit. Replacing MAC with LUT-Based DA algorithm is having efficiency and less area usage, more speed and low power consumption and less hardware complexity. By the reduction of arithmetic in terms of multipliers, our goal is to reduce the parameters namely, hardware, area and power. This is ultimate goal of the implementation of an efficient FIR filter and hence DA algorithm uses for implementation of high order FIR filter. The use of lookup tables reduces the hardware complexity and hence the design of FIR filter using Distributed Arithmetic algorithm is more efficient [1].

3. Comparison of Method

The comparison of different methods has given in the following table 1.

Table.1. Methods of FIR filter implementation

Sr.no.	*Methods*	*Examples*	*Component Used*
1	Conversion based approach	Canonical signed digit	Adders, Subtractors, Shifters
		Dempster-Mcleod method	Adders
2	Memory based methods	Constant Coefficient Multiplier method	RAM, LUTs, ROM
		Distributed Arithmetic method	RAM, LUTs, ROM

4. Proposed Method

The proposed structure of the reconfigurable FIR filter implementation by using DA algorithm, which gives high-throughput is given in fig. 1. The filter coefficients of this filter change during runtime.

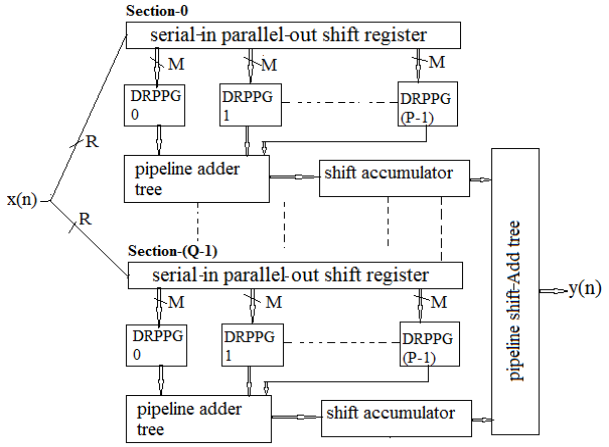

Figure 1: Proposed structure of the DA- based FIR filter for FPGA implementation

The LUT are required to be implemented in RAM for reconfigurable DA-based implementation of FIR filter. RAM based LUT is costly so a shared LUT design is proposed for FIR filter design. The DRAM (distributed RAM) based design is proposed for FPGA implementation of the reconfigurable FIR Filter [1]. The multiple numbers of partial inner products cannot be recovered from the DRAM simultaneously since only one LUT can be read from the DRAM per cycle. Using a DRAM to implement LUT for each bit slice will result in very high resource consumption. Thus we have to decompose the partial inner product generator into Q parallel sections and each section has R time multiplexed operations corresponding to R bit slices. The proposed structure has Q sections which consist of P number of DRPPGs (Distributed RAM Reconfigurable Partial Product Generator) is of M length, Pipeline Adder Tree and Shift Register that perform over R cycles. We have R time slots of the same duration so that we can have one filter output at every R cycle. Finally the Pipeline Shift Adder Tree produces the filter output using the output from each section every R cycles.

5. Conclusion

The distributed arithmetic has proved to be an area efficient technique of FIR filter implementation. The algorithm of distributed arithmetic is extremely simple and its applications are broad. Slicing of LUT of desired length can be effective for high order filter designs. The high throughput reconfigurable FIR digital filter could be implemented by using Distributed arithmetic. So the parameters namely area, power, hardware complexity can be reduced. The hardware cost could be reduced by sharing the same LUT by the DA units for different bit slices.

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