An Optimized Design of High-Speed and Energy-Efficient Carry Skip Adder with Variable Latency Extension

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Abstract: *The portable equipments such as cellular phones, Personal Digital Assistant (PDA), and notebook personal computer, arise the need of effective circuit area and power efficient VLSI circuits. Addition is the most common and often used arithmetic operation in digital computers and also, it serves as a building block for synthesis all other arithmetic operations. Low-power and high-speed adder cells (like carry skip adder) are used in battery operation based devices. Now the biggest challenge is reduction of adder power consumption and delay while maintaining the high performance in different types of circuit design. In conventional carry skip adder the multiplexer is used as a skip logic that provides a better performance and performs an efficient operation with the minimum circuitry. Even though, it affords a significant advantages there may be a large critical path delay revealed by the multiplexer and also it containing twelve transistors that leads to increase of area usage and power consumption. The proposed method uses compound gates such as AOI and OAI as skip logic in the design that leads to decrease area usage, delay and power consumption, also in addition the parallel prefix adder is included to attain further reduction of power. The design is coded in VHDL and simulated in ModelSim and its area, delay and power are analyzed using Xilinx_ISE 9.2i.*

Keywords: Carry skip adder, high performance, concatenation incrementation CSKA, parallel prefix adder

1. Introduction

Adders are key building blocks in ALU (**A**rithmetic and **L**ogic **U**nit) and hence increasing their speed and reducing the power consumption of it adversely affect the parameters of the processors such as speed and power consumption. It is one of the most important components of a CPU (**C**entral **P**rocessing **U**nit). Fast adders are necessary in ALU, for computing memory addresses, and in floating point calculations. In addition, Full-adders are important components in other applications such as **D**igital **S**ignal **P**rocessors (DSP) architectures and microprocessors. Therefore, careful optimization of the adder is more important. This optimization can be done either in the logic or circuit level way. Circuit optimizations manipulate transistor sizes and circuit topology to optimize the speed. On the other hand, logic level optimization tries to rearrange the Boolean equations so that a faster or smaller even less power consumption circuit is obtained. On the other hand, increasing demand for portable equipments such as cellular phones, **P**ersonal **D**igital **A**ssistant (PDA), and notebook personal computer, arises the need of using area and power efficient VLSI circuits.

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. The computers in modern form have adders that reside in the arithmetic logic unit, where other operations are also performed. Low-power and high-speed adder cells are used in battery operation based devices. Now the biggest challenge is to reduce the adder power

consumption while maintaining the high performance in different types of circuit design. Up until now, the power consumption has not been of great concern because of the availability of large packages and the other cooling techniques having the capability of dissipating the generated heat. The carry skip adder is one of the fastest adders used in many digital processors to perform arithmetic operations.

Kantabutra V.,[7] described a method for designing optimum-speed one-level carry skip adders. The one-level carry skip adder is designed with an optimum speed by a method that yields a fastest adder if the ripple time (a circuit parameter) of a carry signal is a linear function of the number of bit positions that the carry signal propagate through, and if the skip time (another circuit parameter) of a carry signal is a linear function of the number of blocks of bit positions skipped by the signal, or if these two parameters are such mildly non-linear functions that they can be modeled by a linear function without any effect on any of the results obtained. In this paper, delay reduced based on skip logic in single level but increase in area, excess power consumption and also less regular layout.

Chirca et al K.,[3] compared a carry skip adder by various existing logic styles. The most timing critical part of logic design usually contains one or more arithmetic operations, in which addition is commonly involved. In VLSI applications, area, delay and power are the important factors which must be taken into account in the design of a fast adder. The carry-skip adder reduces the time needed to propagate the carry by skipping over groups of consecutive adder stages, is known to be comparable in speed to the carry look-ahead technique while it uses less logic area and less power. In this, a design of 8-bit carry skip adder by various existing logic styles are to be compared quantitatively and

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qualitatively by performing detailed transistor-level simulation. In this paper, lower propagation delay and high performance but requires more area and large power consumption.

Alioto M. and Palumbo G.,[1] proposed a carry skip adder design for the achievement of minimum delay with the following two steps. One is a timing consideration based sizing in an analytical way and next is to attain a desired number of bits by a successive refinement. This paper, high performance and minimal circuitry is produced but having high critical path delay.

Milad Bahadori, Mehdi Kamal and Ali Afzali-Kusha,[8] presented a structure of carry skip adder with a high speed and low power consumption. In many of the works only the speed is considered as an important parameter rather than the area usage and the power consumption. The multiplexers that acting as a skip logic provides a large critical path delay eventhough it has a faster speed. The conventional carry skip adder having an optimum structure and it provides a better performance with the skip logics. But in the skip logic multiplexer is used, which reveals a large portion of critical path delay and the 2:1 multiplexer containing 12 transistors that leads to increase in area usage and power consumption.

2. Carry Skip Adder

The carry skip adder comes under the category of a by-pass adder and it uses a ripple carry adder for an adder implementation. The formation of carry skip adder block is attained by improving a worst-case delay. The carry skip adder has a critical path, that passes through all adders and stops at the sum bit but actually it starts at first full adder. This adder is an efficient one according to its area usage and power consumption. The structure of 4 bit carry skip adder is shown in fig.1.
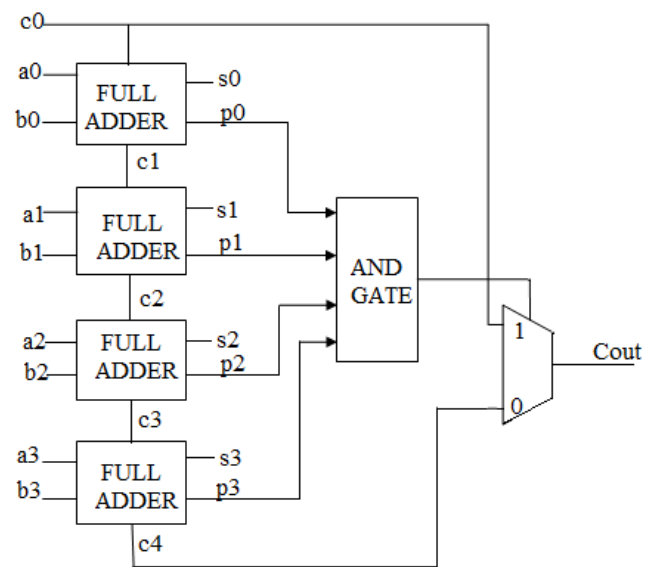

Figure 1: Four bit carry skip adder

In CSKA the wiring lengths is short and also having a simple and regular layout because of the smaller number of transistors. Since it has lower speed, it is not used in high speed applications., this becomes a limitation.

3. Conventional Carry Skip Adder

The CSKA structure in conventional form having stages that includes full adder chains, block of RCA and 2:1 multiplexer, this multiplexer acts as a skip logic. Through this multiplexers, RCA blocks are connected each other, this is placed at one or more structure-level.
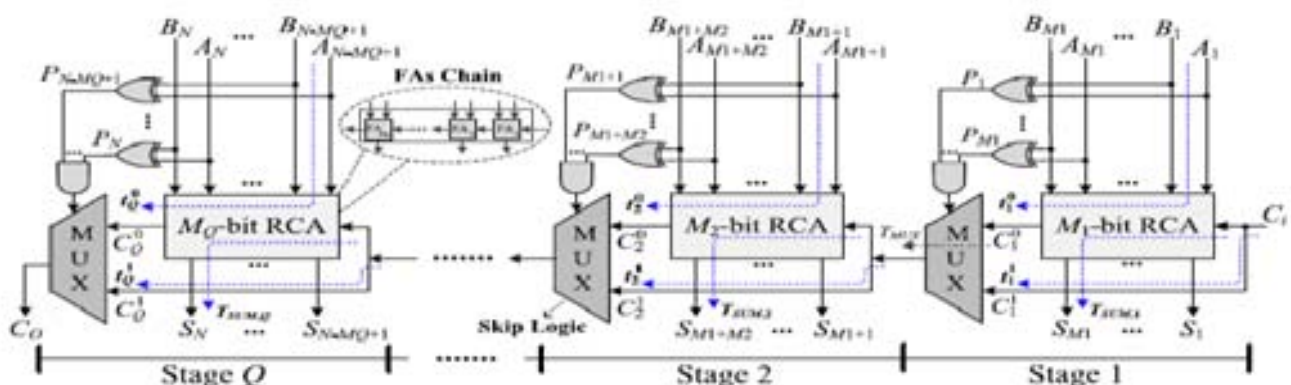

Figure 2: Structure of conventional CSKA

The input of the multiplexer are the carry input of the stage and the carry output of its RCA block and the product of propagation signals is used as the selector signals of the multiplexer. The carry skip adder may be implemented using FSS and VSS where the highest speed may be obtained for the VSS structure. There may be a great impact on speed in a CSKA configuration. Based on a single-level carry skip logic, techniques generated may use variable stage size in order to minimize the delay. In some methods to increase the speed of the circuit multilevel CSKA"s are proposed. The

area and power increased considerably in this technique and having less regular layout.

The A and B are the input bits, that are given normal to the ripple carry adder along with the full adder chain and initial carry that should be zero (i.e. $C_i = 0$) and as a producted form to the input of the multiplexer. In multiplexer the select lines are chosen according to the carry output of the ripple carry adder and the final output of sum and carry are obtained from ripple carry adder and multiplexer

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respectively. Generally, carry skip adder is a form of by-pass adder and it uses a ripple carry adder as an adder implementation. The multiplexer used in the circuit acts as a skip logic, that skip logic is a logic flow and it is a branching of condition, a custom path is created through the certain condition views that may varies based on a respondent answer.

In the conventional carry skip adder the skip logic with multiplexer reveals a large portion of critical path delay. The 2:1 multiplexer containing 12 transistors that leads to increase in area usage and power consumption. So these are to be considered as drawbacks of the existing design.

4. Proposed CSKA Design

The main objective of the proposed method is to enhance the speed and to improve the efficiency of the conventional carry skip adder. Have to reduce the power consumption of the design without impacting the speed of it and also have to reduce the area and critical path delay. In existing method due to the usage of multiplexer that acts as skip logic may leads to a large critical path delay and area usage and also a large power consumption. These drawbacks are going to be solved in the proposed design by using compound gates instead of multiplexer.

The AOI (**A**ND-**O**R-**I**nverter) and OAI (**O**R-**A**ND-**I**nverter) are called as compound gates, they acts as a skip logic in order to decrease the area usage and delay of the skip logics in conventional method.
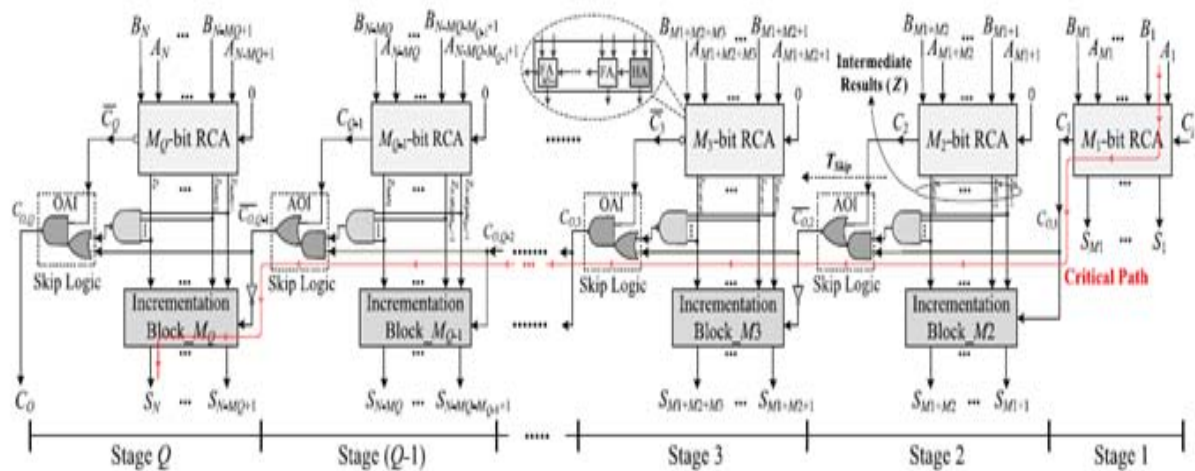

Figure 3: Structure of CI-CSKA

There is a reason behind the usage of both the AOI and OAI gates, these are generally called as compound gates as a skip logic is its inverting function of these gates in a standard cell libraries. Because of this usage of inverter gates the incrementation of power consumption and delay are eliminated.

5. Modified CSKA Design

The CI-CSKA structure may undergo further reduction of power consumption by including a technique called BrentKung. This BrentKung technique is one form of adder technique, it is a parallel prefix adder that may depends on the generate and propagate signals. The parallel prefix adder is mainly used because it offers low cost and wiring complexity.

In this a variable latency technique is involved, it is an adder technique. By using this variable latency feature in the structure offers an ability of power consumption reduction for this a ratio between the slack time and the delay of adder is used. This variable latency design was proposed to reduce the timing waste occurring in traditional circuits that use the critical path cycle. The basic idea is to execute a shorter path using a shorter cycle and longer path using two cycles. Since most paths execute in a cycle period that is much smaller than the critical path delay.

The use of the parallel prefix adder increases the available slack time in the variable latency structure, this parallel prefix adder is a fast adder.
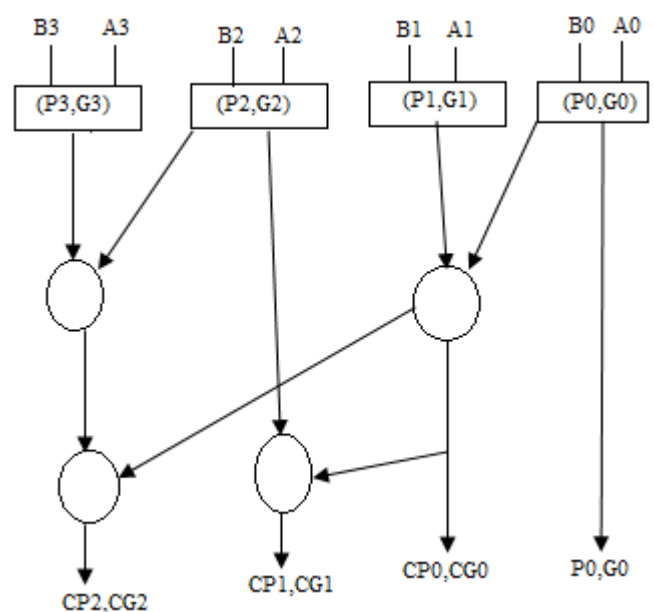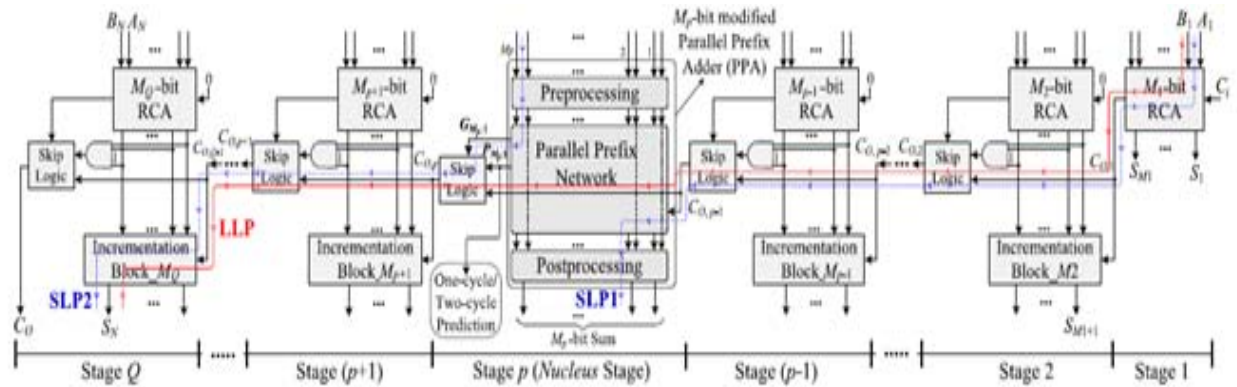

Figure 4: 4-bit BrentKung adder

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Figure 5: Structure of Modified CSKA

6. Results

Here, the coding is written in a VHDL language and simulated in ModelSim and the power is analyzed in Xilinx ISE 9.1e. Here the table shows the comparison of delay, no. of slices, no. of LUTs, no. of IOs and no. of bonded IOs, power of the CONV-CSKA, CI-CSKA and MODIFIED-CSKA.

Table 1: Analysis of CSKA in various forms

Parameters	CONV CSKA	CI CSKA	Modified CSKA
No. of Slices	28	27	27
No. of LUTs	52	48	46
No. of IOs	50	50	50
No. of Bonded IOs	50	50	50
Delay	31.988ns	22.456ns	22.456ns
Power	315mW	314mW	313mW

The waveform for all the form of CSKAs are shown in the following, there its input, output, and its characteristics are analyzed.
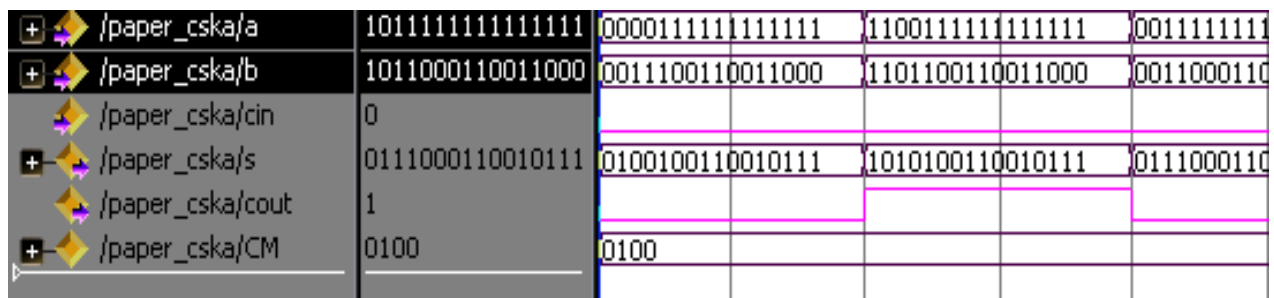

Figure 6: waveform of CONV-CSKA

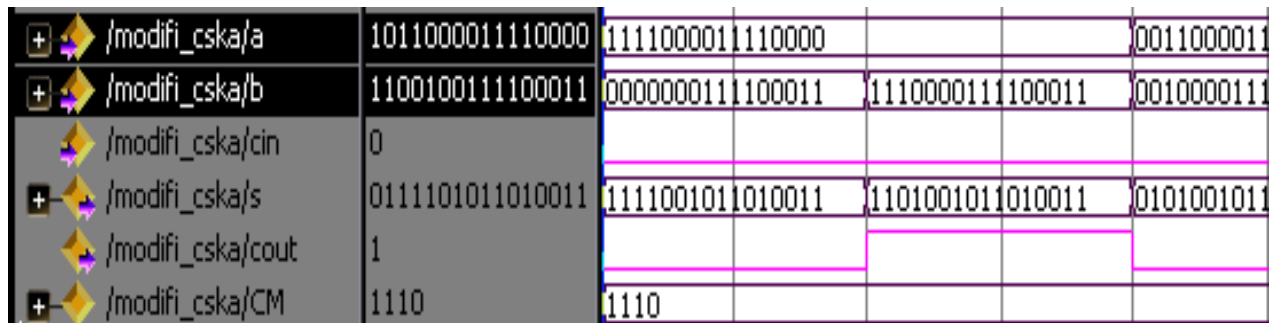**Figure 7:** Waveform of Proposed-CSKA

Figure 8: Waveform of Modified-CSKA

7. Conclusion

Thus an optimized, energy efficient and high speed carry skip adder was designed and its appropriate parameters like area, delay and power consumption were analyzed using Xilinx ISE 9.1e and they are compared for various form of the carry skip adder. The simulated form of the carry skip adder provides the result in the waveform manner, from which its characteristics can be understand.

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