International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2014): 5.611

Electrical Measurements for Semiconducting Devices

Vishakha N. Dhanwate[1], Yogesh P. Patil[2]

Department of Engineering Sciences, AISSMS's Institute of Information Technology Pune, MH, India

Abstract: ***In the last decade the research of semiconducting compounds reached to a particular level having as a goal the elaboration for the high efficiency solar cells of low cost. Functioning of a pn-junction is based on heat dependence of the current-voltage characteristics suggests boundary recombination as dominating transport mechanism. These junctions are appropriate for photovoltaic light conversion and for the growth of solar cells in superstrate configuration. In this Informative paper we have discussed basic of electrical measurements through which it is possible to deal with Current-Voltage Characteristics (I-V) and Capaciatnce-Viltage (C-V) Characteristics' for solar cell applications.***

Keywords: Semiconductors, Heterojunctions, Photovoltaic's, I-V, C-V characteristics

1. Introduction

The current-voltage (I-V) characteristics are based on relations between the electric current passing through a circuit and the corresponding potential (voltage) across it, where electrical current is a measure of the amount of electrical charge transferred per unit time. It represents the flow of electrons through a conductive material and Voltage is the electric potential energy per unit charge. If a unit of electrical charge were placed in a location, the voltage indicates the potential energy of it at that point. In other words, it is a measurement of the energy contained within an electric field, or an electric circuit, at a given point whereas resistance is the opposition to the flow of electric current by the component.

An I-V characteristic is the method of electrical measurements especially for semiconducting devices. There are two types of semiconductors,

Intrinsic semiconductor: It is an undoped or pure semiconductor without any significant doping.

Extrinsic semiconductor: It is a semiconductor in which doping is introduced, due to that it shows different electrical properties than the intrinsic (pure) semiconductor.

There are two types of extrinsic semiconductor, **p-type semiconductor:** p-type semiconductors have a larger hole concentration than electron concentration. The phrase 'p-type' refers to the positive charge of the hole. In p-type semiconductors, holes are the majority carriers and electrons are the minority carriers. P-type semiconductors are created by doping an intrinsic semiconductor with acceptor impurities.

n-type semiconductor: n-type semiconductor have a larger electron concentration than hole concentration. The phrase 'n-type' comes from the negative charge of the electron. In n-type semiconductors, electrons are the majority carriers and holes are the minority carriers. N-type semiconductors are created by doping an intrinsic semiconductor with donor impurities [1].

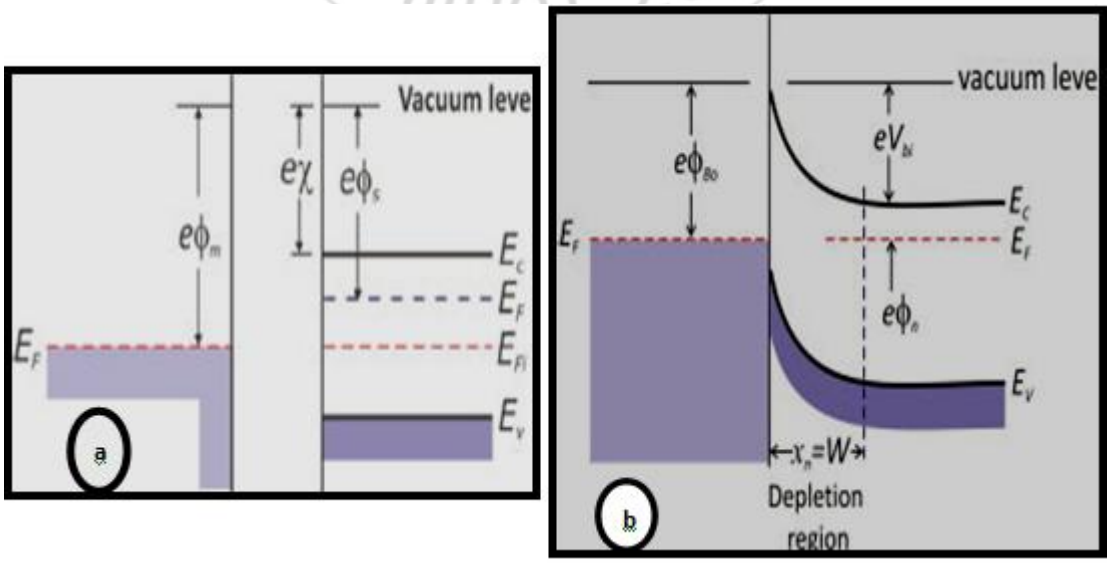

Figure 1: The energy band diagram for a metal and n-type semiconductor rectifying junction a) before contact b) after contact

A p–n junction is a interface between p-type and n-type of semiconductor material. A p–n junction is elementary "fundamental building blocks" of most semiconductor electronic devices such as diodes.

Metal–semiconductor (M–S) junction is a type of junction in which a metal comes in close contact with a semiconductor material. It is the oldest practical semiconductor device. M–S junctions can either be rectifying or non-rectifying. The rectifying metal–semiconductor junction forms a Schottky barrier, making a device known as a Schottky diode, while the non-rectifying junction is called an ohmic contact.

2. Schottky junction

When a metal and a semiconductor with therefore different Fermi energy levels are brought in contact with each other, the Fermi energy of each material will line up to a common level. In case on a n-type semiconductor the Fermi energy of the semiconductor is larger than the Fermi energy of the metal. Because there are many empty energy states in the metal, electrons with sufficient energy will flow into the metal taking the energy state. By leaving the semiconductor there will be unfilled energy states left in the semiconductor. Moreover, because a contact between the two different materials can never be ideal, the presence of chemical defects or broken bonds will cause large numbers of unfilled so called surface states.

These Free states will be filled by electrons from the semiconductor bulk. This provides a positive charge under the junction and a depletion region is formed. During this process the valence and conduction band is bent by the positive depletion charge preventing more electrons to take metal or surface states. Because the number of unfilled surface states is high, the metal side is assumed to be constant.

If a metal work function ϕ_m is larger than a semiconductor electron affinityχ, therefore contacting metal to the semiconductor leads to electron flow from the semiconductor to the metal as a prerequisite of Fermi levels alignment and thermal equilibrium. The remaining positively charged atoms in the semiconductor part create a space charge region. Thus electron flows from semiconductor to metal see a barrier of height ϕ_{BO} known as Schottky barrier.

3. Ohmic Contacts

An ohmic contact is a non-rectifying junction- a region in a semiconductor device that has been prepared so that the current-voltage (I-V) curve of the region is linear and symmetric. Usually it is a metal-semiconductor junction between a metal and semiconductor material. In semiconductor device fabrication (integrated circuit packaging), to make an ohmic contact, the contact region is doped, creating an extrinsic semiconductor to ensure the type of contact wanted (usually an n+ doped contact for an n-type silicon wafer and aluminum wires).

In this type of contacts, after thermal equilibrium, this occurs when electrons flows from the metal to the semiconductor lower energy levels. These electrons flow back into the metal part if a positive bias in the metal part was applied, and they will feel no barrier. Applying negative bias forces electrons to flow from metal to semiconductor seeing a very small barrier.

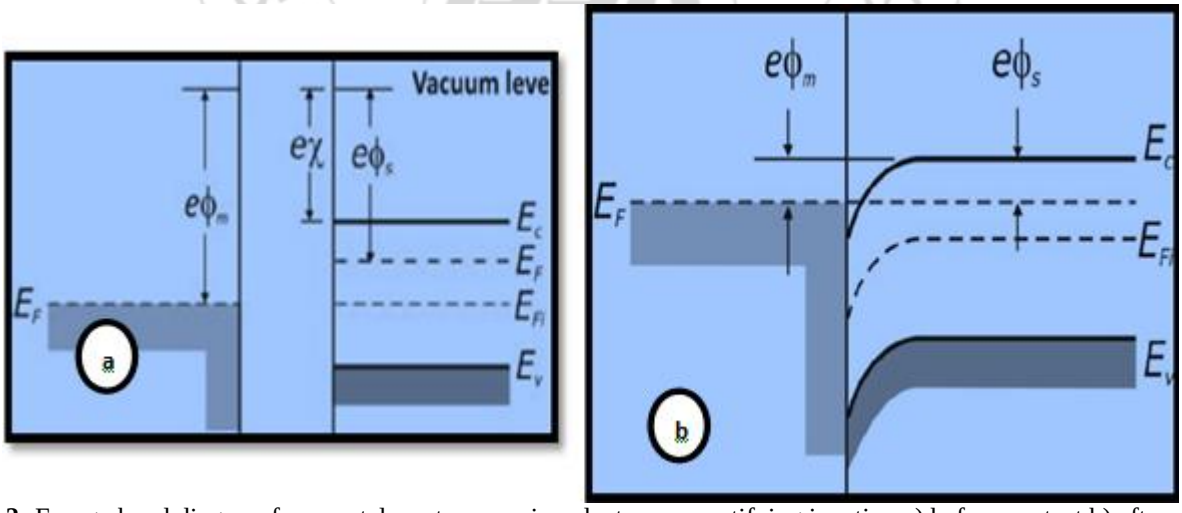

Figure 2: Energy band diagram for a metal –n- type semiconductor non rectifying junction a) before contact b) after contact.

The improvement in current indicates the decrease in grain boundaries and defects [3]. Defect enhances recombination process. More defects mean more space charge combinations. If there were no defects present, the total diode current would be diffusion current and n is equal to 1; this will be ideal diode case [2]. More defects drives n up to 2.

$$n = \frac{q}{nkT}\left(\frac{1}{slope}\right) \text{----------(1)}$$

n is ideality factor, q is Charge on electron, k is Boltzmann constant, Absolute temperature.

Schottky barrier diode characteristics can be expressed as,

$$I = I_0 e^{qv/nkT} \text{ ---------- (2)}$$

I_0 is reverse saturation current which is y-intercept of graph ln(I) verses V.
Barrier potential can be calculated by,

$$\phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{I_0}\right) \text{ ---------- (3)}$$

ϕ_B is barrier potential, A^* is Effective Richardson constant which is calculated by,

$$A^* = \frac{4\pi q k^2 m^*}{I_0} \text{ ---------- (4)}$$

h is Planck's constant , m^* is effective mass. m_0 is rest mass [2].

Capacitance-Voltage (C-V) measurement is widely used to determine semiconductor parameters, particularly in MOSCAP and MOSFET structures. However, other types of semiconductor and technologies also can be characterized with C-V measurements, including bipolar junction transistors, JFETs, III-V compound

Devices, photovoltaic cells, organic thin film transistor (TFT) displays, photodiodes, and carbon nanotubes.

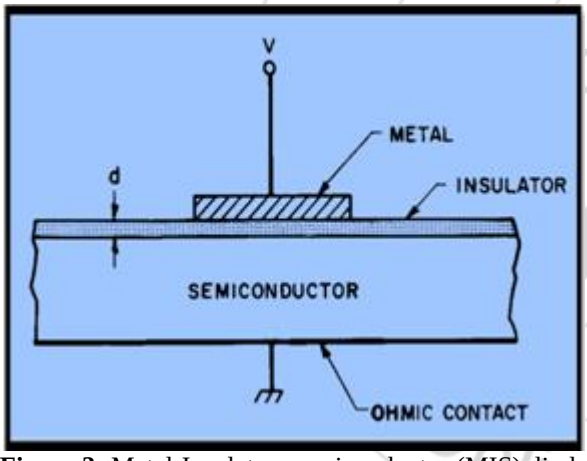

Figure 3: Metal-Insulator- semiconductor (MIS) diode

The metal-insulator semiconductor (MIS) diode is the most constructive in the study of semiconductor surfaces**.** This system has been broadly studied for the reason that it is in a straight line related to the most planner device and integrated circuits. The MIS structure in fig 3, where d is thickness of the insulator and V is the applied voltage on the metal field plate. We use the convention that the voltage V is positive when the metal plate is positively biased with respect to ohmic contact. When the MIS diode is biased with positive or negative voltages, essentially three cases may exist at the semiconductor surface [4].

Firstly the "accumulation" region, when the small negative voltage is applied, the band bends upward, and the majority carriers are depleted in second region called "depletion". When a positive voltage (v>0) is applied to metal plate, the top of the valance band bends downward and closer to Fermi level. For an ideal MIS diode, no current flows in the device. So, the Fermi level remains stable in the semiconductors. Since the carrier density depends exponentially on the energy difference (E_f - $E_{v)}$, this band bending causes an accumulation of majority carriers (electrons) close to the semiconductor surface. When the superior negative voltage is applied, the band bend even more upward so that the intrinsic level E_i at the surface crosses over the Fermi level E_f. At this point the number of holes, the surface is thus inverted, and this is the"inversion" case.

The capacitance-voltage measurement is usually carried out in order to estimate doping concentration of the semiconductor and the flat band voltage of the Schottky diode. The C-V characteristics of all the films involved distinct inversion, depletion, and accumulation regions, during the CV measurement the device is swept from accumulation to inversion. Semiconductor doping concentration can be calculated by the formula [5].

$$N_A = \frac{2}{q \in A^2 \left(\frac{d(1/c^2)}{dV}\right)} \text{ ---------- (5)}$$

N_A is doping concentration of semiconducting material, q is charge on electron, ε is permittivity of the material and $\frac{d(1/c^2)}{dV}$ slope is obtained from graph $1/C^2$ verses V. Flat band potential is used as characteristics potential of individual semiconductor electrodes in the same way as the potential of zero charge is used for metal electrodes. Flat band potential is determined by extrapolation to C = 0 [4].

4. Conclusion

To improve the efficiency of solar cell, we have to enhance the electrical properties of the material. For that electrical properties of heterojunctions involving wide gap n-type and the p-type semiconductor materials. With the above given formulas it is possible to find ideality factor and barrier potential by using I-V characteristics. Same way flat band potential and carrier concentration can be obtained with C-V measurements. These are said to be primary testing for efficiency of device.

References

[1] Mehta V.K, Mehta Shalu, Introduction to solid state Physics, Seventh edition, John Wiley & Sons Inc, India (2009).
[2] Sze S. m, Semiconductor devices, revised edition, John Wiley & Sons inc, UK (2009).
[3] Dhanwate V.N and Chaure N.B, Effect of growth potential on the electrodeposition of CIS thin films, Applied Nanoscience, 3 (2013) 1-5.
[4] Streetman B.G, Sanjay Kumar Banerjee, Sixth edition, Solid state electronic devices, Pearson prentice Hall, USA (2006).
[5] Sze S.M. Physics of semiconductor devices, Second edition, John Wiley & Sons Inc, UK (1981).