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Implementation of VLSI Based Robust Router Architecture

M. N. Karanjkar[1], Pramod Kulkarni[2]

[1]Professor, Department of Electronics and Telecommunication, Shree Tuljabhavani College of Engineering, Tuljapur, Osmanabad , India

[2]Department of Electronics and Telecommunication, Shree Tuljabhavani College of Engineering, Tuljapur, Osmanabad , India

Abstract: ***In this paper, we introduce networking solution by using VLSI architecture techniques to router design for networking system to provide control over the network. We attempts to overcome latency and time reduction issue and can provide multipurpose networking router by means of verilog and it was synthesized in Xilinx 13.2 version, simulated Modelsim 10.0 version. The approach enables the router to process mul-tiple incoming IP packets with different versions of protocols simultaneously, e.g. for IPv4 and IPv6.***

Keywords: Xilinx 13.2 version, simulated Modelsim 10.0 version

1. Introduction

The challenge of the verifying a large design is growing exponentially. There is a need to define new methods that makes functional verification easy. Several strategies in the recent years have been proposed to achieve good functional verification with less effort. Recent advancement towards this goal is methodologies. The methodology defines a skeleton over which one can add flesh and skin to their requirements to achieve functional verification. This project is aimed at building a reusable test bench for verifying Router Protocol Verilog.

In this document the use Verilog to verify a design and to develop a reusable Test bench is explained in step by step as defined by verification principles and methodology. The Test Bench contains different components and each component is again composed of subcomponents, these components and subcomponents can be reused for the future projects as long as the interface is same. The Report is organized as two major portions; first part is brief introduction and history of the functional verification which tells about different technologies, strategies and methodologies used today for verification. Liter-ature survey will contain an organized collection of data from different sources and significant changes that took place in the verification and design.. Second part is verification plan specifying the verification requirements and approaches to attack the problem, architecture of the test bench gives com-plete description about the components and sub components used to achieve the verification goals and also explains about improvements made in the design of the Router, test plan identifies all the test case required to meet the goals and finally results of the project.

Four Port Network Router has a one input port from which the packet enters. It has four output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 byte to 63 bytes. Packet header contains three fields DA and length. Destination address (DA) of the packet is of 8 bits. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data.

A data packet is typically passed from router to router through the networks of the Internet until it gets to its destination computer. Routers also perform other tasks such as translating the data transmission protocol of the packet to the appropriate protocol of the next network.

2. Literature Survey

In this we are comparing the existing generic router architecture and our new robust router architecture. This will give the difference in the designing and would reflect our paper enhancements that we are upgrading in our robust router paper.

A. Generic Router Architecture

Channamallikarjuna Mattihalli et al in [1] give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Attempt to provide a multipurpose network-ing router by means of Verilog code, thus we can maintain the same switching speed with more security as we embed the packet storage buffer on chip and generate the code as a selfindependent VLSI Based router. The approach will results in increased switching speed of routing per packet for both current trend protocols, which we believe would result in considerable enhancement in networking systems.

Feng Liang et al in [2] proposed a novel test pattern generator (TPG) for built-in self-test. His method generates multiple single input change (MSIC) vectors in a pattern, i.e., each vector applied to a scan chain is an SIC vector. A reconfigurable Johnson counter and a scalable SIC counter are developed to generate a class of minimum transition sequences. The proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes. Results show that the produced MSIC sequences have the favorable features of

uniform distribution James Aweya et al in [3] give attention to new powerful architectures for routers in order to play that demanding role. In this work, he identified important trends in router design and outlines some design issues facing the next generation of routers. It is also observed that the achievement of high throughput IP routers is possible if the critical tasks are identified and special purpose modules are properly tailored to perform them.

M. Sowmya et al in [4]he attempt is to give a onetime networking solution by the means of merging the VLSI field with the networking field as now a days the router is the key player in networking domain so the focus remains on that itself to get a good control over the network. This paper is based on the hardware coding which will give a great impact on the latency issue as the hardware itself will be designed according to the need.

B. Four Port Router architecture

Router is a packet based protocol. Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet .The router has a one input port from which the packet enters. It has three output ports where the packet is driven out. The router has an active low synchronous input resetn which resets the router.

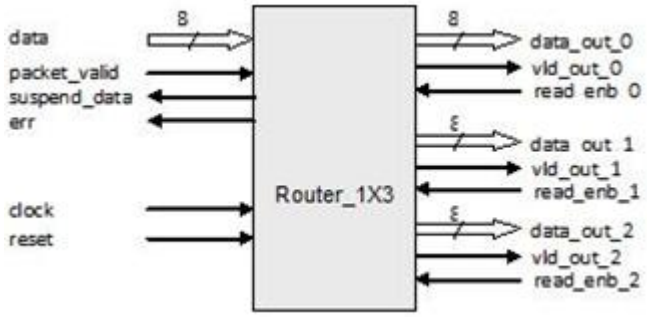

Figure 1: Block diagram of proposed system

Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily. The buffering method used here is store and forward. Control logic is present to make arbitration decisions. Thus communication is established between input and output ports.. According to the destination path of data packet, control bit lines of FSM are set. The movement of data from source to destination is called switching mechanism The packet switching mechanism is used here, in which the flit size is 8 bits.

The paper design has the following modules.

C. Input Interface Block

This block is mainly responsible for receiving the incoming IP packets over multiple input channels. This block asserts the necessary response signals in order to communicate with t**he**

3. Simulation and Discussion

The Net List is RTL level of the robust router system, which

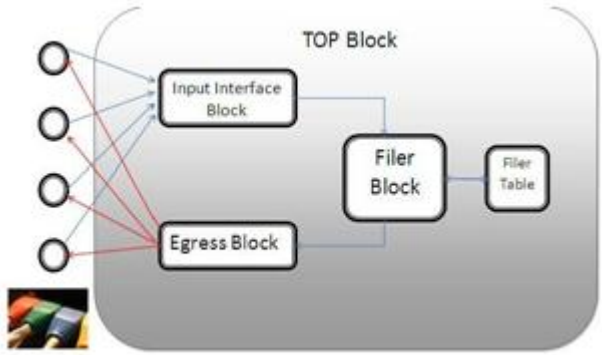

Figure 2: Interface diagram

IP packet driver modules. After receiving the IP packets, this block forward the same to the Ingress Block for the further process. This block forwards the same to packet store block as well as parser block.

D. Packet Store Block

This is responsible for storing the error free received packets. This module receives the packet contents from Ingress block and dispatches the same based on the request from Egress block.

E. Parser Block

This block is mainly responsible for parsing the complete packet into multiple set of data according to its field. The parsed contents will be inputted to the filer block. The above three blocks are merged all together as IIB in code to single file.

F. Filer Block

This block is responsible for selecting the egress ring. The block receives the parsed data from the parser block. The parsed data will be forwarded to the filer table. In response to this, the filer table provides the output ring number. Then, the received output from the filer table will be forwarded to the egress block.

G. Egress Block

This block receives the data from filer block as egress ring number through which the received packet shall be forwarded. Upon receiving the egress ring number, this block initiates the communication with packet store block to fetch the packet to be forwarded. Then, the fetched IP packet will be forwarded to the output interface block with the output channel details, over which the packet has to be transmitted.

H. Output Interface Block

Upon receiving the packet with output port details from the egress block, this block forwards the IP packet over mentioned output channel. This block is also responsible for asserting all the necessary handshaking signals for the receiving device while transmitting the packets. The Egress Block and Output Interface Block are merged together in code as single file.

is syntasizable and can be extracted on the Xilinx tool. By which we can get preface look of the system and a transition from the frontend of the VLSI designing to backend of the VLSI designing. Which means the same can run on FPGA kit

and test its robustness and errors of the system can be debugged before it is taken to SOC Level and to Fab-Labs.

The snap below is the Pin configuration of the proposed Robust Router

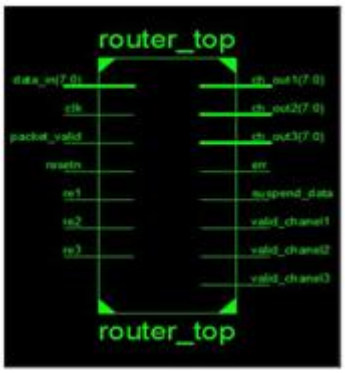

Figure 3: Net List

The snap below is the Pin configuration of the proposed Robust Router TECHNOLOGY SCHEMATIC

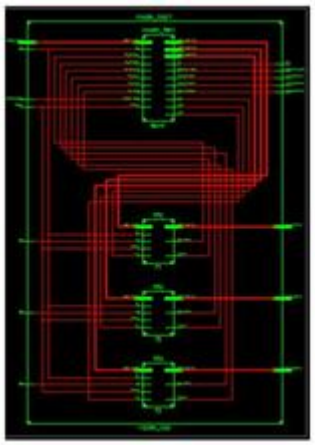

Figure 4: Technology Schematic

The snap below is Timining Diagram of the proposed Robust Router

4. Conclusion

In this paper the code given in the output is put in the router at the same time. The proposed Robust Router will route packets at the same time at the same speed with improved run time in comparison to conventional design. The Robustness is reviewed with Model-Sim Tool with different Test Cases and the same codes Net List is extracted with Xilinx Tool for the synthesizable code. The same can be taken to the SOC (System on chip) level with Cadences Encounter Tool.

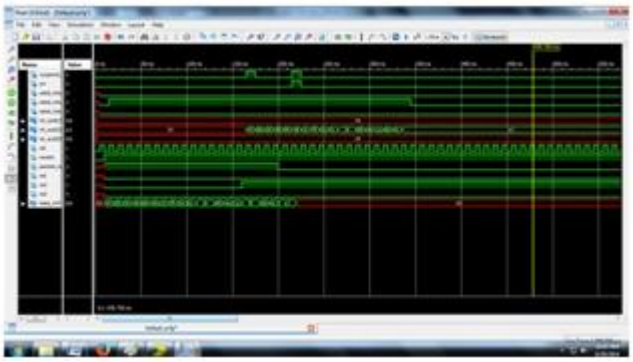

Figure 5: Timining Diagram

This paper used System verilog i.e., the technology used is direct test cases, randomized test case, ovm for verification even though the coverage is 100shown so in order to overcome this the new technology of System verilog i.e. OVM and UVM. In the coming future the Router can be done by using OVM and UVM.

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