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Design and Implementation of 16 X 16 High speed Vedic multiplier using Brent Kung adder

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Abstract: ***In VLSI design, the performance of any system is determined by the performance of the elements i.e. Multiplier. Multiplier is the slow element in the system. The speed of multiplier depends on multiplication technique and type of adder. This paper proposes the architecture of 16 x 16 high speed binary arithmetic multiplier using 'Urdhva Tiryagbhyam' sutra of Vedic mathematics. Urdhva Tiryagbhyam sutra is used for generating the partial products. The partial product addition in Vedic multiplier is realized using Brent Kung adder. The HDL used for design is Verilog and code is implemented in Xilinx ISE 14.7 software. The combinational path delay of 16x16 bit Vedic multiplier obtained after synthesis is compared with Vedic multiplier using MUX based adder and found that the proposed Vedic multiplier circuit seems to have better performance in terms of speed.***

Keywords: Vedic Multiplier, Delay, VLSI, Brent Kung adder, Urdhva Tiryagbhyam Sutra, Verilog HDL

1. Introduction

In modern VLSI design period, delay in data path considered as a critical parameter these days. Designers are demanding to minimize the delay as the speed up operation becomes faster. There has been lot of researches and work regarding reducing of delay and now designer look for making a multiplier circuit which is efficient and considerably faster [1][6]. A fast speed processor performance depends greatly on the multiplier as it is one of the essential hardware component in most digital signal processing systems as well as in all-purpose processors [6][9].It also consumes more area. Vedic multiplier gives the better speed than the conventional multiplier and decreases the system memory. Very small area is required for this multiplier as compared to other multiplier design.

In paper [3], 8- bit Vedic multiplier using Brent Kung adder has been designed. Brent Kung adder is the parallel prefix form of carry look ahead adder. The results shows that the proposed 8- bit Vedic multiplier is faster than 8- bit Vedic multiplier with MUX based adder. The reduction in the delay is approximately 30.6%. The main purpose of this work is to design and implement a high speed 16 X 16 bit Vedic multiplier by combining the best technique in Vedic mathematics named Urdhva Tiryagbhyam and Brent Kung adder.

2. Vedic mathematics

It is an ancient technique, which simplifies multiplication, divisibility, complex numbers, squaring, cubing, square roots and cube roots. In Vedic mathematics, two of sixteen sutras are mostly used for performing multiplication method [5]. One sutra is Urdhva-Tiryagbhyam and other is Nikhilam Navatashcaramam Dashatah. Urdhva-Tiryagbhyam is relevant to all cases of multiplication [3]. The use of Vedic mathematics reduces the complex calculations in conventional mathematics to very easy one. This is so because the Vedic sutras are declared to be based on the natural principles on which the human mind works. Vedic Mathematics is a scheme of arithmetic rules that permit more efficient speed achievement.

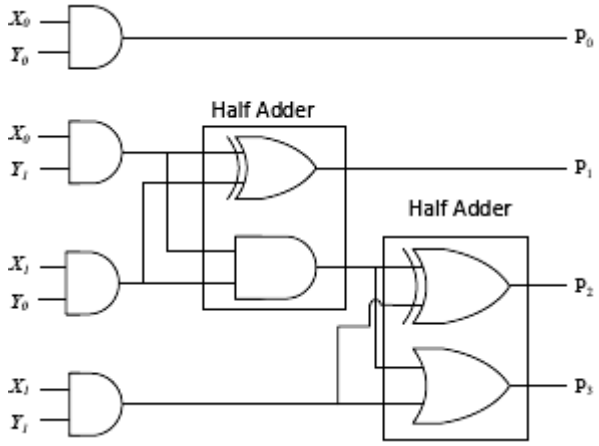

Figure 1: 2X2 Vedic Multiplier

2.1. Urdhva Tiryagbhyam

Urdhva Tiryagbhyam is the general formula applicable to all cases of multiplication [9]. It is also referred as "Vertically and crosswise algorithm" [5]. This Sutra has been conventionally used for the multiplication of two numbers in the decimal number system. But in this work the same idea has been applied for binary multiplication. This can solve the multiplication of larger number (N X N bits) by breaking it into smaller sizes. The first step in multiplication is vertical multiplication of LSB of both multiplicands, and then second step is crosswise multiplication and additions of the partial products. Third step involves vertical multiplication of MSB of the multiplicand and addition with the carry propagated from step 2.

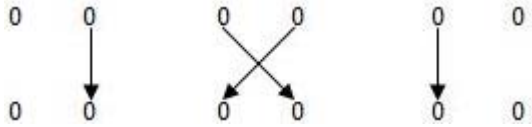

Figure 2: Line Diagram for 2 X 2 Bit binary multiplication using Urdhva Tiryagbhyam Sutra

Step a: 0X0 = 0
Step b: 0X0 + 0X0 = 0
Step c: 0X0 = 0

a) Algorithm for 16 X 16 Bit binary numbers Multiplication Using Urdhva Tiryagbhyam:

A=A15A14A13A12A11A10A9A8 A7A6A5A4A3A2A1A0
X1 X0
B=B15B14B13B12B11B10B9B8 B7B6B5B4B3B2B1B0
Y1 Y0

X1 X0
* Y1 Y0

F E D C

CP = X0 * Y0 = C
CP = X1 * Y0 + X0 * Y1 = D
CP = X1 * Y1 = E
Where CP=Cross product

3. Brent Kung adder

The schematic of the Brent Kung Adder is shown in figure 3. It is a type parallel prefix adder. Parallel prefix adders have the best performance in VLSI Design Parallel prefix adder is the most flexible and widely used for binary addition.

In carry look ahead adder, as the size of the input operands is increased the combinational delay is also increased. So the idea here is to have a gate level depth of O(log 2(n)). Brent Kung adder takes less area to implement than the other prefix adders such as Kogge-Stone adder and it also has less wiring congestion. This adder will reduce the delay without compromising the power performance of the adder. The Brent Kung adder comprises of three stages like Pre-processing Stage, Carry generation Stage and Post-Processing Stage [3] [11].

a) Pre-processing Stage

$P_i=A_i$ XOR B_i (1)

$G_i=A_i . B_i$ (2)

b) Carry generation Stage

$Cp=Pi.Pj$ (3)

$Cg=Gi+Gj.Pi$ (4)

c) Post-Processing Stage

$S_i=P_i$ XOR C_{i-1} (5)

$C_{i-1}= (P_i . C_{in}) + G_i$ (6)

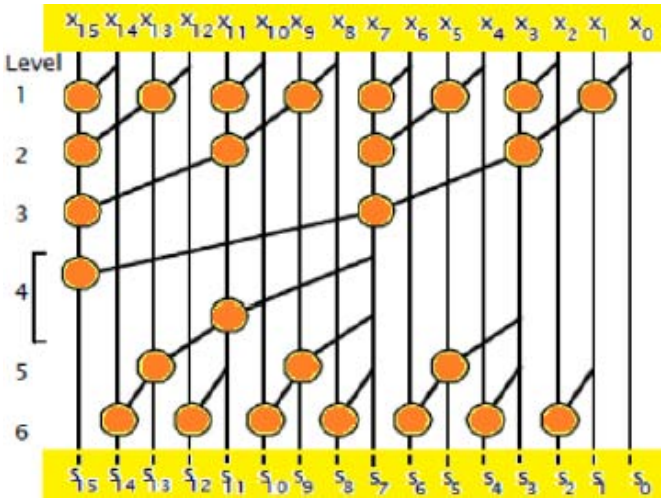

Figure 3: Schematic of 16-bit Brent Kung adder

4. Design of 16 X 16 Vedic Multiplier using Brent Kung adder

The approach applied for developing a 16 X 16-bit Vedic multiplier is to design a 2 X 2-bit Vedic multiplier as a basic building section for the system. Two Half adders are required in designing 2 X 2 Vedic Multiplier.The development of a 4 X 4-bit multiplier is designed using 2 X 2-bit Vedic multiplier . By using 4 x 4 bit Vedic multiplier as a building block, 8 x 8 bit Vedic multiplier is designed .Then the design of 16 X 16 bit multiplier using four 8 X 8 bit multiplier blocks and three 16-bit Brent Kung adder blocks is shown in fig 4

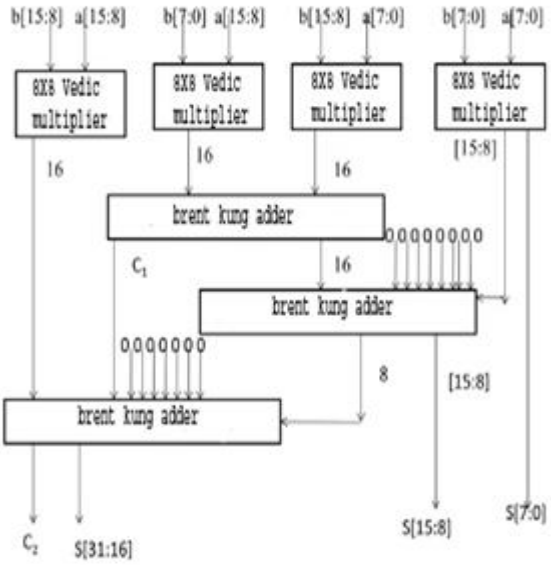

Figure 4: Block diagram of 16X16 Vedic multiplier using 8 bit Brent Kung adder

5. Result

5.1. Synthesis

The Verilog code of proposed multipliers and Vedic multiplier using MUX based adder are synthesized using XILINX ISE 14.7. The RTL diagrams of both multipliers are shown in figure 5 & 6.

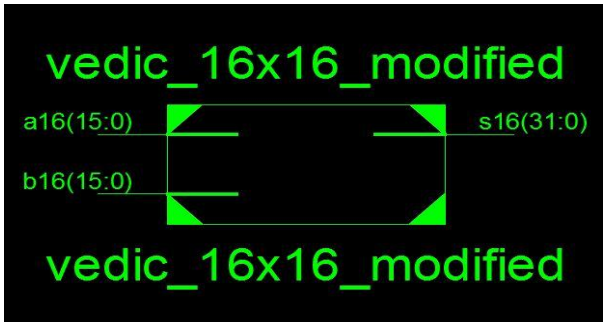

Figure 5: RTL view of 16x16 Vedic multiplier using Brent Kung adder

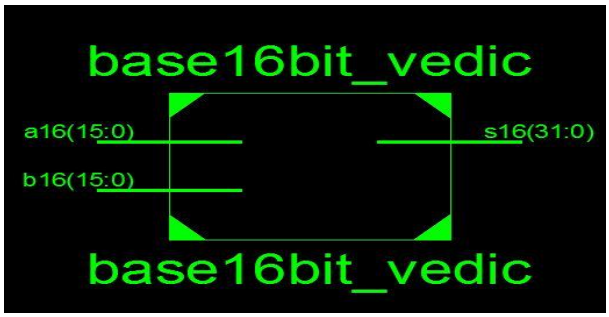

Figure 6: RTL view of 16x16 Vedic multiplier using MUX based adder

5.2. Simulation

From the simulated waveforms the functionality is verified and confirms the operation of the design. With a little bit of trade off in terms of area the combinational delay is reduced drastically. ISim simulator is used for simulation purpose. The Simulation result for 16 bit is shown in Fig 7 & 8 in which a and b are inputs and c is their product.

a) Simulation of 16 X 16 bit Vedic Multiplier using Brent Kung adder

The Simulation result for 16 X 16-bit Vedic multiplier using MUX based adder is shown in figure 8 in which a=1111111111111111 and b=1111111111111111 is taken and result c=11111111111111100000000000000001 is obtained.

Figure 7: Simulation Result of 16X 16 bit Vedic multiplier using Brent Kung adder

b) Simulation of 16 X 16-bit Vedic Multiplier using MUX based adder

The simulation result of proposed 16 X 16-bit Vedic multiplier for same set of inputs as used in Fig 7 is shown in Fig 8.

Figure 8: Simulation Result of 16 X 16 Vedic multiplier using MUX based adder

Table 1

Type	No. of Bits	No.of bonded IOs	Delay (ns)
Vedic multiplier using Brent Kung adder	16	64	10.548
Vedic multiplier using MUX based adder	16	64	16.144

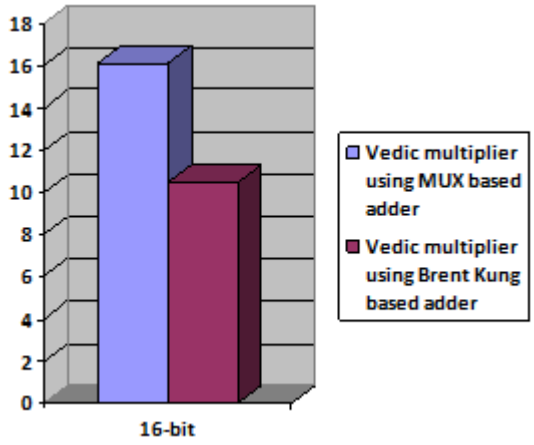

Figure 9: Delay (ns) comparison between two Vedic multipliers

6. Conclusion and Future Work

This paper presents a novel high speed design for multiplication by combine the features of Vedic mathematics & Brent kung adder. From the table 1 we conclude that the proposed Vedic multiplier is 34.7% faster from the Vedic Multiplier using MUX based adder.

Our proposed Vedic multiplier shows drastically faster performance than the Vedic multiplier using MUX based

adder. This architecture and fast performance makes this multiplier particularly attractive for VLSI implementations. This 16 bit multiplier can be further extended to 32 bit multiplier and 64 bit multiplier using the proposed method for multiplication operation can be done as future work

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