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FPGA Implementation for Contrast Enhancement in Images Using Xilinx System Generator

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Abstract: ***This paper presents novel image contrast enhancement models using Xilinx System Generator (XSG). The proposed models are specifically to enhance the images captured under extremely dark / non-uniform lighting environment as well as for poor contrast environment. To perform the contrast enhancement the proposed design adapts windowing operation by utilizing linear intensity scaling and clipping. By which the proposed models maps a partial range of the grayscale window to the full dynamic range. Thus it brings up the image contrast in a certain grayscale window at the expense of saturating pixels which fall outside the window. For illumination correction, the whole input image is enhanced by the proposed window model 1. And for low contrast enhancement, the input image is split into four non overlapping windows and each window is enhanced by the proposed window model 2. Finally all the windows are mapped to get the output image. These dual models are designed and implemented in Spartan3E (XC3S500E-FG320) and Spartan6-LX9 (XC6SLX9-2CSG324) micro board and their results are compared. The experimental results show that the proposed XSG based designs adapt minimum resources as well as it preserves the quality of the image.***

Keywords: Contrast enhancement, Simulink, Xilinx System Generator, FPGA

1. Introduction

Image processing algorithms implemented in hardware is the most suitable solution for improving the performance of the image processing systems. Many image processing algorithms are based on local image features. It requires simultaneous access to many neighbouring input image pixels to calculate the result for a single pixel of the output image. The system level hardware programming languages and reconfigurable devices has speed up the design of image processing in hardware. Almost many of the system level hardware programming languages are highly hardware specific. And it requires intermediate to advance hardware knowledge for design and implementation of the system.

Besides, the complexity of many algorithms increases the requirements for computational power. Modern digital signal processers offer enough speed and architectural features for image processing. But at the cost of high clock rates, power consumption and unit price of the devices. Hence there is a need of technology which is free from above drawbacks for the hardware implementation of image processing algorithms. Although many powerful design tools are available to make the development process fast and effective. One such solution is the Field Programmable Gate Array (FPGA) technology which is a cheap and easy way to build dedicated processors for many widely used image transformations. FPGA based implementation is fully programmable and is more flexible [1]. FPGA supports XSG, is a tool with a high-level of graphical interface. XSG uses the MATLAB and Simulink based blocks which makes it very easy to handle with respect to other software for hardware description.

FPGA technology is widely used in many modern imaging applications such as image filtering, medical imaging, image compression and wireless communication [2]. In paper [3], a reconfigurable architecture for performing adaptive histogram equalization and contrast limited adaptive histogram equalization (CLAHE) was presented. In which the images are accessed from off-chip memories and enable processing of high definition images.

The histogram mapping is carried out with respect to the stored image pixels. A complicated model for the contrast enhancement of the images was reported in [4]. The author implemented the model in FPGA using XSG. In paper [5], adaptive histogram equalization with less computation time was suggested. Also this work optimizes the algorithm for computation in hardware architecture. A parallel architecture for CLAHE was proposed in [6] for images affected by poor lighting. The author implemented the architecture using vertex FPGA device and also make use the Graphical User Interface (GUI) features of XSG. Hardware architecture for microscopic images of bacteria and alga was reported in [7]. The implementation was carried out by using XSG as the development platform.

The rest of the paper is organized as follows. Sections 2 discuss the significance of contrast enhancement. Section 3 presents the proposed method. Section 4 shows the hardware co-simulation results and finally section 5 concludes the paper.

2. Significance of Contrast Enhancement

Illumination is one of the most important factors which affect the visual quality of an image. Uneven illumination produces diminished structures or inhomogeneous intensities of the image. This is due to different texture of the object surface and also the formation of the shadows from different light source directions. Sometimes this may cause due to the uneven background. It is known as background bias, non-uniform background or background intensity in-homogeneity. Consider that an ideal image I is corrupted by an uneven background signal B so that the observed image O = I + B. In this recovering I from O is not an easy task when B is non-uniform. Hence it is clear that

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both the varying illumination and the uneven background are inhomogeneous intensity patterns which are either multiplicative or additive [4].

Another important task is identifying the edges of the low contrast structures for interpreting medical images [8]. Elimination of low contrast structures are essential for all kinds of digital medical images such as magnetic resonance (MR), computed tomography (CT), digital mammography, angiography, ultrasound and nuclear medicine. Acquiring high contrast in the raw image directly from the imaging device is always expensive in medical examination time or X-ray dose to patient. The low contrast CT images are only increased by raising the number of photons absorbed in each voxel which is proportional to the X-ray dose. So most important structure of medical images has low contrast with the surrounding structures. Generally the production of these images involves a tradeoff between the need for enhancement and the cost of obtaining it. For these situations, the contrast enhancement is essential [9].

However in image processing the contrast enhancement is a problem similar for all images obtained from different medical imaging modalities. Always low contrast is considered as a bad distribution of pixel intensities over the dynamic range of the display device. This will be enhanced by modifying the intensity distribution of the image. Also contrast enhancement techniques are widely used in most outdoor vision applications such as terrain classification, surveillance and autonomous navigation. Images taken under bad weather conditions will severely degrade its contrast. Hence it is essential to remove weather effects from images in order to make vision systems more reliable [10]. When the above problems are related, some are more dependent on the quality of the capture devices used whereas others are related to the conditions in which the image was captured. Thus the contrast enhancement of images is essential for many applications. The proposed model adapts a non model based enhancement method. The block diagram of the proposed design is shown in Figure 1.

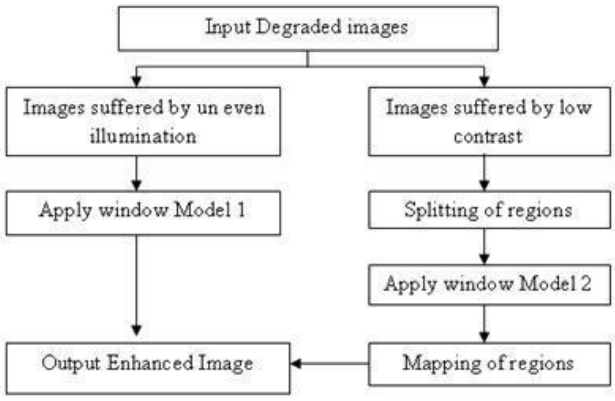

Figure 1: Block diagram of the proposed design

3. Proposed System Generator Based Design

The proposed system generator based design consists of three phase operation using xilinx blocks as:

- Image pre-processing blocks
- Contrast enhancement using XSG
- Image post processing blocks

To perform the contrast enhancement in hardware, the image must be pre-processed prior to main architecture. In software level simulation there is no need for image pre processing phase. It will access an image as a two dimensional (2D) matrix of pixels with size M x N. But in hardware implementation, this matrix must be considered as an array of one dimensional (1D) vector, where it requires image pre-processing.

3.1 Image pre-processing blocksets

The system generator based design used for image pre-processing is shown in Figure 2. Input images are provided as input to the file block which could be color or gray scale. A color space conversion block converts RGB (Red,Green,Blue) color model to gray scale image. Then the data which are in 2D are to be converted to 1D for further processing. Frame conversion block sets output signal to frame based data. It provides input to unbuffer block which converts this frame to scalar samples output.

3.2 Contrast enhancement using XSG blocksets

The proposed system generator based design for contrast enhancement of the input image is processed using xilinx system generator [11]. In the proposed design, two different xilinx blocksets are designed for non uniform illumination and low contrast image correction.

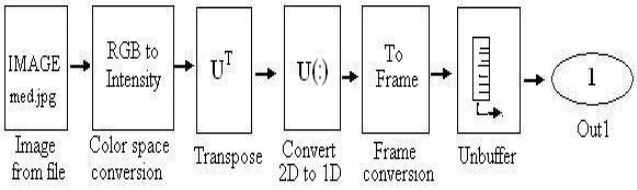

Figure 2: Xilinx block sets for image pre-processing operation

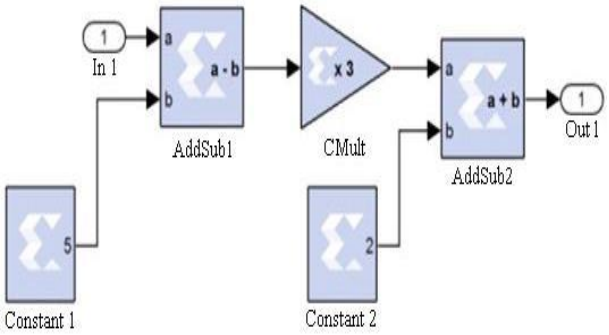

Figure 3: Proposed window model 1 for non uniform illumination correction

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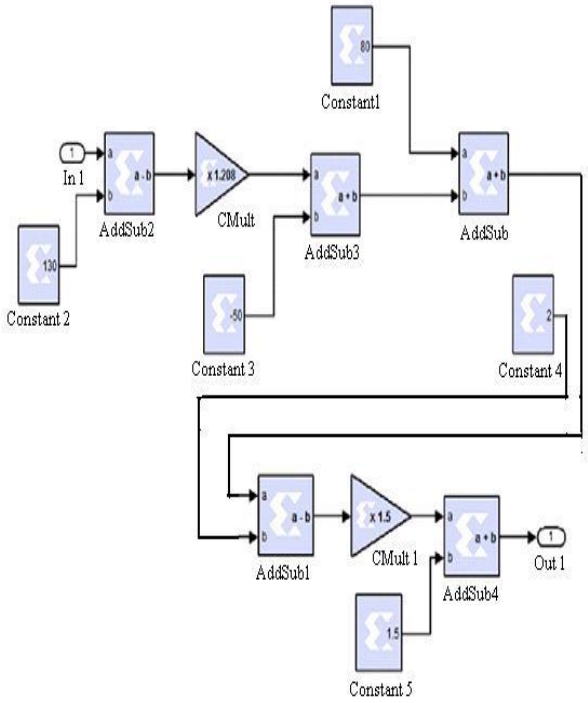

Figure 4: Proposed window model 2 for low contrast correction

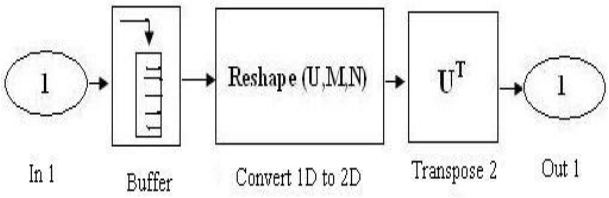

Figure 5: Xilinx block sets for image post-processing operation

For illumination correction, the proposed window model 1 is used to enhance the input image. The model 1 is shown in Figure 3. To enhance the low contrast images, the input image is split into four non overlapping windows. And each window is enhanced by the proposed window model 2 shown in Figure 4. Finally all the windows are mapped to get the output image. Xilinx fixed point data type conversion is made possible by the input block namely gateway in. To perform the contrast enhancement the proposed work adapts a non model based design by utilizing clipping and linear intensity scaling. Commonly it is called as windowing the image because it maps a partial range of the grayscale to the full dynamic range of it. By windowing operation, the contrast is improved in certain grayscale window at the expense of saturating pixels which fall outside the window. Usually the gray level is varying across the image. So choosing the right window at each part of the image needs prior knowledge or intensive human interaction. Windowing itself can be regarded as a method of contrast enhancenment. This is followed by certain arithmetic blocks to merge all the processed data and a data converter block namely gateway out.

3.3 Image post-processing blocksets

The image post processing blocks are used to convert the image output back to display format is shown in Figure 5. Buffer block used in post-processing converts scalar samples to frame output followed by 1D to 2D format signal block. Finally a sink is used to display the output image back in the display unit. The complete architecture with the hardware and software co-simulation is shown in Figure 6.

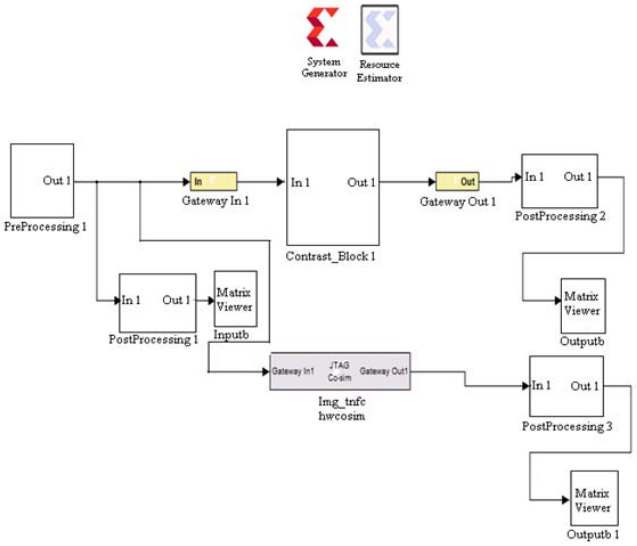

Figure 6: Complete design for hardware /software co-simulation

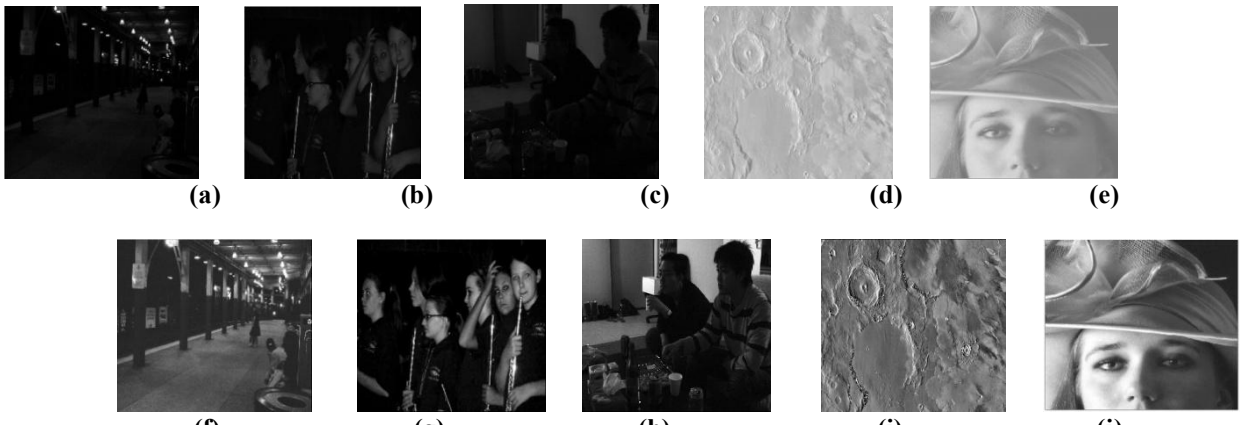

Figure 7: (a), (b), (c), (d) & (e) shows images degraded by un-even illumination and its hardware co-simulation results for illumination correction are shown in (f), (g), (h), (i) & (j) respectively

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Table 1: Resource utilization of non uniform illumination correction algorithm

Resource	SPARTAN-3E			SPARTAN-6 LX9		
	Used	Available	Utilization	Used	Available	Utilization
Slices	9	4656	1%	11	1430	1 %
LUTs	25	9312	1%	34	5720	1 %
IOBs	20	232	8%	26	200	13 %

Table 2: Resource utilization of low contrast correction algorithm

Resource	SPARTAN-3E			SPARTAN-6 LX9		
	Used	Available	Utilization	Used	Available	Utilization
Slices	136	4656	2%	130	1430	9%
LUTs (4 Inputs)	142	9312	1.50%	290	5720	5%
IOBs	45	232	19%	52	200	26%

Table 3: Comparison of resource utilization (Spartan 3) of non uniform illumination correction algorithm

Resource	Available	Used	Utilization	
			Acharya et al (2011)	Proposed design
Slices	4656	9	21 %	1%
LUTs	9312	25	9 %	1%
IOBs	232	20	36 %	8%

4. Hardware Co-Simulation Results

The above section discusses the architecture for software simulation. To implement this design in FPGA board, the entire module should be converted to FPGA synthesizable format. For that purpose, the main module of the contrast enhancement blockset is converted to JTAG (Joint Test Action Group) hardware co-simulation. This is implemented with the System Generator Block (SGB). This block is configured according to the target platform and a bit stream (*.bit) file is generated.

In this paper, Spartan 3E starter kit (XC3S500E-FG320) with 50 MHz clock frequency is used for board level implementation and the generated bit stream file is inputted to the selected target. For evaluation different types of images like satellite image, medical images, poor lighting images and foggy images of size 256 × 256 are considered.

The hardware outputs of the proposed design for non uniform illumination correction and low contrast correction of satellite image, medical images and foggy images are shown in Fig. 7 and 8 respectively. From the results it is clear that the proposed design works well for un even illumination and low contrast correction. The same design is also implemented in Spartan 6 FPGA-LX9 Kit (XC6SLX9-2CSG324). The performance of the hardware output is same but the resources usage of XC6SLX9-2CSG324 is little bit higher than XC3S500E-FG320. The resource utilization for non uniform illumination correction and low contrast correction are shown in Table 1 and 2 respectively. Table 3 shows the comparison of resource utilization of FPGA (Spartan 3) for non uniform illumination correction algorithm with existing method [4].

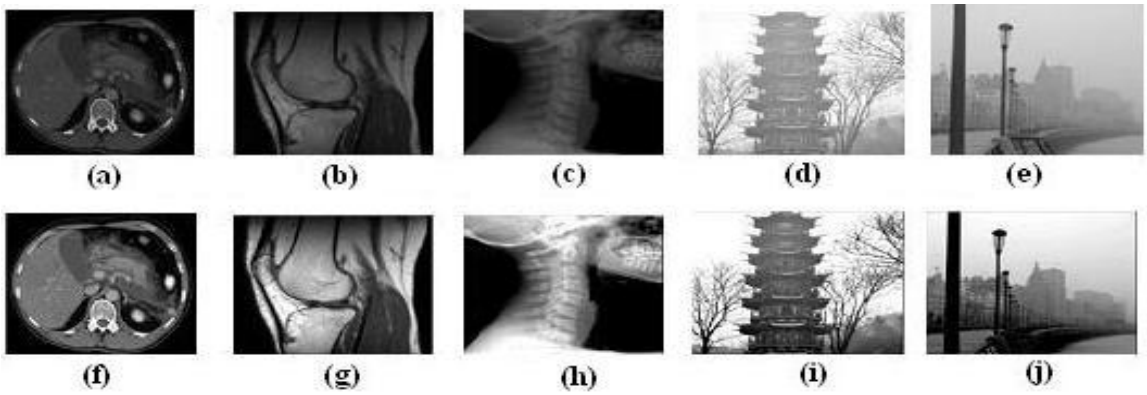

Figure 8: (a), (b), (c), (d) & (e) shows images degraded by low contrast and its hardware co-simulation results for contrast correction are shown in (f), (g), (h), (i) & (j) respectively.

5. Conclusion

The xilinx system generator tool offers a friendly environment design for image processing applications. The processing units of the proposed model are designed by xilinx blocksets. This tool supports software simulation as well as it can be implemented in FPGA boards which offer parallelism, robust and speed. These features are essential for real time image processing. This paper presents a dual architecture for non uniform illumination and low contrast image correction. For evaluating its resource utilization, the dual architecture is implemented in both SPARTAN 3E and SPARTAN 6LX9 FPGA boards. This paper also compares the proposed architecture with the existing work. It shows that the proposed design eliminates the design complexity with minimum resource usage.

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